Fig. 3 Current-voltage characteristics at different incident optical powers at resonance

than intended. Intended base and collector dopings of 5×10^{17} and 5×10^{16} , respectively, would produce a punch-through voltage of ~ 10 V. The operating voltage of 2 V is, however, lower than the punch-through voltage.

In conclusion, we have fabricated a GaAs-based resonant cavity enhanced HPT with a peak responsivity of 110 A/W at 10 μ W incident optical power and a resonant wavelength of 929 nm. This is in the transmission window of the GaAs substrate. The peak responsivity increases from 17 A/W at 0.1 μ W incident optical power to 400 A/W at 100 μ W.

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High temperature InAs infrared detector based on metal-insulator-semiconductor structure

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Indexing terms: Indium compounds, Infrared detectors, Metal-semiconductor-metal structures

The Au/Cr/a-SiN_x/H/(n)InAs/GaAs metal-insulator-semiconductor (MIS) capacitor was fabricated as a basic element of charge injection devices using plasma enhanced chemical vapour deposition. The electrical properties of the capacitor were analysed as a function of temperature using high frequency (1 MHz) capacitance-voltage measurements. It was demonstrated that the capacitor can still be biased into deep depletion at 180 K. When this capacitor is used as an integrated infrared detector in a charge injection device, it exhibits the capacity to detect infrared signals at a temperature of 180 K, higher than that of an InSb infrared detector (77 K), and the device can be cooled thermoelectrically.

Indium arsenide (InAs) is a direct, small energy gap semiconductor. Its energy gap is 0.36 eV at room temperature [1], and increases to 0.41 eV at 77 K. Since its energy gap is larger than that of InSb, InAs infrared detectors can be used in higher temperature applications.

InAs charge injection devices (CIDs) are surface charge devices [2] similar to the charge coupled device (CCD) in that photogenerated charges are collected, integrated, and stored in the metal-insulator-semiconductor (MIS) capacitor. The most critical step in fabricating a CID is the deposition of thin insulator film on the semiconductor. In this Letter, we describe the successful fabrication of Au/Cr/a-SiN_x/H/(n)InAs/GaAs MIS capacitors by plasma enhanced chemical vapour deposition (PECVD). Their electrical properties were analysed using high frequency (1 MHz) capacitor-voltage (C-V) measurements. The results of these experiments demonstrate that this MIS capacitor can be used at a temperature of 180 K, which can be achieved by using a thermoelectric cooler.

The substrates used for fabricating the capacitors consist of a 2 μ m thick undoped InAs epilayer grown on n^+ (100) GaAs substrates [3] using molecular beam epitaxy. The InAs epilayer has a donor concentration of $3 \times 10^{16} \text{ cm}^{-3}$. Before the a-SiN_x/H film was grown on the InAs epilayer, AuGeNi was evaporated onto the back side of the n^+ GaAs substrate and annealed to form an ohmic contact. The a-SiN_x/H films were prepared by PECVD using SiH₄+H₂+NH₃ gases. The flow rates of SiH₄, H₂, and NH₃ were 3.7, 3.7 and 30 sccm, respectively. The thickness of the a-SiN_x/H layer was about 120 nm. The 100 nm Cr and 300 nm Au double layer were evaporated and lifted-off to form the metal gate.

Fig. 1 shows the 1 MHz C-V characteristics of an InAs MIS capacitor for different temperatures. It is clear from Fig. 1 that the C-V curves gradually stretch out as the temperature is increased from 120 to 180 K. This indicates that the interface states can gradually follow the 1 MHz measuring signal and results in large energy loss as the temperature increases. For temperatures beyond 200 K, the generation rate of minority carriers from interface states is so large that the MIS capacitor can no longer function as a charge storage device. When the CID is operated in the charge sharing mode [4, 5], the potential well underneath each CID usually keeps the bias charge at all times. The bias charge helps keep interface states or traps filled, which facilitates an efficient charge transfer. The InAs MIS capacitor 606 was used in the CID read-out experiments. To operate the capacitor in charge sharing mode, two closely spaced metal gates are required. The gate areas are 1.26×10^{-3} , and $1.96 \times 10^{-3} \text{ cm}^2$, respectively. Since the donor concentration of InAs is $3 \times 10^{16} \text{ cm}^{-3}$, the maximum depletion width is only about 146 nm. The gate metal is made very thick so the light cannot penetrate into the semiconductor near the gate area. The sensing area is thus only a narrow ring (hole diffusion length) outside the gate circle, i.e. $2.4 \times 10^{-3} \text{ cm}^2$ if the hole diffusion length is 1.5 μ m. The specific detectivity D^* of InAs CID is measured at 77 K under a 800 K black body radiator with an aperture diameter of 6.4 mm. The measured D^* is about $2.7 \times 10^8 \text{ cm}^2/\text{Hz/W}$.

Fig. 1 Temperature dependence of high frequency (1 MHz) C-V curves of InAs MIS capacitor 606

— 120 K
 --- 140 K
 160 K
 - · - · - 180 K
 - - - - - 200 K

Fig. 2 Waveforms of InAs CID (606) readout signal measured at 77 K in dark and with heat source at distances of 0.5 and 2 cm

— dark
 --- 2cm
 0.5cm

Fig. 2 shows the charge sharing mode waveforms of the CID readout signal at 77 K in dark or with an illuminating heat source at distances of 0.5 and 2 cm. Before the injection (0 to 9 μs), the voltage drop across the load capacitor C_L will be grounded to zero. After a delay of 6 μs, an injection pulse (15 to 28 μs) was applied to the InAs CID to inject the photogenerated signal carriers (holes) into the substrate. The same number of electrons, and hence the same amount of bias charge, will leave the metal gate into C_L , generating a positive voltage. After the injection, the substrate bias voltage immediately returns to the value before injection. At that instant, the inversion charge has no time to form and the depletion width must increase to balance the large bias of the substrate. Meanwhile, negative bias charge flows out of C_L to the gate of the MIS capacitor and results in a steep drop of the output voltage. During integration (28 to 90 μs), positive charges either photogenerated or thermally generated are gradually collected in the potential well and the depletion region must shrink to keep the same voltage drop across the MIS capacitor. The consequence is

that the readout voltage gradually returns to zero. The voltage drop in this time frame is proportional to the photogenerated signal. When a heat source is placed at a distance of 0.5 or 2 cm from the CID, the photogenerated charges increase, and more charges are collected during the integration time. This results in a higher readout voltage as shown in Fig. 2.

Fig. 3 Temperature dependence of waveforms of InAs CID (606) readout signal measured in dark at reset pulse frequency of 91 Hz

— 120 K
 --- 140 K
 160 K
 - · - · - 180 K
 - - - - - 200 K

Fig. 3 shows the temperature dependence of the CID readout signals in dark at a pulse frequency of 91 Hz. When the temperature increases (from 120 to 180 K), dark current increases with increasing carrier generation rate and the CID readout curves decay faster in the integration region. In the injection region, the maximum readout voltage also increases with increasing temperature. This is because the capacitance in the inversion region is larger at a higher temperature (Fig. 1) which results in a larger dark bias charge at the constant injection pulse voltage ($Q = CV$). When the temperature is below 140 K, the depletion layer cannot return to the equilibrium state during the integration period and the potential well is only partially filled. For this reason, the readout voltage at 120 K is smaller than that at 140 K. At a temperature of 180 K, the depletion layer returns to the equilibrium state in about 30 μs. This suggests that the InAs CID circuit can be applied to detect the IR signal at a temperature up to 180 K.

In conclusion, InAs CIDs have been successfully fabricated and are able to detect IR signals up to 180 K. The integration time must be shorter than the time for the dark current to fill the potential well (30 μs). If the interface traps could be reduced, the performance of the InAs CID may be further improved to operate at even higher temperatures (> 200 K).

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Inversion channel vertical cavity double heterostructure optoelectronic switch lasers

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Indexing terms: Photonic switching, Vertical cavity surface emitting lasers

Inversion channel technology provides a straightforward way to integrate lasers with detectors and transistors. One inversion channel laser is the double heterostructure optoelectronic switch VCSEL which is reported here with a 2.1mA threshold for a 10 μm diameter device. A deposited stack of $\text{SiO}_2/\text{TiO}_2$ was used with post-growth etching of the cavity. Excellent electrical switching parameters of $V_{sw} = 13\text{V}$, $V_h = 2.1\text{V}$ and $I_h = 0.5\text{mA}$ were obtained, making the device suitable for the digital optoelectronic sensing of small optical inputs.

Vertical cavity surface emitting lasers (VCSELs) are attractive components for optical interconnects, optical signal processors, telecommunications and many new emerging markets, because of their small size, small beam divergence and potentially low threshold current and cost [1-3]. Most of these applications require digital data transfer and so device structures with inherently digital performance such as the LAOS [4], VSTEP [5], and DOES [6-8] can be used to advantage. In the DOES (double heterostructure optoelectronic switch) laser, the thyristor-like switching action and the dual optical and electrical inputs provide higher functionality than the conventional pn laser with the consequent potential for higher integration and lower power consumption. Previously, a DOES VCSEL was reported with a 4.5mA threshold for a 14 μm diameter device by the use of a post-growth cavity mode positioning technique and a deposited top dielectric stack applied at the end of the processing sequence [8]. In this work, using a dielectric stack for the top Bragg reflector, a threshold of 2.1mA has been achieved in the DOES laser for a device geometry of 10 μm and an output power of 0.64mW. These results are as good as most reported pn laser structures. However, in addition to the lasing property, the DOES laser may be switched optically or by electrical injection from a selfaligned third terminal. Furthermore, the heterostructure field effect transistors (HFETs) formed with the inversion channel can be used to control the switch.

The advantages of the post-growth dielectric stack are numerous. First, it serves to minimise the forward biased series resistance because it eliminates the conduction through the top stack. The Joule heating in this resistance causes voltage drops and temperature rises in the device which substantially degrade the threshold current, the quantum efficiency and the wall-plug efficiency. Secondly, it shortens the growth cycle and results in higher tolerance MBE growth, which improves manufacturability. Thirdly, it allows a wider stop-band and higher reflectivity for a fewer number of pairs when compared with a grown stack, which allows a smoother surface topology for the purposes of integration. Fourthly, it allows a minor adjustment of the cavity to correct for errors in the MBE growth or a major adjustment to alter the emission frequency of the laser. Lastly, it may function as a passivation layer and as an interlevel dielectric for the fabrication of

additional components to build optoelectronic circuits. Eventually the adjustment of the cavity mode by etching should no longer be a requirement when the epitaxial growth is under tight control such that the realised thickness is within a critical tolerance of the intended thickness. This will be an important attribute for those inversion channel lasers in which the ohmic contact is not alloyed.

The DOES VCSEL structure was grown by molecular beam epitaxy (MBE) and the active region consisted of three 80 $\text{\AA}$ strained $\text{In}_{0.20}\text{Ga}_{0.80}\text{As}$ quantum wells. The bottom mirror is a 27 1/2 period GaAs/AlAs distributed Bragg reflector and the cavity length was designed to be 5λ to contain the entire inversion channel structure within the cavity and still achieve controlled switching parameters for the DOES VCSEL. The detailed growth structure of the DOES, including the appropriate barrier and charge sheet dopings, was similar to previously reported edge emitting DOES lasers with strained InGaAs quantum wells. The switching voltage was predicted to be 12V [9].

Fig. 1 Schematic diagram showing cross-section of vertical cavity surface emitting DOES laser

The DOES VCSEL was fabricated by monitoring the reflectivity spectrum of the as-grown wafer with an AVIV spectrophotometer and then determining the required etch back thickness by calculations with the transmission matrix method (TMM) [8]. The lasing occurs in a single mode at 0.98 μm . The laser was then fabricated using the standard proton implant techniques as shown by the device cross-section in Fig. 1. First, hydrogen was implanted into the region above the quantum wells using photoresist masking to force the current flow into the active area and then a mesa was etched to expose the n^+ subcollector layer. In this scheme, both contacts are made on the topside, since the substrate was semi-insulating (SI). It was pointed out previously that the SI substrate is essential to isolate devices and to obtain high speed performance from optoelectronic circuits when the DOES is integrated with other components such as the HFET, in the inversion channel technology. Next the metal contacts were made with lift-off of AuGe/Ni/Au to the n -type subcollector and AuZn/Au to the p -type emitter. After alloying of the contacts, seven pairs of $\text{SiO}_2/\text{TiO}_2$ were deposited for the top mirror, producing a reflectivity of 99.8%.

Fig. 2 CW L-I and I-V characteristics for 10 μm diameter vertical cavity surface emitting DOES laser