Single-switch soft-switching electronic ballast with high input power factor

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Abstract: Design and analysis of a new single-switch soft-switching class-E electronic ballast with high input power factor is presented. Design equations for the optimum operating condition are derived and complete computer analysis performed. It is shown that low duty-cycle control of the class-E ballast can reduce the voltage stress of the controlled switch. A 40-W fluorescent lamp ballast is implemented and experimental recordings verify the analytical results.

1 Introduction

High-frequency electronic ballasts have attracted much attention in recent years. Electronic ballasting for fluorescent lamps greatly improves efficacy, efficiency and compactness. Moreover, with the goal of alleviating problems of noises, line-voltage distortion, and enforcement of new harmonic regulations on the utility line, there is a growing need for electronic ballasts with high input power factor. For this purpose an input current shaper power factor corrector (PFC) can be used in the input stage, in place of the usual diode rectifier followed by a bulk capacitor. This solution, however, may result in unacceptable cost for ballast applications.

Single-switch high input power factor electronic ballasts have been proposed [1, 2] to improve efficiency, reliability, size and weight. The input current shaper and the output high-frequency inverter are combined into one stage. Only one active switch is used. Yet, the single-switch ballast presented by Licitra, etc. [1] would dim when the input sinusoidal voltage crosses zero. Flickering of twice line frequency might appear. Deng and Cuk presented a family of class-E ballasts [2]. Simple structure and high performance are achieved. However, with fixed 50% duty cycle control, the maximum voltage stress on the controlled semiconductor switch is 3.56 times the peak AC input voltage [3, 4]. This peak stress would reach 604/1108V for 120/220V AC input.

In this paper a new single-switch soft-switching electronic ballast with high input power factor is presented. Low duty-cycle control is proposed for this class-E ballast to reduce the maximum switch voltage stress. Design equations for the optimum operating condition to facilitate soft switching are derived and complete computer analysis is performed.

2 Circuit description

The proposed circuit topology is shown in Fig. 1. The basic functions of the subcircuits are:

- EMI filter: filters high-frequency noise
- Bridge rectifier: converts line-frequency AC power to DC
- Prefilter of the EMI filter: filters switching noise
- Current shaper: shapes input current waveform
- Controlled active switch: controls charging/discharging of \( L_1 \)
- Soft switching components: facilitates soft switching of \( S_1 \)
- Energy storage capacitor: reduces output ripples
- Transformer: isolates lamp load from source
- Resonant tank: corrects load angle [5] of resonant tank under proper design of \( L_1 \) and \( C_r \)
- Start-up capacitor: preheats lamp filaments and starts lamp
- Equivalent resistance of lamp

![Fig. 1 Circuit diagram of proposed single-switch electronic ballast](image)

3 Analysis

3.1 Equivalent circuit

The equivalent circuit of the proposed ballast circuit presented in Fig. 1 is shown in Fig. 2a. \( V_{DC} \) represents the rectified and filtered direct voltage before \( L_1 \). \( L_m \) is the magnetizing inductance of the transformer. \( R_p \) represents the primary-side equivalent lamp resistance \( R_L \). Fig. 2b gives the further simplified high-frequency equivalent circuit model. The bulk capacitor \( C_2 \) does not affect the high-frequency operation, so it is shorted...
in the simplified equivalent circuit. A dummy inductor \( L_1 \) is introduced to represent the equivalence of \( L_1 \) paralleling \( I_m \). It is exactly a class-E inverter.

\[ \text{Fig. 2 Equivalent circuits of proposed electronic ballast} \]
\[ \text{a} \] Equivalent circuit of Fig. 1
\[ \text{b} \] Simplified equivalent circuit as class E converter

To facilitate the analysis, the main switch and all other components of the circuit are assumed ideal, so the efficiency of the converter is 100%. The load quality factor of the resonant tank must be high enough to generate a pure sinusoidal output current [6-8]. The damping ratio of the circuit is assumed small enough so that the damping of the switching waveforms can be neglected. The inductor \( L_1 \) need not be infinity to act as a constant-current source. The class-E inverter with finite DC-feed inductance can also perform the soft switching [9, 10].

3.2 Circuit operation

There are two stages of operations in the class-E simplified equivalent circuit:

Stage 1: \( S_1 \) turned off, \( L_1 \) discharged: The equivalent circuit of this stage is depicted in Fig. 3a. The supply current \( i_{L1} \) and the output current \( i_o \) pass through \( C_1 \). The voltage across \( C_1 \), \( V_{C1} \), forms a tilted sine wave as shown in Fig. 4.

\[ V_{C1}(t) = k_1 \sin(\omega_1 t) + k_2 \cos(\omega_1 t) \]

\[ \text{Stage 2:} \quad S_1 \text{ on, } L_1 \text{ charged:} \quad \text{The equivalent circuit of this stage is depicted in Fig. 3b. In this stage the supply current } i_{L1} \text{ and the output current } i_o \text{ pass through } S_1. \]

\[ \text{The current across } S_1 \text{ forms a tilted sine wave as shown in Fig. 4.} \]

3.3 Circuit analysis

Two differential equations can be used to describe the waveform of \( V_{C1} \) and \( i_{L1} \) in stage 1

\[ \begin{cases} \frac{dV_{C1}}{dt} = \frac{dV_{DC} - L_1 \frac{di_{L1}}{dt}}{C_1} \\ \frac{dL}{dt} = i_{L1} - I_0 \sin(\omega t + \varphi) \end{cases} \]

with the boundary conditions for \( V_{C1} \)

\[ V_{C1}|_{t=0} = 0, \quad V_{C1}|_{t=t_{on}} = 0, \quad \frac{dV_{C1}}{dt}|_{t=t_{on}} = 0 \]

where \( \omega = 2\pi f_s \) and \( f_s \) is the switching frequency. \( \varphi \) is the lagged load angle when the output current passes through the resonant network \( L_r - C_r - R \). \( t_{on} = (1 - D)T \), \( T \) and \( D \) are the switching period and duty cycle, respectively. The \( V_{C1} \) waveform can then be solved as

\[ V_{C1}(t) = k_1 \sin(\omega_1 t) + k_2 \cos(\omega_1 t) \]

\[ \frac{\omega}{C_1(\omega^2 - \omega_1^2)} I_0 \cos(\omega t + \varphi) + V_{DC} \]

where \( k_1 \) and \( k_2 \) can be solved by the boundary conditions in eqn. 2

\[ k_1 = -\frac{k_2 \cos(\omega_1 t_{on}) + \frac{\omega_1 \cos(\omega_1 t_{on} + \varphi)}{C_1(\omega^2 - \omega_1^2)}}{-\sin(\omega_1 t_{on})} + V_{DC} \]

\[ k_2 = -V_{DC} + \frac{\omega_1 I_0 \cos \varphi}{C_1(\omega^2 - \omega_1^2)} \]

and \( \omega_1^2 = 1/L_1 C_1 \). The load angle \( \varphi \) can be found numerically from eqn. 4 when the duty cycle is not 20%.

\[ (1 - D) \sin(\omega t_{on} + \varphi) + \frac{1}{2\pi} \left( \cos(\omega t_{on} + \varphi) - \cos \varphi \right) = 0 \]

The output current \( I_o \) can be calculated by solving

\[ I_o \sin(\omega t_{on} + \varphi) - \left( \frac{I_{DC} - D^2 T V_{DC}}{2L_1} \right) = 0, \quad I_o \geq 0 \]

The output lamp resistor \( R \) can be determined from the assumption of input/output power equality as a
first-cut estimate

\[ P = V_{DC} \times I_{DC} = \frac{V_o I_o}{2} = \frac{R I_o^2}{2} \]  \hspace{1cm} (6)

\( C_1 \) can be found by observing no direct voltage across \( L' \):

\[ \frac{1}{T} \int_0^{t_{on}} V_{C_1} dt = V_{DC} \]  \hspace{1cm} (7)

i.e.

\[ \frac{k_1}{\omega_1} [1 - \cos(\omega_1 t_{on})] + \frac{k_2}{\omega_1} \sin(\omega_1 t_{on}) + \frac{I_o}{C_1 (\omega^2 - \omega_1^2)} [\cos(\omega t_{on} + \varphi) - \sin \varphi] + (t_{on} - T) V_{DC} = 0 \]  \hspace{1cm} (8)

Once the circuit parameter has been determined, the voltage stress of \( S_1 \) can be found by solving the instant when the maximum \( V_{C_1} \) occurs

\[ \left. \frac{dV_{C_1}}{dt} \right|_{t=t_{Vmax}} = 0, \quad 0 < t_{Vmax} < t_{on} \]  \hspace{1cm} (9)

i.e.

\[ \omega_1 k_1 \cos(\omega_1 t_{Vmax}) - \omega_1 k_2 \sin(\omega_1 t_{Vmax}) - \frac{\omega^2 I_o \sin(\omega t_{Vmax} + \varphi)}{C_1 (\omega^2 - \omega_1^2)} = 0 \]  \hspace{1cm} (10)

Then the peak voltage stress is derived

\[ V_{S1,\text{max}} = \left. V_{C_1} \right|_{t=t_{Vmax}} \]  \hspace{1cm} (11)

the switch voltage stress is the maximum voltage of \( V_{C_1} \) in eqn. 9.

In the second stage, the current passes through \( S_1 \) can be mathematically expressed as

\[ i_{S1} = i_{L_1} - i_o \]

\[ = I_{L_1}(t_{on}) + \frac{V_{DC}}{L_1} (t - t_{on}) - I_o \sin(\omega t + \varphi) \]  \hspace{1cm} (12)

where \( I_{L_1}(t_{on}) \) is the instantaneous current of \( L_1 \). The instant when the maximum switch current occurs is obtained by solving

\[ \left. \frac{dI_S}{dt} \right|_{t=t_{I_{max}}} = 0, \quad t_{on} < t_{I_{max}} < T \]  \hspace{1cm} (13)

the result is

\[ t_{I_{max}} = \frac{1}{\omega} \left[ \cos^{-1}\left( \frac{V_{DC}}{\omega I_o L_1} - \varphi \right) \right] \]  \hspace{1cm} (14)

or the maximum current occur at \( t = t_{on} \) when eqn. 14 has no solution. Thus the maximum current is

\[ i_{S1,\text{max}} = \left. i_{S1} \right|_{t=t_{I_{max}}} \]  \hspace{1cm} (15)

Fig. 5 shows the simulation waveforms of the \( S_1 \) switch voltage and current for the proposed electronic ballast. The switch stresses against duty cycle \( D \) from 0.5 to 0.2 when \( L_1 \) is operated at continuous conduction mode as shown in Fig. 5a. In the continuous conduction mode, the voltage stress decrease from 3.5 to 2.5 \( V_{DC} \) when \( D \) decreases from 0.5 to 0.3 and the current stress increase from 2.8 \( I_{DC} \) (average output current of \( V_{DC} \)) to 5\( I_{DC} \). This phenomenon is similar at discontinuous mode as shown in Fig. 5b. The low duty cycle operation of the circuit can reduce the voltage stress and increase the current stress. In low-power electronic ballasts design, there is a slight voltage safety margin but a large current safety margin for the switch. For example, the voltage and current rating of IRF740 is 400V/5.5A. If the output power is 40W, usually the peak current of the switch is 1A, much lower than

\[ \begin{align*}
\text{Fig. 5} & \quad \text{Voltage and current waveforms of } S_1 \text{ varied with duty cycle } D \\
& \text{a Continuous mode operation of } L_1, \\
& \text{b Discontinuous mode operation of } L_1 \\
\end{align*} \]
Thus in class-E ballasts one can transfer the voltage stress to the current stress by low duty-cycle operation.

### 4 Power factor correction

For single-stage electronic ballasts, a front-ended discontinuous inductor current mode power factor correction is utilized. The discontinuous-current inductor can be considered as \( L_1 \) in the class-E electronic ballast in Fig. 1. The inductor \( L_1 \) has a critical value when operating at the boundary of continuous and discontinuous mode

\[
L_{1_{\text{max}}} = \frac{DTV_{\text{Sm}}}{{2f_s}} \quad L_1 < L_{1_{\text{max}}}
\]

where \( R_s \) is the equivalent resistor seen at the input of the ballast. The voltage conversion ratio is

\[
M = \frac{B_{\text{boost}}}{V_{\text{Sm}}}
\]

where \( V_{\text{Sm}} \) is the maximum value of input alternating voltage. \( V_{\text{boost}} \) is the boost power factor corrector output direct voltage. In this circuit \( V_{\text{boost}} \) is the DC component of \( V_{C1} \) in stage 1

\[
V_{\text{boost}} = \frac{1}{t_{on}} \int_{0}^{t_{on}} V_{C1} \, dt = \frac{1}{1 - D} V_{\text{DC}}
\]

then

\[
V_{\text{DC}} = M(1 - D)V_{\text{Sm}}
\]

In Fig. 1 \( C_2 \) blocks the DC component of \( V_{C1} \), so

\[
V_{C2} = \frac{1}{T} \int_{0}^{T} V_{C1} = V_{\text{DC}} = M(1 - D)V_{\text{Sm}}
\]

\( C_2 \) must be large enough to hold up the power while the input power decreases. The minimum value of \( C_2 \) can be determined by

\[
C_2 = \frac{P}{\omega L V_{C2} \Delta V}
\]

where \( \Delta V \) is the peak-to-peak ripple of \( V_{C2} \) and \( \omega_L \) is the AC source angular frequency. Figs. 6a and 6b show the ballast output current with large \( C_2 \) and small \( C_2 \), respectively. Obviously, a large \( C_2 \) can avoid the twice line-frequency flicker which causes low-quality lighting and shortens the lamp lifetime.

At discontinuous operation, neglecting the high-order terms, the approximate average input current can be expressed as

\[
i_s = I_{sm} \sin(\omega_L t) \frac{M D}{M - |\sin(\omega_L t)|}
\]

where \( I_{sm} \) is the maximum value of the filtered input current \( i_s \) of the ballast. The plot of average input current against duty cycle is shown in Fig. 7. The power factor varies with duty cycle as given in Fig. 8. The low duty cycle slightly deteriorates the power factor, but it is still higher than 0.95.

### 5 Design procedure

According to the foregoing analysis, the design procedure of the ballast can be outlined as follows:

(i) Determine the lamp equivalent resistance \( R_s \) and the switching frequency \( f_s \). The fluorescent lamp can be modelled as a constant resistor at high-frequency operation [12]. The lamp resistor can be obtained from data sheets or dividing the RMS lamp voltage by the RMS lamp current. The switching frequency is usually in the range of 20k-30kHz, 40k-50kHz and higher than 60kHz to avoid interfering with other electronic apparatus. Choose the duty cycle \( D \) usually at 0.3-0.5 depending on the main switch voltage and current ratings. When \( D = 0.3 \) the maximum voltage on the main switch is about 2.5 times the input direct voltage. When \( D = 0.5 \) the switch stress is 3.5 \( V_{\text{DC}} \).
(ii) Choose the resonant inductor $L_r$ from the following equation:

$$Q_L = \frac{\omega L_r}{R}$$

where $Q_L$ is the load quality factor of the resonant tank. $Q_L$ must be high enough to make the output current sinusoidal, but the higher $Q_L$ also causes the larger $L_r$. The trade-off between the quality of the output and the size and weight of the ballast is the designer’s choice.

(iii) The load angle $\phi$ can be found by eqn. 4, $-90^\circ < \phi < 0^\circ$. Computer-aided numerical approaches are convenient to cope with this nonlinear equation.

(iv) Determine the approximate value of $C_r$ from the following equation:

$$C_r \approx \frac{1}{\omega^2 I_r^2} + \frac{1}{\omega \sin \phi + \omega \frac{\tan \phi}{\cos \phi}}$$

(v) Determine the approximate value of $C_1$ from eqn. 8.

(vi) Calculate the voltage and current stress of $S_1$ from eqns. 8–15. The switch ratings must be greater than these values.

(vii) Determine the energy storage capacitor $C_2$ from eqns. 17 and 18. The voltage across $C_2$ is about the maximum of the input voltage.

(viii) Determine the input inductor $L_1$ from eqn. 16. It is better to design the input inductor value near the boundary of the continuous and discontinuous mode because the maximum current of $i_{L1}$ is smaller.

(ix) The voltage ratings of $D_1$ and $D_2$ are the same as the main switch. The current rating of $D_1$ is the RMS value of the input current. Ideally the current passing through $D_1$ is zero when at optimum operating condition, but actually a small current appears when $S_1$ is turned on.

(x) The rated lamp current might not match the output current $I_0$ in eqn. 5. Adjust the transformer turns ratio to make the impedance matching between the primary and secondary side. Determine the value of $R$, $C$, and $L_2$ from $R_2 = n^2 R$, $C_r = C_r/n^2$ and $L_2 = n^2L_r$, where $n$ is the transformer turns ratio.

(xi) The lamp start-up capacitor $C_s$ is often small compared to $C_r$, so it can be neglected at steady state. When starting the lamp the filament resistance and $L_r - C_s$ form a resonance, the lamp starting voltage and the preheat current are the ratings to determine the value of $C_s$.

(xii) All component values are derived in the ideal condition (100% efficiency), but in the real implementation of the ballast circuit, the soft-switching condition can be achieved by slightly adjusting the value of $C_1$.

(xiii) The EMI filter for the ballast is mainly to suppress the switching noise and its harmonics. Second-order filters are often used in low-cost electronic ballasts. Fig. 9 shows a second-order EMI filter for the proposed electronic ballast. The X-capacitor $C_{X1}$, $C_{X2}$ and differential choke $L_{D1}$, $L_{D2}$ suppress the differential noise. The Y-capacitor $C_{Y1}$, $C_{Y2}$ and the common choke $L_{C1}$, $L_{C2}$ suppress the common-mode noise. The noise must be measured before the filter design. The peak magnitude of the switching noise and frequency determine the filter components. For example, if the switching noise is mainly at 50kHz, and the peak of noise is 100dB/\mu V over the EMC standard by 40dB/\mu V. It must be attenuated 40dB at 50kHz; a second-order filter at the cutoff frequency must be set below 5kHz because a second-order filter provides 40dB per decade attenuation. The filter capacitor $C_f$ across the output of the bridge rectifier is to help filter the high-frequency switching noise.

Fig. 9 EMI filter for proposed single-switch electronic ballast

6 Experimental results

A 40W fluorescent lamp ballast adopting the circuit is developed. Circuit parameters of the experimental ballast in Fig. 1 are $L_1 = 0.9\text{mH}; C_1 = 14.7\text{nF}; L_2 = 2\text{mH}; L_r = 4\text{mH}; C_r = 100\text{nF}; R_2 = 250\Omega; C_2 = 3.3\text{nF}; C_3 = 68\mu F; S_1: IRF830; f_c = 50\text{kHz}; f_r = 110\text{VAC}; D = 0.3$; turns ratio $n = 1:1.25$. The EMI components in Figs. 1 and 9 are: $C_1 = 0.68\mu F; C_{Y1} = C_{Y2} = 1\mu F; L_{D1} = L_{D2} = 2.4\text{mH}; C_{X1} = C_{X2} = 4.7\text{nF}; L_{C1} = L_{C2} = 1.4\text{mH}$.

Fig. 10 Measured voltage and current waveforms of main switch $S_1$

Fig. 11 Measured discontinuous current waveform of $L_1$ for half cycle of line frequency

The recorded voltage and current waveforms of $S_1$ are shown in Fig. 10. The discontinuous current waveform of inductor $L_1$ is shown in Fig. 11. The input and output voltage/current waveforms of the ballast are shown in Figs. 12 and 13, respectively. The maximum voltage stress for $S_1$ is about 400V. The EMC spectra of the proposed ballast are shown in Fig. 14. These spectra are the composed noise of common mode and differential mode. Fig. 14a shows the noise spectrum at the ballast input terminal without the EMI filter except the prefilter $C_f$. The peak noise is 100dB/\mu V at 50kHz.


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The cutoff frequency is set at 5kHz at first and adjusted the components to pass the EMC standard. The final values are 1.6kHz for differential mode and 25kHz for common mode because the common-mode noise is smaller than the differential mode. Fig. 14b shows the noise spectrum with EMI filter which meet VDE-0871 class-B EMC standard. The measured input power factor and input current THD and harmonics are listed in Table 1. The measured efficiency of the ballast is 82%.

### Table 1: Measured input power factor, input current THD and harmonics of proposed single-switch ballast compared with IEC-1000-3-2

<table>
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<th>IEC-1000-3-2 class C equipment</th>
<th>Proposed electronic ballast</th>
</tr>
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<tbody>
<tr>
<td>Power factor</td>
<td>—</td>
<td>0.972</td>
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<tr>
<td>THD</td>
<td>—</td>
<td>14.21%</td>
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<tr>
<td>Order-2 harmonic</td>
<td>2%</td>
<td>0.03%</td>
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<tr>
<td>Order-3 harmonic</td>
<td>30% *λ</td>
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<td>10%</td>
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<td>5%</td>
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<td>Order-11 harmonic</td>
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<td>1.15%</td>
</tr>
<tr>
<td>Order-13 harmonic</td>
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<td>1.61%</td>
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*λ is the power factor

### 7 Conclusions

A single-stage single-switch high-power-factor electronic ballast has been presented. The high-voltage stress problem of class-E type ballasts was solved by the proposed low duty cycle operation. While the duty cycle is less than 0.5 circuit parameters are difficult to determine owing to nonlinear circuit operation. We have proposed design equations and a procedure to determine the circuit parameters. A 40-W ballast was experimentally designed and implemented. The analytical results were verified by experimental recordings.

### 8 References