Design And Implementation of a Microprocessor-Based Intelligent Electronic Meter

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ABSTRACT

This paper presents the design and implementation of a microprocessor-based intelligent electronic measuring apparatus. The meter can measure instantaneous values of voltage, current, and power of electrical power distribution system. A novel random asynchronous sampling technique that samples voltages and currents at predetermined intervals is exploited. Using the proposed random asynchronous sampling technique, the circuit complexity can be reduced. Furthermore, the accuracy of the meter is improved significantly by compensation of phase shift error due to current transformer (CT). Moreover, the A/D quantization error is compensated for low current measurement. A prototype including CT is built to verify the theoretical analysis and examine the performance of the proposed system. The proposed meter can be used as a universal electrical meter for both local power consumption indication and computerized power management system.

I. INTRODUCTION

The conventional Ferraris induction disk metering based on electromechanical principles have been used worldwide since 19th century. Recently, the requirements of precision measurement, data acquisition, energy management, and communication for modern electricity metering have stimulated the idea to develop intelligent meters based on electronic and microprocessor techniques. Several electronic metering systems were presented previously [1] - [6]. Kinston and Woolner developed a combined *Whr* and *Varh* poly-phase meter based on mark-space-amplitude (MSA) multiplier technique [1]. Hutt and Fielden proposed a wholly digital microelectronics meter based on CALMS (Credit and Local Management System) technology [2]. Rozman presented a static watt-hour meter based on Hall effect [3]. Summers utilized oversampled A/D conversion technique to develop an integrated meter for remote telemetering applications [4]. Hill described a low-cost microprocessor-based wattmeter for the measurement of power from a sinusoidal source [5]. Triger proposed the concept of a universal digital meter using a sampling technique [6].

However, most existing electronic metering systems have the following disadvantages: high circuit complexity, large error for low current measurement, inherent power measurement error due to phase shift of current transformer (CT) or potential transformer (PT). This paper proposes a microprocessor-based intelligent meter, in

which the error for low current measurement due to A/D quantization is improved, and the power measurement error due to the phase shift of CT is compensated by software technique.

II. SYSTEM BLOCK DIAGRAM

The functional block diagram of the proposed meter is illustrated in Fig. 1. The meter consists of the following major blocks: Transducers (CT and PT), Phase lead/lag detector (ZCD circuits), sample-and-hold (S/H 1 ~ S/H 3) circuits, multiplexer (MUX), A/D converter (ADC), and microprocessor (μP). In our system, the input voltage (110 Vrms $\pm 10\%$) is attenuated by a resistor divider (with attenuation ratio of 1/34) to produce a voltage of ± 5.0 V (peak-to-peak), which is suitable for the processing of subsequent S/H and A/D converter stages. A resistor divider is used as PT (potential transformer) in our design. The CT used in our system provides the conversion ratio of 0.025 V/A. Two amplifiers with voltage gain of $A_{V1} = 10$ and $A_{V2} = 5$ are employed to amplify the output signal from CT.

Fig. 1 Functional block diagram

The phase lead/lag detector is composed of two zero-crossing detectors (ZCDs). One ZCD is employed to detect the zero-crossing point of voltage waveform, the other ZCD to detect the zero-crossing point of current waveform.

The S/H is an analog voltage storage device in which an input voltage is sampled and then stored on a capacitor. The sampling rate, operating at 481 samples/sec, is generated by the timing circuit in the microprocessor. The 481 Hz timing signal is used to control S/H from the "sample" state to the "hold" state. The input voltage which occurs at the time of "hold" command is retained for subsequent A/D conversion.

The multiplexer is employed to provide time sharing of an A/D converter among a number of different analog input channels. As shown in Fig. 1, the analog outputs from three S/Hs, representing voltage (S/H 1), high level current (S/H 2), and low level current (S/H 3), are applied to the input channels of the multiplexer. One input channel is selected at a time for connection to the multiplexer output by the command from microprocessor.

III. SYSTEM OPERATION PRINCIPLE

An electronic meter needs to measure the electrical parameters such as voltage, current, and power, etc. Measurement of the true rms value for instantaneous voltage and current using traditional analog method becomes difficult if the input waveform is non-sinusoidal or distorted sinusoidal [7]. The digital sampling method is a good alternative to solve this problem. A number of sampling techniques, such as real time sampling, asynchronous sampling, and random repetitive sampling, are available. A novel random asynchronous sampling technique, illustrated in Fig. 2, is utilized in this paper. The sampling occurs asynchronously with the input signal being measured. This sampling method captures data on the input waveform by acquiring sampling points on more than one cycle of the input signal. On each occurrence of the trigger event, a few more points in one input signal cycle are acquired after waiting a predetermined amount of time from triggering point. The predetermined time interval is incremented for each successive input cycle. After a number of cycles, the waveform is reconstructed from all the sampled points. This sampling technique alleviate speed requirements of hardware, and thus circuit complexity can be reduced significantly. Assume the frequency of input signal and sampling frequency are f_m and f_s respectively, then the total sampling points in one cycle (pass) will be f_s/f_m . From Fig. 2, the number of samples per second is f_s , and the time interval between two consecutive sampled point for successive cycles is $1/f_s$ second.

Fig. 2 Random asynchronous sampling technique

Assume there are M samples per second, and the sampled voltage and current values are V_k and I_k respectively, then the rms voltage (V_{rms}), rms current (I_{rms}), and average power (P_{avg}) can be calculated as follows:

$$V_{rms} = \sqrt{\frac{\sum_{k=1}^M V_k^2}{M}} \quad (1)$$

$$I_{rms} = \sqrt{\frac{\sum_{k=1}^M I_k^2}{M}} \quad (2)$$

$$P_{avg} = \frac{1}{M} \sum_{k=1}^M V_k I_k \quad (3)$$

The digitizing error (ϵ) due to sampling of M samples in the period from $t = 0$ to $t = T$ can be calculated as follows [8].

$$\epsilon = \sqrt{\frac{2}{M} \sum_{k=1}^M \sin^2 \frac{2\pi(k-1)}{M}} - 1 \quad (4)$$

A phase shift, denoted by α , exists between the secondary current and primary current of a CT. Assume the phase angle between voltage and current is θ , then the power error (ϵ_p) between the measured power (P_m) and true power (P_t) is found to be

$$\epsilon_p = P_m - P_t = \cos \alpha - 1 - \sin \alpha \tan \theta \quad (5)$$

Form (5), it is obvious that the power error becomes large when θ is close to 90° . The relationship between the power error and the phase angle θ at the phase shift of $\alpha = 1^\circ$ is shown in Fig. 3.

Fig. 3 Power error versus phase angle θ

In our system, the error compensation due to phase shift in CT is based on the following formulas [8].

1) $\theta > 0$ (I leads V)

$$P_t = P_m \cos \alpha + \sqrt{(V_{rms} I_{rms})^2 - P_m^2} \sin \alpha \quad (6)$$

2) $\theta < 0$ (I lags V)

$$P_t = P_m \cos \alpha - \sqrt{(V_{rms} I_{rms})^2 - P_m^2} \sin \alpha \quad (7)$$

VL ANALYSIS OF CURRENT TRANSFORMER

Current transformer is frequently used to facilitate the measurement of large current flowing through a conductor of an AC power circuit. As illustrated in Fig. 4(a), a CT is comprised of three major parts: primary winding, secondary winding, and ferrite core. In Fig. 4(a), i_1 is the current flows in the primary winding and i_2 is the current induced in the secondary winding. Other related parameters are as follows: μ is the permeability of the ferrite core; A is the cross section of ferrite core; l is the average length of the magnetic flux path; N_1 and N_2 are the number of turns of the coils in the primary and secondary winding; R_s is the load resistance of CT; r is the DC resistance of the secondary coils.

Fig. 4 Current transformer
(a) Construction (b) Equivalent circuit

The amplitude response $|G(j\omega)|$ and phase angle $\theta(j\omega)$ of the transfer function of CT can be found from [8].

$$|G(j\omega)| = \left| \frac{I_2(j\omega)}{I_1(j\omega)} \right| = \frac{N_1}{\sqrt{N_2^2 + \left[\frac{(r + R_s)l}{N_2 A \omega \mu} \right]^2}} \quad (8)$$

$$= \frac{1}{\sqrt{N^2 + \left[\frac{(r + R_s)l}{NA \omega \mu} \right]^2}}$$

$$\theta(j\omega) = \pi + \tan^{-1} \frac{(r + R_s)l}{N_2^2 A \omega \mu} \quad (9)$$

where the turns ratio $\frac{N_1}{N_2} = N$

The response curves of (8) and (9) are indicated in Fig. 5. It is observed that the phase shift is close to -180° when frequency is higher than 100 Hz. The phase shift in the

secondary coil is about -178.1° at the operating frequency of 60 Hz.

Fig. 5 Frequency response of the CT transfer function
(a) Amplitude response (b) Phase response

From (8), assuming that the amplitude error due to frequency response is less than δ , i.e.

$$\frac{1}{N} - \frac{1}{\sqrt{N^2 + \left[\frac{(R_s + r)l}{NA \omega \mu} \right]^2}} < \delta \quad (10)$$

$$\text{let } k = \left[\frac{(R_s + r)l}{NA \omega \mu} \right] \quad (11)$$

then

$$N \geq \frac{k(1 - \delta)}{\sqrt{2\delta - \delta^2}} \quad (12)$$

If $r = aR_s$, then (10) can be modified to

$$k = \frac{(1 + a)l}{A \omega \mu} \frac{R_s}{N} \quad (13)$$

The conversion ratio of CT is

$$\alpha = \frac{R_s}{N} \quad (14)$$

Substitute (13) into (12), we obtain

$$k = \frac{(1 + a)l}{A \omega \mu} \alpha \quad (15)$$

V. DESIGN CONSIDERATIONS

The analysis and design consideration of CT have been discussed in previous section. The design consideration for electronic circuitry and microprocessor operation are presented as follows.

A voltage divider made of two resistors (R_5 and R_6) with a attenuation of approximately 3% is required to convert 171 V to 5 V for A/D conversion.

$$\frac{R_5}{R_5 + R_6} = \frac{5V}{171V} = 0.02924 \quad (16)$$

The capacitor voltage on sample-and-hold circuit in the "hold" mode at $t = t_1$, is

$$v_i(t) = V_0 e^{-\frac{t-t_1}{RC}} + V_1 (1 - e^{-\frac{t-t_1}{RC}}) \quad (17)$$

where $v_i(0) = 0$, and $v_i(t) = V_1$ for the sampling interval from t_1 to t_2 .

The time constant (τ) of the holding circuit should be selected as $\tau > 5RC$ in order to obtain error less than 1%.

The settling time for voltage follower used in the output of multiplexer is

$$t_s = \frac{2F_{ADC}}{SR} \quad (18)$$

where $\pm F_{ADC}$ is the full scale voltage of A/D converter, and $2F_{ADC}$ is the maximum output voltage swing of voltage follower.

The resolution of the A/D converter can be determined as follows. Assume the minimum input voltage to A/D converter is represented by pF_{ADC} ($p=0.01-0.1$ for normal application), and the required meter accuracy by ϵ . Then bits number (Q) of A/D converter can be found from the following equation.

$$Q \geq \log_2 \frac{0.5}{p\epsilon} \quad (19)$$

The microprocessor is the heart of the electronic meter. The random asynchronous sampling method, the computation algorithm are all realized by microprocessor software. Intel 8751 8-bit micro-controller has been chosen in our design to design a cost-effective electronic meter with less component counts.

VI. PROTOTYPE DESIGN

A prototype is built to verify the performance of the proposed system. An electronic meter including CT which can meet the following specifications is to be designed and implemented: full scale voltage $V_F = 120V$ (rms); full scale current $I_F = 20A$ (peak); input signal frequency at $60 \text{ Hz} \pm 3 \text{ Hz}$; voltage accuracy at 1% (from $0.1V_F$ to V_F); current accuracy at 1% (from $0.1I_F$ to I_F); power accuracy at 2% (from $0.01 I_F$ to I_F at 110V).

1. CT Design

In our system, a CT with conversion ratio of $\alpha=0.025V/A$, accuracy of $\delta = 0.1\%$, and frequency response of $f > 60 \text{ Hz}$ is to be designed:

A ferrite core TDK H5C2/EE28 is chosen, which has the following parameters: relative permeability $\mu_r = 10000$; core area $A = 38.4 \text{ mm}^2$; core length $l = 53.88 \text{ mm}$. Substitute above parameters into (15), we can calculate the value of k .

$$k = \frac{(1+a)l}{A \omega \mu} \alpha = 10.6(1+a) \quad (20)$$

With accuracy requirement of $\delta = 0.1\%$, and substitute this value into (14), we obtain

$$N > \frac{k(1-\delta)}{\sqrt{2\delta-\delta^2}} \quad (21)$$

From (20), (21) and $a = 1$, we obtain $N > 348$. Therefore $N = 400$ is selected. Since $N_1 = 1$ is used in our design, we obtain $N_2 = 400$ turns.

From (14) $\alpha = R_s/N$. Since $\alpha = 0.025$, $N = 400$, we have $R_s = 10 \Omega$.

2. Hardware Design

The design considerations described in Section V are used as a guideline for circuit design. The complete hardware circuit is illustrated in Fig. 6. The design of each block is explained as follows:

In order to obtain 0.25 V/A and 1.25 V/A from CT, a 2-stage amplifier using OP07 is designed with gain of $A_{V1} = 10$ and $A_{V2} = 5$.

Fig. 6 Hardware circuit

From (16), a voltage divider (R_5 , R_6) with attenuation ratio at $1/34$ is used. In order to meet condition of power consumption less than $0.1W$, R_5 and R_6 can be found as $R_5 = 3536 \Omega$ and $R_6 = 117464 \Omega$. We choose $R_5 = 3K$, $R_6 = 100K$ in our design.

LF398 IC is chosen to design S/H circuit. R_7 (1K, VR), R_8 (24K) are used to adjust offset voltage. With sampling time at $100\mu\text{s}$ and the condition of $\tau > 5RC$, the capacitance value of the holding capacitor is chosen as

$C > \frac{100\mu\text{s}}{5R}$. Since $R = 300\Omega$ inside LF398, we obtain $C > 0.0167\mu\text{F}$. A capacitor of $C = 0.0333\mu\text{F}$ is selected.

LM311 comparator IC is used to design ZCD circuit (A6 & A7). $R_9=1\text{K}$, $R_{10}=10\text{K}$, $R_{11}=268\Omega$ are selected to provide hysteresis voltage of 30 mV in our design.

CD4066 IC (A4) is used as analog multiplexer. The output of A4 is connected to a voltage follower designed by LM318 (A5). The output of A5 is applied to an A/D converter.

The required bits number of A/D converter is determined by the conditions of error ($\varepsilon \leq 1\%$), and minimum voltage input at $0.1V_F$ ($p=0.1$). From (19), we have $Q \geq 10$. Therefore a 12-bit successive approximation A/D converter IC (AD574A) is selected.

VII EXPERIMENTAL RESULTS

The test results of the prototype is shown in Fig. 7. The rms voltage measurement result is indicated in Fig. 7(a). It is observed that the error is less than 0.5% for input voltage less than 30V. The rms current measurement result is indicated in Fig. 7(b), in which the error is less than 0.5% for the input current less than 1A. For current input less than 0.68A, the error increases rapidly.

The average power measurement result is indicated in Fig. 12(c). The error result for power factor at PF=1, PF=0.6 (lead), and PF=0.6 (lag) are indicated, respectively. It is observed that the error of power measurements is less than 2% for power factor ranged from 0.6 (I leads V) to 0.6 (I lags V).

IX. CONCLUSION

An intelligent meter using electronic and microprocessor-based technique has been designed and implemented. Using the random asynchronous sampling method, the circuit complexity is reduced. Furthermore, the system accuracy is improved significantly due to compensation techniques exploited for error due to phase shift and low current measurement. Moreover, the functions of the intelligent meter are configurable by software; this provides the flexibility for adding different metering applications. The proposed system can be expanded to include data acquisition and communication capability to facilitate precise control of power consumption for efficient energy management. Based on the proposed hardware/software architecture, a high performance intelligent meter can be built cost-effectively.

Fig. 7 Experimental measurement result
(a) rms voltage (b) rms current (c) average power

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