Ultra-Low-Voltage Mixer and VCO in 0.18- μm CMOS

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Abstract — Ultra-low-voltage techniques for RF frontend circuits are presented in this paper. Using a standard 0.18- μm CMOS technology, a down-conversion mixer and a voltage-controlled oscillator were designed and fabricated for 5-GHz wireless applications. With a 5.2-GHz RF signal, the mixer has a conversion gain of 3 dB, while the VCO exhibits a tuning range of 8.9% and a phase noise of -97 dBc/Hz at 1-MHz offset. Both circuits operate at a reduced supply voltage of 0.6 V. The power consumptions of the mixer and the VCO are 792 and 696 μW , respectively.

Index Terms — CMOS RF, mixers, voltage controlled oscillators, ultra-low-power, ultra-low-voltage.

I. INTRODUCTION

With recent advances in semiconductor technology, CMOS provides a promising solution for the integration of the RF frontend with the baseband circuitry in a single chip. The trend of high-level integration significantly reduces the implementation cost and the operation power of commercial wireless products. Fully integrated wireless transceivers fabricated in CMOS technologies have been reported [1]–[3] for all kinds of wireless applications, such as cellular phones, global positioning systems and wireless local-area-networks. In addition to standard wireless communication systems, the development of ultra-low-power and ultra-low-voltage RF techniques has attracted great attention in recent years due to the emerging applications such as RFID and wireless sensor networks.

Because of the required threshold voltage and the inherently low transconductance of the MOSFETs, it is extremely difficult to operate RF frontend circuits with a reduced supply voltage and power dissipation, especially for multi-gigahertz applications. Using a standard 0.18- μm CMOS technology, a down-conversion mixer and a VCO are presented to demonstrate the potential of CMOS frontend circuits for low-power and low-voltage operation. With the proposed topologies, the fabricated circuits operate at a reduced supply voltage of 0.6 V with a power consumption less than 1 mW while maintaining reasonable performance at 5-GHz frequency band.

Section II of this paper presents the proposed circuit topologies of the mixer and the VCO. The experimental results of the fabricated circuits are shown in Section III.

Fig. 1. Schematic of the ultra-low-voltage mixer.

Finally, a conclusion is provided in Section IV of this paper.

II. CIRCUIT DESIGN

A. Down-Conversion Mixer Topology

Figure 1 shows the schematic of the proposed down-conversion mixer with all on-chip components. In order to achieve the highest possible conversion gain with a reduced supply voltage and power dissipation, a folded single-balanced mixer topology with a current bleeding technique is employed. As shown in Fig. 1, M_{N1} is used as the input stage for the RF signal, while M_{P1} and M_{P2} act as the switching pair driven by the LO signals. The RF current generated by the transconductance of M_{N1} is directed to the source of the switching pair through the bypass capacitor C_1 , providing frequency conversion of the single-balanced mixer. In this design, resistors R_1 and R_2 are used as the loads of the switching pair. The values of the resistive loads are chosen to maximize the conversion gain. Due to the supply voltage limitation, a current bleeding technique provided by R_3 is employed. As part of the bias current flows through R_3 , large voltage

Fig. 4. The conversion gain of the mixer versus LO power.

Fig. 5. The measured P_{in-1dB} and IIP_3 of the mixer with input frequency spacing of 10 MHz.

is achieved at the RF port with the source degeneration of M_{N1} . An input return loss better than 10 dB is obtained at the RF frequency band.

The linearity of the mixer was characterized by measuring the P_{in-1dB} and the IIP_3 of the circuit as shown in Fig. 5. Based on a two-tone test with an input frequency spacing of 10 MHz, the measured P_{in-1dB} and IIP_3 are -15 and -8 dBm, respectively. The performance of the proposed mixer is summarized in Table I together with the results from the previously published data [4]-[6] for comparison. As indicated in Table I, the mixer presented in this work exhibits the lowest power consumption and supply voltage for active mixers while maintaining a reasonable conversion gain at the 5-GHz frequency band.

Fig. 6. The frequency tuning characteristics of the VCO.

Fig. 7. The phase noise measurement of the VCO.

B. VCO

The fabricated VCO was tested for ultra-low-power and ultra-low-voltage operation. The VCO core consumes a dc power 696 μ W from a reduced supply voltage of 0.6 V. Figure 6 shows the frequency tuning characteristics of the VCO. As the controlled voltage sweeps from 0 to 0.6 V, the oscillating frequency varies from 5.55 to 6.05 GHz, exhibiting a frequency tuning range of 8.9%. The phase noise measurement of the VCO is illustrated in Fig. 7. With an output frequency of 5.8 GHz, the measured phase noise is -97 dBc/Hz at 1-MHz offset. The performance of the VCO is summarized in Table II.

TABLE I
PERFORMANCE SUMMARY OF THE LOW-POWER
AND LOW-VOLTAGE MIXER

	This Work	[4]	[5]	[6]
Technology	0.18- μ m CMOS	0.18- μ m CMOS	0.18- μ m CMOS	0.35- μ m CMOS
RF/LO Frequency (GHz)	5.2/5.1	5.8/5.6	2.4/2.3	5.01/5
Supply Voltage (V)	0.6	1.5	1.8	1
DC Power (mW)	0.792	6.89	5.94	0.4
Convergent Gain (dB)	3	7	6.7	6
IIP ₃ (dBm)	-8	-2.94	-7.5	5
P _{in-1dB} (dBm)	-15	—	-18	—

IV. CONCLUSION

In this paper, low-voltage circuit topologies have been proposed for RF applications. Using a standard 0.18- μ m CMOS process, the RF frontend circuits are designed for wireless communications at 5-GHz frequency band. The single-balanced mixer employs a folded circuit topology with a current-bleeding technique. The fabricated circuit exhibits a conversion gain of 3 dB with a 5.2-GHz RF frequency while consuming a dc power of 792 μ W from a supply voltage of 0.6 V. The cross-coupled LC-tank VCO topology is modified for low-voltage operation by eliminating the tail transistor. Drawing a dc current of 1.16 mA from a 0.6-V power supply, the VCO has a frequency tuning range of 8.9% and a phase noise of -97 dBc/Hz at 1-MHz offset. The proposed down-conversion mixer and the VCO demonstrate the potential of implementing CMOS RF circuits for ultra-low-power and ultra-low-voltage applications.

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TABLE II
PERFORMANCE SUMMARY OF THE LOW-POWER
AND LOW-VOLTAGE VCO

	This Work	[7]	[8]	[9]
Technology	0.18- μ m CMOS	0.25- μ m CMOS	0.18- μ m CMOS	0.25- μ m CMOS
Supply Voltage (V)	0.6	0.85	0.8	0.7
DC Power (mW)	0.696	4.08	—	2
Tuning Range (GHz)	5.6-6.1	3.65-4	4.4-4.6	2.2-2.5
Tuning %	8.9%	5%	4.4%	13%
Phase Noise (dBc/Hz)	-97 @ 1MHz	-79.24 @ 100 kHz	-100 @ 500 kHz	-118.1 @ 1MHz

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