Impact of Bias Schemes on Doherty Power Amplifiers

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Abstract—This paper investigates the performance of a 2.4-GHz CMOS two-way Doherty power amplifier with the different bias schemes for the auxiliary power device. For the conventional bias schemes, there are design tradeoffs in terms of power gain, gain flatness, P_{1dB} , power-added efficiency, and third order harmonics. An adaptive bias scheme is proposed to bias the auxiliary device at class C for low power operation and at class AB for high power operation. It is shown that the adaptive bias scheme can achieve excellent performance without compromising some characteristics.

I. INTRODUCTION

Mobile communications have been very popular and almost indispensable. To extend the operation and standby time of mobile communication devices, the efforts on reducing power consumption is never enough. It is well known that power amplifier (PA) is one of the most power hungry components in a RF transceiver system. The efficiency issues of power amplifiers become more severe when the modulation techniques which result in high peak-to-average power ratios, such as the prevailing OFDM, are adopted in the modern wireless communications. Typical power amplifiers have decent power efficiency at the peak output power, but their efficiency declines dramatically when they are operated at the 6-dB or more back-off, for example, the average output power levels of the OFDM systems.

The Doherty amplifier architecture is a promising technique to tackle the efficiency issues of the systems with high peak-to-average power ratio. A classical Doherty power amplifier architecture [1], [2], shown in Fig. 1, consists of one main power device and one auxiliary power device. The main device is operating normally and the auxiliary device is off in the low power regime. For high output power, the main device is operating at saturation region to achieve high efficiency and the auxiliary PA is providing the additional power required. The typical efficiencies of a Doherty PA and a conventional PA are compared in Fig. 2. The bias schemes of the main and auxiliary devices in the Doherty architecture will definitely affect the performance of whole PA system. However, the

impact of the bias schemes on the gain, linearity, and efficiency of the Doherty has not been well studied yet.

This paper reports the design trade-off of different bias schemes on the Doherty PA in terms of P_{1dB} , power gain flatness, back-off efficiency and the third order harmonics (TOH).

Fig. 1. The classical Doherty power amplifier architecture.

Fig. 2. The efficiency of a typical power amplifier and Doherty PA.

II. POWER AMPLIFIER IMPLEMENTATION

The 2.4-GHz Doherty amplifier was designed using the 0.18- μm CMOS technology and a 40-mil-thick FR-4 board. The 0.18- μm CMOS technology has the dual gate option and the thick oxide devices have higher breakdown voltage for power amplifier implementation. For a two-way Doherty amplifier to get an efficiency peak at the 6-dB backoff from the $P_{1\text{dB}}$, the ideal scaling ratio between the sizes of the auxiliary and main power devices is 2:1 [3]. However, because the auxiliary power device can not reach the required magnitude of current at the maximum drive, the scaling ratio of 3:1 was chosen. The total gate widths of the main and auxiliary power devices are 420 μm and 1260 μm , respectively. The design goal is to keep the efficiency above 40% at the 6-dB backoff from the peak power operation in an OFDM system.

The investigation of the impact on the performance of the Doherty PA focuses on the bias scheme of the auxiliary power device. The main power device of the Doherty amplifier is biased at class AB to provide linear output power when the auxiliary power device is not turned on. If the main device is biased at class B or C, the power gain flatness will be degraded in the low power operation regime. The auxiliary power device will be biased at class AB, B, and C for the performance investigation in terms of power gain, linearity, and efficiency. The adaptive bias scheme which can offer the excellent tradeoff between output power, linearity, and efficiency is proposed.

III. OUTPUT POWER AND LINEARITY

For the auxiliary device operated at deeper class AB than the main device, the total linear power gain is higher than the other bias schemes under investigation. The auxiliary device has started working at low input power. As the input power is increased to more than -10 dBm, the auxiliary device will provide more power than needed and the total output power gain will have a “mound” in the high power regime. For the class-B bias scheme, the power gain flatness is pretty good in general. The output power begins dropping when the input power reaches 5 dBm. It is because the main device has been saturated and the auxiliary device can not deliver enough current or power. For the class-C bias scheme, the power gain degradation is more severe than the class-B bias scheme. The power gain begins to decline even before the input power reaches 0 dBm. The significantly deteriorated power gain limits its usable operation power range. The power gain with respect to input power of the Doherty PA under different bias schemes is shown in Fig. 3.

The third order harmonics (TOH) of the Doherty PA with the different bias schemes are shown in Fig. 4. The class-C bias scheme presents very low TOH. It is because the TOH of the main and auxiliary devices are not in phase and tend to cancel out with each other [4]. The class-B bias scheme has the worst TOH performance in the low power regime, but its performance improves, even better than class-AB bias scheme, as the output power increases.

Fig. 3. The output power gains of the Doherty PA for the different bias schemes on the auxiliary power device.

Fig. 4. The third order harmonics of the Doherty PA for the different bias schemes on the auxiliary power device.

IV. EFFICIENCY

The Doherty power amplifier architecture arranges nicely such that the auxiliary device starts to work as the main device is saturated to boost the overall efficiency at the low power regime. The power-added efficiency (PAE) of the Doherty PA with differently biased auxiliary devices respect to the output power is shown in Fig. 5.

As expected, the class-C bias scheme exhibits better PAE than the other bias schemes because the auxiliary device is hardly turned on until the main device is saturated. The class-AB bias scheme has the worst PAE characteristics. For the output power of 16 dBm, the class-C bias scheme has the PAE 8% higher than the class-B bias scheme and

15% higher than the class-A bias scheme. However, the excellent PAE performance of the class-C bias scheme comes along with the obvious clip on the power gain characteristics, as shown in Fig. 3.

If the auxiliary device turned on in the low-power operation regime, like the class-AB bias scheme, the efficiency of the auxiliary device will play an important role in the total efficiency. Raising the bias voltage of the auxiliary device will make the PAE curve approach to that of the conventional Class-AB amplifier.

Fig. 5. The PAE vs. output power characteristics of the Doherty PA for the different bias schemes on the auxiliary power device.

V. ADAPTIVE BIAS SCHEME

The clip on the gain of the class-C biased Doherty PA results from the insufficient bias voltage of the auxiliary device from the moderate to high power regime. If the auxiliary device can be biased at class C in the low-power

operation region and class AB in the high-power operation region, so called adaptive bias scheme [5], the excellent PAE characteristics can be achieved without sacrificing the gain flatness. The configuration of an adaptive-biased auxiliary amplifier is shown in Fig. 6. The adaptive bias circuit needs to detect the input power and adjust the DC bias accordingly.

Fig. 6. The Adaptive bias circuit for the auxiliary amplifier.

Fig. 7. The adaptive bias voltage with respect to the input power.

TABLE I. COMPARISON OF THE DOHERTY PA WITH DIFFERENT BIAS SCHEMES

Auxiliary power device	Class AB	Class B	Class C	Adaptive Bias
Power gain	○ (12.3 dB)	△ (11.5 dB)	△ (11.5 dB)	△ (11.1 dB)
P_{1dB}	○ (22.2 dBm)	○ (22.1 dBm)	× (16.5 dBm)	○ (23.1 dBm)
PAE _{6dB} (6-dB back-off from P_{1dB})	× 32.5%	△ 37.8%	× 15 % ○ 44.2 % @ 15 dBm*	○ 46.5 % @ 17 dBm
Gain flatness	△	○	×	○
TOH	×	△	○	○
Chip size	○	○	○	△**

○: good △: medium ×: bad

* The P_{1dB} is 16.5dBm for the class-C bias scheme. Therefore, the efficiency at the 6-dB backoff will degrade significantly. However, its efficiency is very good as the output power is 15 dBm.

** The adaptive bias circuit will increase the die estate about 10~30 %.

The proposed adaptive bias scheme can be fit into the following equation:

$$V_g = 0.4078 + \frac{0.3159}{1 + \frac{e^{-P_{in} + 11.2789}}{0.5253}} \quad (1)$$

where V_g is the adaptive bias voltage and P_{in} is the input power in dBm. The bias voltage variation with respect to input power is shown in Fig. 7. The power gain of the adaptive bias scheme with respect to input power is shown in Fig. 3. Although the gain is a little bit lower than the other bias scheme, the gain flatness vs. input power is excellent and its P_{1dB} is actually the highest. The TOH characteristic of the adaptive bias scheme is also very good as shown in Fig. 4. The efficiency of the adaptive bias scheme, shown in Fig. 5, seems to be just a little better than that of the class-C bias scheme, but it may be misleading. If the efficiency at the output power of 6-dB backoff from P_{1dB} is scrutinized, the efficiency of the adaptive bias scheme is 46.5% higher than that of the class-C bias scheme. The proposed adaptive bias scheme can maintain the excellent efficiency and TOH without sacrificing the gain flatness, but some design issues must be handled properly such as time delay, matching, sensitivity, etc.

VI. CONCLUSION

The investigation result of the different bias schemes for the Doherty PA is summarized in Table I. The class-A bias scheme can deliver good power gain, the class-B bias scheme can offer good efficiency for backoff operation, and the class-C bias scheme can provide good TOH characteristics. There are obvious design tradeoffs between different bias schemes. The proposed adaptive bias scheme which biases the auxiliary power device at class C for low power operation and class AB for high power operation demonstrates the excellent performance for all of gain flatness, P_{1dB} , PAE at 6dB-backoff, and TOH.

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REFERENCES

- [1] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, Norwood, MA, 1999.
- [2] S. C. Cripps, *Advanced Techniques in RF Power Amplifier Design*, Artech House, Norwood, MA, 2002.
- [3] M. Iwamoto, A. Williams, P. Chen, A.G. Metzger, L.E. Larson, and P.M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Microwave Theory Tech.*, vol. 49, pp. 2472-2479, Dec. 2001.
- [4] Youngoo Yang, *et al.*, "A Microwave Doherty Amplifier Employing Envelope Tracking Technique for High Efficiency and Linearity," *IEEE Microwave and Wireless Components Letters*, vol. 13, pp. 370-372, Sep. 2003.
- [5] B. Sahu, G. A. Rincon-Mora, "A high-efficiency linear RF power amplifier with a power-tracking dynamically adaptive buck-boost supply," *IEEE Trans. Microwave Theory Tech.*, vol. 52, pp. 112-120, Jan. 2004.
- [6] D. W. Lew, *et al.*, "A design of the ceramic chip balun using the multilayer configuration," *IEEE Trans. Microwave Theory Tech.*, VOL. 49, NO.1, Jan. 2001.
- [7] C. P. McCarroll, G. D. Alley, S. Yates, and R. Matrecci, "A 20 GHz Doherty power amplifier MMIC with high efficiency and low distortion designed for broad band digital communication systems," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2000, pp. 537-540.
- [8] R. J. McMorro, D. M. Upton, and P. R. Maloney, "The microwave Doherty amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1994, pp. 1653-1656.