Integrated CMOS Power Sensors for RF BIST Applications

Hsieh-Hung Hsieh and Liang-Hung Lu

Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan.

hsid@adsi.ee.ntu.edu.tw, lhlu@cc.ee.ntu.edu.tw

Abstract

This paper presents the design and experimental results of fully integrated CMOS power sensors for RF built-in self-test (BIST) applications. Using a standard 0.18- μm CMOS process, the power sensors, on-chip terminations and switches are integrated with a 5.2-GHz variable-gain amplifier. Built-in RF test was performed on the amplifier in the vicinity of 5.2 GHz for demonstration. With the proposed built-in power sensors and BIST technique, the circuit parameters of the amplifier including the forward gain and gain compression were extracted without expensive automatic test equipments while minimum performance degradation of the device under test (DUT) is maintained at multi-gigahertz frequencies.

1. Introduction

With recent advances in CMOS process technology, the concept of system-on-a-chip (SoC) has been realized by integrating more and more digital and analog building blocks in a single chip. Due to the fast-growing market in wireless communications, the demands on low-cost RF systems have motivated the integration of RF frontends into the SoC environment. By implementing all the functional blocks on the same substrate, the RF SoC benefits from reduced hardware cost, lower power dissipation and enhanced system performance. However, the lack of efficient testing techniques, especially for the RF modules, has impeded the development of RF SoC products.

Typical RF testing involves various circuit parameters such as gain, reflection, linearity, signal power and noise. In addition, the performance of an RF frontend is usually defined in frequency domain rather than in time domain. It is extremely difficult to define a standard procedure to achieve RF testing for all wireless standards. Nowadays, test of RF modules still requires expensive automatic test equipments (ATE) which impose restrictions on the cost and the through-

put of high-volume production. In the trend of system integration, the testing issues become crucially important to the success of the RF SoC products. Therefore, the concept of built-in self-test (BIST) was introduced to alleviate the complexity and the cost of RF tests [1]-[2]. In this paper, a novel BIST technique is proposed to extract the forward gain and gain compression of RF amplifiers. With the built-in power sensors and switches, the required RF test functionality can be achieved for multi-gigahertz applications.

The organization of this paper is as follows. Section II describes the proposed BIST architecture and the test methodology. The design considerations and circuit topology of the built-in power sensors and the DUT are presented in Section III. The experimental results and discussion are shown in Section IV. Finally, a conclusion is given in Section V.

2. The proposed RF BIST technique

The block diagram of the proposed BIST architecture is shown in Fig. 1. The BIST module includes two built-in power sensors (BIPSSs), on-chip switches and termination resistors, while a RF amplifier is employed as the DUT in the circuit implementation. Based on the test mechanism, the BIST operation is described in three different modes as follows.

2.1. Calibration mode

To ensure the accuracy of the RF test, a calibration procedure is performed prior to the test. The configuration of the calibration mode is established by the switches as shown in Fig. 1(a), where the DUT is disconnected and the two ports are terminated with the on-chip 50- Ω resistors. As the ports are terminated, the power level of the incident wave from the signal source is proportional to the voltage amplitude observed at the termination. The power sensors are calibrated by feeding a sinusoidal signal to the ports and recording the output readings (V_{OUT1} and V_{OUT2}) during the sweep

Fig. 1. The proposed BIST architecture in (a) calibration mode, (b) test mode and (c) operation mode.

of the incident power level. As a result, the errors caused by the process variation and device mismatch can be corrected for accurate measurement.

2.2. Test mode

During the test mode, the BIST module is reconfigured by on-chip switches as shown in Fig. 1(b). Extraction of the amplifier parameters such as forward gain and gain compression is achieved by the output reading of the power sensors.

2.2.1. Test of the forward gain. The measurement of the forward gain $|S_{21}|$ is achieved by feeding a small-signal sinusoidal wave, which can be provided by either an on-chip synthesizer or an off-chip signal source, to the input port while the output port is terminated. According to the definition of S_{21} , the power gain is therefore approximated as

$$|S_{21}| = |A_2/A_1| \quad (1)$$

when impedance matching is provided at the input of the DUT. Note that A_1 and A_2 represent the amplitudes

measured from the power sensors at port 1 and port 2, respectively.

As indicated in (1), the forward gain of the DUT is extracted by the readings of the power sensors at a given input frequency. Therefore, a complete frequency response can be achieved by repeating the procedures at the various frequencies within the band.

2.2.2. Test of the gain compression. The testing technique of the forward gain is extended for the measurement of gain compression by increasing the power level of the incident wave. From the measured gain versus the incident power level, the input referred 1-dB gain compression can be obtained to characterize the large-signal behavior of the DUT.

2.3. Operation mode

Once the task of RF testing is completed, the power sensors are turned off and the signal path of the DUT is established in the operation mode, as shown in Fig. 1(c). In this design, the influence on the DUT performance due to the existence of the built-in power sensors is negligible. Therefore, the BIST module can either be turned off to minimize the power dissipation or maintain its functionality during the operation mode to provide on-line performance monitoring.

3. Circuit implementations

3.1. Built-in power sensors

Figure 2 shows the schematic of the power sensors used in this BIST design. In order not to disturb the impedance and the power wave in the signal path, a voltage divider (R_1 and R_2) with large resistance values is inserted between the port and the power sensor to minimize the loading effect.

Note that the transistor M_1 is biased in weak inversion by its gate voltage while M_2 and M_3 are saturated. The drain current (i_{D1}) and gate-to-source voltage (v_{GS1}) of M_1 can be expressed as [3]

$$i_{D1} = I_{D0} \left(\frac{W}{L} \right)_1 \exp \left(\frac{v_{GS1}}{\zeta V_T} \right) \quad (2)$$

where V_T is the thermal voltage, ζ is the nonideality factor, $(W/L)_1$ is the aspect ratio of M_1 and I_{D0} is a current constant independent of the gate-to-source voltage. When a sinusoidal wave with an amplitude of A and frequency of ω_b is applied at the port, the output voltage of the power sensor is given as

Fig. 2. (a) The schematic of the power sensors for built-in RF tests, and (b) the spectrum at the critical points of (a).

$$v_{BIPS} = I_{D0}(W/L)_1 \frac{(W/L)_3}{(W/L)_2} R_L \exp\left(\frac{mA \cos(\omega_0 t) + V_{GS1}}{\zeta V_T}\right) \quad (3)$$

where $m = R_2 / (R_1 + R_2)$, and $(W/L)_2$ and $(W/L)_3$ are the aspect ratios of M_2 and M_3 , respectively. Equation (3) can be approximated by the power series as

$$\begin{aligned} v_{BIPS} &\approx I_s \frac{(W/L)_3}{(W/L)_2} R_L \left(1 + \frac{mA \cos(\omega_0 t)}{\zeta V_T} + \frac{m^2 A^2 \cos^2(\omega_0 t)}{2 \zeta^2 V_T^2} \right) \\ &= V_s \left(1 + \frac{m^2 A^2}{4 \zeta^2 V_T^2} + \frac{mA \cos(\omega_0 t)}{\zeta V_T} - \frac{m^2 A^2 \cos(2\omega_0 t)}{4 \zeta^2 V_T^2} \right) \end{aligned} \quad (4)$$

where I_s and V_s represent $I_{D0}(W/L)_1 \exp(V_{GS1}/\zeta V_T)$ and $I_s R_L (W/L)_3 / (W/L)_2$, respectively. From (4), the dc component of v_{BIPS} is given by

$$V_{BIPS} = V_s \left(1 + \frac{m^2 A^2}{4 \zeta^2 V_T^2} \right). \quad (5)$$

The value of V_{BIPS} is extracted by passing the output voltage of the power sensor through a low-pass filter with a cut-off frequency lower than the input sinusoidal

Fig. 3. The schematic of the 5.2-GHz variable-gain RF amplifier as the DUT.

frequency. Therefore, the simplified relation between the output reading (V_{OUT}) and the amplitude of the sinusoidal wave (A) is expressed as

$$V_{OUT} - V_s = \frac{V_s m^2 A^2}{4 \zeta^2 V_T^2}. \quad (6)$$

As indicated in (6), the proposed built-in power sensors can be used to characterize the signal power at the input and output of the DUT, providing on-chip measurement of the forward gain and gain compression at radio frequencies.

3.2. Device under Test

In order to verify the BIST functionality provided by the built-in power sensors, a 5.2-GHz fully integrated variable-gain amplifier is employed as the DUT for demonstration. Figure 3 shows the complete schematic of the cascaded amplifier where MN_1 and MN_2 represent the first and second gain stage, respectively. The inductances L_G and L_{S1} are used to achieve the input matching while the output matching is provided by C_2 , C_3 and L_{D2} . In this design, the gain-controlled mechanism is achieved by adjusting the bias voltage at the gate of the second stage, resulting in a wide gain-tuning range without significant degradation in the input matching.

4. Experimental results and discussion

The RF BIST module integrated with a 5.2-GHz RF amplifier is designed and implemented in a standard 0.18- μm CMOS process. The die photo of the fabricated circuit is shown in Fig. 4 with a chip area of 0.83 $\times$ 1.08 mm².

Fig. 4. The die photograph of the fabricated circuit.

Fig. 5. The measured characteristics of the power sensors in calibration mode.

4.1. Built-in Power Sensors

Figure 5 shows the experimental results of the power sensors in the calibration mode, exhibiting good agreement with the theoretical derivation and the circuit simulation. Consuming a dc power less than 3.5 mW from a 1.8-V supply voltage, the power sensors has an input dynamic range better than 25 dB. In addition, the characteristics of the proposed power sensors are insensitive to the input frequency, allowing power measurement for wide-band RF systems. The performance of the built-in power sensors is summarized in Table I.

4.2. Built-in RF Test

To verify the BIST functionality, on-wafer probing was performed to characterize the S-parameters of the DUT in the vicinity of the center frequency for

Table I. Performance summary of the built-in power sensor.

Process	CMOS 0.18 μ m
Die Area	0.06 mm ²
Dynamic Range	>25 dB
Operating Frequency	5.2 GHz
Supply Voltage	1.8 V
Power Consumption	3.5 mW

comparison. The measured $|S_{21}|$ and the extracted forward gain from the BIST module are illustrated in Fig. 6. As indicated in Fig. 6, the proposed power sensors and the BIST module provide a satisfactory estimation of the forward gain for the RF amplifier operating in both gain modes, especially in the vicinity of the center frequency. In addition to the small-signal behavior extraction, the large-signal characteristics are also tested by measuring of the 1-dB compression point of the DUT. The results from the BIST module and from the test equipment are shown in Fig. 7. Table II summarizes the measured performance of the DUT along with the BIST extraction for comparison.

4.3. Error Analysis

The accuracy of the proposed test mechanism relies on the impedance matching at the input of the DUT. If the input impedance is not perfectly matched, an error will be introduced during the test. Assuming the DUT has an input reflection as $\Gamma = |\Gamma| \cdot \exp(j\phi)$, the output voltage of the power sensors can be rewritten as

$$V_{OUT} = V_s \left(1 + \frac{m^2 A^2}{4\zeta^2 V_T^2} + \frac{m^2 A^2 |\Gamma|}{2\zeta^2 V_T^2} \cos \phi \right). \quad (7)$$

Therefore, the gain error with the proposed BIST technique due to the input mismatch is approximated as

$$Error(dB) \approx 10 \log(1 + 2|\Gamma| \cos \phi)^{-1}. \quad (8)$$

According to the estimation from (8), an input return loss better than 17.7 dB is required for the DUT if a gain error within 1 dB is desirable for the test.

Another important contribution to the gain error results from the on-chip termination resistors due to the process variation. With a $\pm 10\%$ variation in the values of the on-chip resistors, a gain error of 1 dB is expected in the proposed BIST technique.

Table II. Performance summary of the DUT and BIST Results

	DUT mode	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	P_{in-1dB} (dBm)	NF (dB)
Test mode	High gain	12.2	-12.7	-18.0	-8.0	3.90
	Low gain	9.5	-12.6	-15.2	-3.0	4.10
Operation mode	High gain	12.1	-12.6	-17.8	-8.0	3.85
	Low gain	9.4	-12.4	-15.0	-3.0	4.05
BIST extraction	High gain	13.6	—	—	-7.6	—
	Low gain	10.9	—	—	-3.8	—

Fig. 6. The measured $|S_{21}|$ of the DUT and the extracted forward gain from the BIST module.

Fig. 7. The measured gain compression of the DUT and the extracted results from the BIST module.

5. Conclusion

This paper presents the architecture and experimental results of a proposed BIST technique for RF integrated circuits. With built-in power sensors, on-chip switches and terminations, the general-purpose BIST module provides power gain and gain compression measurement at multi-gigahertz frequencies. According to the experimental results, circuit parameters can be extracted with reasonable accuracy while maintaining negligible DUT performance degradation.

6. Acknowledgment

The authors would like to thank National Chip Implementation Center (CIC) and the Radio Frequency

Technology Center of National Nano Device Laboratories for chip fabrication and technical supports.

7. References

- [1] D. Lupea, U. Pursche and H.-J. Jentschel, "RF-BIST: loopback spectral signature analysis," *Design, Automation and Test in Europe Conference and Exhibition, 2003*, pp. 478-483.
- [2] M. Negreiros, L. Carro and A. A. Susin, "Low cost analogue testing of RF signal paths," *Design, Automation and Test in Europe Conference and Exhibition, 2004*, vol. 1, pp. 292-297.
- [3] D. J. Comer and D. T. Comer, "Using the weak inversion region to optimize input stage design of CMOS op amps," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 1, pp. 8-14, Jan. 2004