MODEL FOR PROPAGATION DELAY EVALUATION OF CMOS INVERTER INCLUDING INPUT SLOPE EFFECTS FOR TIMING VERIFICATION

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A propagation delay model of a short-channel CMOS inverter is reported, which considers input slope effects for timing verification by semi-empirical coefficients. Model calculations which demonstrate the source-drain series resistance effect show good agreement with SPICE MOS level 3 simulations.

Introduction: To date, the propagation delay modelling of an inverter has been the main problem in the field of timing verification of CMOS data paths. The reported works on this topic either focused on the switching response of a long-channel CMOS inverter [1-3] or neglected input slope effects on propagation delay evaluation [4]. Therefore, these models may not meet the strong demand of today's VLSI applications. For this purpose, we report a propagation delay model which concentrates on both short-channel device characteristics and input slope effects.

Model development: In this model derivation, the propagation delay which is defined as the time from a $0.5V_{DD}$ point of the input to a $0.5V_{DD}$ point of the output is used. We also focus on the discharging process of the loading capacitance, that is, the propagation delay T_{PHL} is the subject of this Letter. As pointed out in Reference 2, the switching response of a long-channel CMOS inverter triggered by an input voltage ramp can be described as follows:

$$T_{PHL} = T_{PHL}^{in} + T_{PHL}^s \quad (1)$$

where T_{PHL}^{in} is a contribution due to input slope effects and T_{PHL}^s is the step response of an inverter, which is sensitive to the DC behaviour of the device. In fact, as the MOS effective channel length scale down, T_{PHL} has to include second-order effects for the operation of short-channel devices. Based on our previous work [5] which presented a short-channel CMOS inverter fall time and rise time evaluation including both parasitic source-drain resistance and channel-length modulation for the first time in the literature, T_{PHL}^s can be obtained in a similar approach as given below:

$$\frac{I_{DS}}{C_{load}} \cdot T_{PHL}^s = 0.5V_{DD} - \frac{1}{L_{eq}} \int_{0.5V_{DD}}^{V_{DD}} L_{SAT} dV_{out} \quad (2)$$

where

$$\int_{0.5V_{DD}}^{V_{DD}} L_{SAT} dV_{out} = l^2 E_c (y \sinh y - \cosh y) \Big|_{y_2}^{y_1} + D \quad (3)$$

$$D = l \left(V_{DSAT} - V_{dsat}^* + \frac{q\eta N_A l^2}{e_s} \right) (y \cosh y - \sinh y) \Big|_{y_2}^{y_1} \quad (4)$$

$$Y_1 = \frac{L_{SAT}|_{V_{DS}=V_{DD}}}{l} \quad (5)$$

and

$$Y_2 = \frac{L_{SAT}|_{V_{DS}=0.5V_{DD}}}{l} \quad (6)$$

The above symbols either have their conventional meanings or have been defined in Reference 6. So far, the step response of an inverter which consists of short-channel MOS devices has been developed, which considers second-order effects such

as parasitic source-drain resistance and channel-length modulation as compared to others [1-4].

As for the contribution due to input slope effects, T_{PHL}^{in} is determined by a semi-empirical coefficient related to the input rise time, T_r :

$$T_{PHL}^{in} = A \cdot T_r \quad (7)$$

where A is a constant and can be obtained by fitting SPICE simulations. Although the semi-empirical model is simple, it will be demonstrated to be sufficiently accurate. Therefore, from eqns. 2 and 7, an explicit formulation of T_{PHL} is obtained.

Results: In Fig. 1a and b we present the results of our propagation delay model plotted as a function of the output capacitance with SPICE MOS level 3 simulations for input rise

Fig. 1 Propagation delay T_{PHL} plotted as function of output capacitance for input rise time of 0.0 and 1.0 ns

- (i) $R_{sd} = 60 \Omega$
- (ii) $R_{sd} = 0 \Omega$, $A = 0.1359$
- SPICE
- a 0.0 ns
- b 1.0 ns

time $T_r = 0.0$ and 1.0 ns. The aspect ratio of this inverter is the same as that of the example in Reference 5. As shown in these two Figures, the delay degradation effect caused by source-drain resistance shows good agreement with our model calculations. Note that the value of A is determined to be 0.1359.

Fig. 2a shows the propagation delay related to input slope effects for an output capacitance of 1.5 pF. Judging from this Figure, the propagation delay is approximately proportional to the input rise time. Therefore, it is acceptable to use a semi-empirical proportionality coefficient to include input slope effects on the propagation delay of a CMOS inverter. Furthermore, the unique features of our model are illustrated

in Fig. 2b, where the propagation delay is plotted against source-drain resistance for input rise times of 1.0 and 2.0 ns.

Fig. 2 Propagation delay T_{PHL} plotted as functions of input rise time and source-drain resistance ($A = 0.1359$)

- (i) $R_{sd} = 60 \Omega$
- (ii) $R_{sd} = 0 \Omega$
- SPICE
- a Input rise time
- b Source-drain resistance

Conclusions: A simple propagation delay model of a CMOS inverter suitable for timing verification has been described and verified by SPICE simulations. This model including input slope effects can be used in applications of short-channel MOSFET circuits such as propagation delay evaluation of a CMOS inverter chain or other data paths. To calculate these data-path delays, our previous work [5] can be incorporated which will generalise input voltage ramps to realistic input signal waveforms.

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HIGH PERFORMANCE AlGaAs/GaAs QUANTUM WELL MODFETs GROWN BY CHEMICAL BEAM EPITAXY

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Indexing terms: Field-effect transistors, Epitaxy and epitaxial growth

High quality modulation doped AlGaAs/GaAs QW structures were grown by chemical beam epitaxy using TEGa, TiBAI and AsH₃. MODFETs with gate lengths of 0.2 μ m fabricated from these heterostructures show extrinsic DC transconductances $g_{m,max} = 330$ mS/mm at drain currents $I_D = 145$ mA/mm. Maximum drain currents are $I_{D,max} = 275$ mA/mm. RF characterisation reveals extrinsic cutoff frequencies $f_T = 72$ GHz for the current gain, and $f_{max} = 144$ GHz for the unilateral power gain, respectively.

Introduction: Chemical beam epitaxy (CBE) of III-V semiconductors combines features of molecular beam epitaxy (MBE) and metal organic vapour phase epitaxy (MOVPE) by using gaseous precursors for both the group III and the group V elements at low growth pressures ($< 10^{-4}$ mbar). Especially, InP-based heterostructures for optoelectronic devices have been grown with comparable or even superior quality to related growth techniques, showing excellent interfaces, low residual doping and perfect homogeneity [1].

AlGaAs/GaAs heterostructures for high frequency devices, on the other hand, are deteriorated by the significant carbon incorporation in the AlGaAs due to the use of Al-alkyls with strong Al-C bonds. The use of tri-isobutylaluminium (TiBAI) reduces this carbon incorporation in the AlGaAs [2]. Heterostructures suitable for the fabrication of MODFETs with good performance can be grown [3-5].

We discuss the DC and RF properties of MODFETs with gate lengths of 0.2 μ m made of such AlGaAs/GaAs quantum well heterostructures grown by CBE using triethylgallium (TEGa), TiBAI and arsine (AsH₃). These high performance MODFETs compare well in every respect to MBE grown devices.

Device structure and fabrication: The layer sequence of the AlGaAs/GaAs QW heterostructure is shown in Fig. 1. It consists basically of a GaAs active layer with a thickness $L_a = 17$ nm separated by AlGaAs spacer layers (Al content: 25%; 2.3 nm and 5.5 nm) from the AlGaAs doping layers (Al content: 25%; with thickness 40 nm and 8 nm; $n = 2 \times 10^{18}$ cm⁻³) and capped by a highly doped GaAs contact layer (68 nm; $n = 3.4 \times 10^{18}$ cm⁻³). The structure was grown at a substrate temperature $T_s = 580^\circ$ C and a V/III ratio of 10 to minimise the carbon incorporation in the AlGaAs [2, 5]. The total flow rate of the group III precursors $F_{III} = 2$ sccm gave a growth rate $\alpha \approx 1$ μ m/h. N-type doping

GaAs	$n = 3.4 \times 10^{18}$ cm ⁻³	68 nm
Al _{0.25} Ga _{0.75} As	$n = 2.0 \times 10^{18}$ cm ⁻³	40 nm
Al _{0.25} Ga _{0.75} As	undoped	2.3 nm
GaAs-QW	undoped	17 nm
Al _{0.25} Ga _{0.75} As	undoped	5.5 nm
Al _{0.25} Ga _{0.75} As	$n = 2.0 \times 10^{18}$ cm ⁻³	8 nm
Al _{0.25} Ga _{0.75} As	undoped	90 nm
GaAs	undoped	500 nm
10 $\times$ SL Al _{0.25} Ga _{0.75} As	undoped	170 nm/170 nm
GaAs	undoped	500 nm
SI GaAs substrate		

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Fig. 1 Nominal layer sequence of CBE grown AlGaAs/GaAs QW MODFET structure