represented by $(x_1, x_2, \dots, x_7)$ and $(-x_1, x_2, \dots, x_7)$, $(x_1, -x_2, \dots, x_7)$, $\dots$, and $(x_1, x_2, \dots, -x_7)$, respectively. The solution can be verified by taking any of the above codewords as input to the network and see what results.

Note the connection complexity of this network is very low as compared to the number of memory patterns it stores and the error-correction capability it achieves. This is an example where a neural associative memory has storage capacity larger than its network size.

(ii) *Example 2:* In this example, six patterns the same as those in Reference 6 are used as memory patterns:

$$\begin{aligned} X_1 &= [-1, 1, -1, 1, 1, 1, -1, 1, 1, 1] \\ X_2 &= [1, 1, -1, -1, 1, -1, 1, -1, 1, 1] \\ X_3 &= [-1, 1, 1, 1, -1, -1, 1, -1, 1, -1] \\ X_4 &= [1, 1, -1, 1, -1, 1, -1, 1, 1, 1] \\ X_5 &= [1, -1, -1, -1, 1, 1, 1, -1, -1, -1] \\ X_6 &= [-1, -1, -1, 1, 1, -1, 1, 1, -1, 1] \end{aligned}$$

A network of 10 high-order perceptrons is used to store these six memories as well as their neighbouring patterns (in Hamming distance). Among $2^{10} = 1024$ possible inputs, there are 351 patterns that are equidistant from at least two memories. These patterns are classified as indistinguishable inputs and are indicated by an eleventh perceptron which outputs -1 if any of these inputs is detected and 1 otherwise. There are 512 product terms in each perceptron in the beginning. The algorithm learns the memory patterns and their neighbouring patterns in a short period whereas it takes ~ 4 h to learn to classify the indistinguishable inputs. The product terms for the first 10 perceptrons can further be reduced to 256 without affecting the training time very much, but a reduction in the number of terms in the 11th perceptron leads to an indefinite convergence time. This shows that it is easy to learn the patterns clustered in neighbouring regions and difficult to learn those scattered over the whole pattern space.

(iii) *Example 3:* In this example, the same memory patterns as those in the above example are stored but a distance measure different from the common Hamming distance is used. Let X be a vector of n bipolar elements and X^* be a reverse vector of X . For example, if $X = [1, 1, -1]$, then $X^* = [-1, 1, 1]$. Define an undirected Hamming (UH) distance between two vectors X and Y as

$$UH(X, Y) = \min[H(X, Y), H(X, Y^*)]$$

where $\min$ chooses the smaller one of its two arguments and $H(X, Y)$ is the Hamming distance between X and Y . (As an application example, the bar code used in consumer products might require this distance measure to allow it to be scanned in either direction.) In this simulation, there are now 410 equidistant inputs and a total of 608 neighbouring patterns for the six memories. Again 512 product terms appear in each perceptron and the convergence speed for the first 10 perceptrons is high, as can be expected. But the convergence time for the 11th perceptron is indefinite. The 11th perceptron has difficulty converging because it has to classify those indistinguishable patterns among all possible inputs.

Conclusion: We have shown that associative memories using high-order perceptrons achieve a set of desirable characteristics described in Reference 12: tolerance of noisy input versions of stored memories; high storage capacity; convergence to a stable state in a small number of iterations (in this feed-forward associative memory, only one forward pass is needed); existence of a passive or 'no decision' state which attracts indistinguishable inputs. Besides, it is possible to arbitrarily shape the basin of attraction of a memory pattern, under any metrics definition, by selecting a pattern to a 'neighbour' of that memory pattern and putting it on the list of the training set such that once the learning process converges, the neighbouring pattern is associated with its corresponding memory pattern. All these characteristics are

possible if the number of training patterns is within tractable bounds. Thus it can be considered as an alternative approach to constructing associative memories.

As we pointed out in the second Section, that high-order perceptrons can be reduced to multilayer perceptrons, it turns out that the above results can all be realised by existing implementation techniques that are applicable to multilayer perceptrons.

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BiCMOS DYNAMIC FULL ADDER CIRCUIT FOR HIGH-SPEED PARALLEL MULTIPLIERS

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Indexing terms: Large-scale integration, Adders, Multipliers

A BiCMOS dynamic full adder circuit for VLSI implementation of high-speed parallel multipliers using Wallace tree reduction architecture is presented. With the BiCMOS dynamic full adder circuit, an 8×8 multiplier designed based on a $2 \mu\text{m}$ BiCMOS technology shows a six times improvement in speed as compared to the CMOS static circuit. The speed advantage of using BiCMOS dynamic full adder circuits is even greater in 16×16 and 32×32 multipliers as a result of the BiCMOS large driving capability for realising the complex Wallace tree reduction architecture.

Introduction: High-speed multipliers are usually realised by parallel architectures [1], where the Wallace reduction structure [1] and carry look ahead circuits have been used to increase the speed. In a high-speed parallel multiplier using the Wallace tree reduction structure, the most important building cell is the full adder circuit. Although the CMOS dynamic technique [2] can provide a speed advantage over the static technique for implementing serial adders, it is suitable for realising the full adder circuit for parallel multipliers using the Wallace tree reduction structure due to race prob-

lems. Currently, BiCMOS static logic circuits have been proven to be helpful for realising high-speed VLSI systems [3]. In fact, BiCMOS dynamic logic circuits can also be very helpful for implementing high-speed digital systems. Recently, a BiCMOS dynamic carry look ahead circuit, which is built by cascading BiCMOS dynamic logic gates without race problems, has been reported [4]. In this Letter, a BiCMOS dynamic full adder circuit suitable for the VLSI implementation of parallel multipliers without race problems is described.

BiCMOS dynamic full-adder circuit: Fig. 1 shows the BiCMOS dynamic full adder circuit composed of cascading N

Fig. 1 BiCMOS dynamic full adder circuit

and P type BiCMOS dynamic logic cells [4]. The N type BiCMOS dynamic logic cell is used to implement the carry signal ($carry = AB + BC + AC$) and the P type cell is used to realise the sum signal [$sum = carry(A + B + C) + ABC$]. As in a dynamic BiCMOS digital circuit [4], during the precharge/predischage period, the clock signal (CK) is low and the outputs of the N and P type cells are charged to high and discharged to low, respectively. During the logic evaluation period, CK is high. If at least any two of the three inputs are high, the carry signal is pulled low by the pull-down bipolar transistor. The sum signal will then be pulled up only when all of the three signals $\bar{A}$, $\bar{B}$, $\bar{C}$ are low or when the carry signal is high and at least one of the three signals $\bar{A}$, $\bar{B}$, $\bar{C}$ is low. In the P type cell, three signals $\bar{A}$, $\bar{B}$, $\bar{C}$ are generated from the inputs A, B, C via static CMOS inverters, which are used to ensure that the arrival time of the signals $\bar{A}$, $\bar{B}$, $\bar{C}$ is later than that of the carry signal to the P type cell. Using the cascading N and P type BiCMOS dynamic logic cells, the full adder can be used in the high-speed parallel multiplier with Wallace reduction structure without race problems because signals are passed via a series of cascaded N type and P type logic cells. During the precharge/predischage period, the outputs of the N and P type logic cells are charged to high or discharged to low, respectively. Consequently, during the logic evaluation period, two prohibited states to any next stage logic circuit are naturally eliminated. As a result, race problems are successfully avoided.

Fig. 2 shows the propagation delay in the BiCMOS dynamic full adder against load capacitance. Also shown in Fig. 2 is the propagation delay in the CMOS static full adder. The propagation delay of the BiCMOS dynamic full adder is determined by the delay associated with the path from the P type cell input $\bar{A}$ via two pMOS transistors to the output. As shown in Fig. 2, for a wide range of load, the propagation delay of the BiCMOS dynamic full adder is about three times shorter as compared to that of the CMOS static order. The consistent higher switching speed advantage of the BiCMOS dynamic full adder is very important for realising parallel multipliers using the Wallace tree reduction architecture.

High-speed BiCMOS dynamic multiplier: High-speed parallel multipliers with Wallace tree reduction have been realised by CMOS static circuits [5] but they suffer from a speed penalty as a result of complex routing, long wiring, and irregular layout of the architecture [5]. Owing to race problems,

CMOS dynamic circuits are not suitable for building high-speed parallel multipliers with Wallace tree reduction structure. In fact, BiCMOS dynamic circuits are appropriate for

Fig. 2 Propagation delay of BiCMOS dynamic full adder and CMOS static full adder against output load capacitance

..... CMOS static 1 bit full adder
 — BiCMOS dynamic 1 bit full adder

implementing Wallace tree reduction architecture with complicated wiring. To show the versatility of the BiCMOS dynamic full adder circuit for constructing parallel multipliers with Wallace tree reduction structure, a test chip including two 8×8 parallel multipliers has been designed using a $2 \mu\text{m}$ BiCMOS technology. Fig. 3 shows the block diagram of the BiCMOS dynamic parallel multiplier using Wallace tree

Fig. 3 Block diagram of 8×8 parallel multiplier using Wallace tree reduction architecture with BiCMOS dynamic full adders and carry look ahead circuit

reduction architecture with BiCMOS dynamic full adders and the BiCMOS carry look ahead circuit [4]. Fig. 4 shows the layout of the BiCMOS dynamic and CMOS static multipliers. As shown in Fig. 4, the BiCMOS dynamic multiplier occupies an area of $2908 \times 3160 \mu\text{m}^2$ and the CMOS multiplier has an area of $2054 \times 2580 \mu\text{m}^2$. The die area of the BiCMOS dynamic multiplier is 73% larger as a result of a large portion of the space being allocated for the complex routing, long wiring, and irregular layout for realising the Wallace tree reduction architecture, although the BiCMOS dynamic full adder occupies a much smaller area as compared to the CMOS adder. Fig. 5 shows the calculated propagation delay against bit number of a parallel multiplier using the BiCMOS dynamic and CMOS static circuits. In a CMOS static multiplier without Wallace tree reduction structure and carry look ahead circuit, the propagation delay increases linearly as the bit number increments. On the other hand, the propagation

delay in a BiCMOS dynamic multiplier with Wallace tree reduction structure and carry look ahead circuit is relatively insensitive to its size. For the 8×8 multiplier, the BiCMOS

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Fig. 4 Layout of 8×8 parallel BiCMOS dynamic and CMOS static multipliers

Fig. 5 Speed performance of CMOS static and BiCMOS dynamic full multipliers against bit number

+ CMOS static
★ BiCMOS dynamic

dynamic multiplier has a 5.7 times speed advantage over the CMOS static one. For the 32×32 configuration, the speed enhancement is 11.6 times. In spite of the 73% larger layout area for complex wiring, the BiCMOS dynamic multiplier still provides very attractive speed performance as a result of the intrinsic excellent property of BiCMOS in driving a large load.

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SINGLE-POLARISATION FIBRE AMPLIFIER

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Indexing terms: Optical fibres, Amplifiers, Lasers

A novel single-polarisation fibre amplifier design is presented. The use of a Faraday mirror in a double-pass design yields optical gain with high efficiency, without spatial hole burning and independent of gain-fibre birefringence. An amplifier, tunable polarised laser, and a high-power polarised superfluorescent source are demonstrated.

Introduction: Single-polarisation fibre amplifiers (SPFAs) are needed for numerous fibre-optic applications. In single-frequency ring lasers and passively mode-locked fibre lasers, an SPFA is required to eliminate polarisation-mode competition [1] and dispersion [2], respectively. Single-polarisation (SP) or polarisation maintaining (PM) optical fibre obviates the need for polarisation insensitive receivers in coherent transmission systems [3] and overcomes polarisation dispersion penalties [4] in long haul, high bit rate fibre systems. Even if non-PM transmission systems are used, SP sources are still required for external modulators, fibre optic gyros, and interferometric sensors.

Highly birefringent [1] and SP [5] Er-doped fibres have been demonstrated as SPFAs. However, both require rather exotic noncommercial fibre, which requires radially-asymmetric fabrication, may limit design flexibility, and increases costs. We present a new efficient SPFA configuration that can use any singlemode dual-polarisation fibre with gain; the design is independent of both inherent and varying birefringence.

Basic design: The SPFA basic configuration is shown in Fig. 1a. An SP input signal from a PM fibre connected to port 1 is injected through a polarising beam splitter (PBS) into a standard non-PM fibre amplifier. After the signal has made a single pass through the amplifier it is reflected by a Faraday rotator mirror (FRM). The FRM reflects the light in the orthogonal polarisation state, regardless of the incident state. The light then makes a second pass orthogonally through the amplifier. On reaching the PBS, the light is in a linear polarisation state and is reflected into a second PM fibre connected to port 2. Because the technology needed to construct a fibre pigtailed FRM is very similar to that for a fibre isolator, the FRM has already become a commercial fibre component. It should be noted that any mechanism that exchanges the axes of polarisation on reflection will accomplish the same purpose as the FRM, and an alternative using a PBS and a length of PM fibre has been reported [6].

There are several consequences of the design that are particularly advantageous. The double-pass configuration allows higher gain, and more complete extraction (in the case of a superfluorescent source) [7, 8]. The counterpropagating light is in an orthogonal polarisation state at each point in the fibre so that there is no spatial hole burning and (reciprocal) birefringence is compensated for [9, 10]. All time dependent birefringence changes in the fibre will be compensated for provided that they are slow compared to the amplifier round-trip