We consider small unmodulated input signals of equal amplitude injected into the laser diode:

\[ I = I_0 + i_1 \exp(2nf_1 t) + \exp(2nf_2 t) \]

and let

\[ N = N_0 + N_1 + N_2 + \ldots \]

\[ P = P_0 + P_1 + P_2 + \ldots \]

where the quantities with subscripts 1, 2, \ldots represent different order perturbation quantities. Using eqns. 9–11 in eqns. 7 and 8, and with some approximations and fairly tedious procedures (as carried out by Lau and Yariv [4]), but retaining the effects induced by gain compression and spontaneous emission, we obtain the two-carrier third-order intermodulation-distortion-to-carrier ratio as

\[
\frac{IMD}{C} = \frac{m^2}{2g_{\text{dm}}(f_1, f_2)} \left[ \frac{\left( f_1^2 + f_2^2 + \frac{\beta T_p N_0}{2} \right) \left( f_1^2 + f_2^2 + \frac{\beta T_p N_0}{2} \right)}{r^2} \right]^2
+ \left( \frac{f_1^2 + f_2^2 + \frac{\beta T_p N_0}{2}}{4f_1 r_1} \right)^2 \left( \frac{1}{4f_2 r_2} + \frac{\beta T_p N_0}{2r_2 P_0} + \frac{1}{4f_1 r_1} \right)
\times \left( 2f_1 r_1 + 3 \frac{2nf_2}{6n_f} \right) \left( f_1^2 + f_2^2 + \frac{\beta T_p N_0}{2} \right)^2
\times (f_1^2 + f_2^2 + \frac{\beta T_p N_0}{2})^2
+ f_1^2 \left( \frac{f_1^2 + f_2^2 + \frac{\beta T_p N_0}{2}}{2f_1 r_1} \right) \left( f_1^2 + f_2^2 + \frac{\beta T_p N_0}{2} \right)^2
\times (f_1^2 + f_2^2 + \frac{\beta T_p N_0}{2})^2
\]

It can be shown that \( g_2(f) \) of eqn. 13 has the same form as \( g_1(f) \) of eqn. 4, i.e. the Helms equation, with certain manipulations. Combining the Iannoone and Darci's and the Helms formulas, our formula has some extra terms involving \( \beta \) and \( \varepsilon \). Usually, spontaneous effects can be ignored, but we retain the terms related to \( \varepsilon \) because it becomes important. When the number of subcarriers is large, such as in SCM optical communication systems, the laser is biased far away from the threshold, the terms related to \( \beta \) may be ignored, and eqn. 12 simplifies to eqn. 5.

Conclusions: In this Letter, we have modified the formula for two-carrier third-order intermodulation distortion induced by semiconductor laser diodes. When compared with previous results, our formula is more accurate and has an extended range of applications.

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**References**


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**CHARGE-BASED CURRENT MODEL FOR CMOS GATES**

J. H. Wang, J. T. Fan and W. S. Feng

**Indexing terms:** CMOS integrated circuits, Logic gates, Semiconductor devices models

A charge-based current model is introduced for the first time, which includes the current waveform induced by non-active events. Time-domain current waveforms can be obtained and the results show good agreement with SPICE. Three error values, DC, Max. J, and Max. T, differ by no more than 10% from SPICE.

**Introduction:** Owing to the electrical characteristics of MOS transistors, many parasitic capacitors exist inside a CMOS gate, e.g. \( C_P, C_g \). There will thus be current flowing if the voltage drop across two terminals of the MOS transistor changes. The gate terminal of MOS transistors is in general the controlling terminal, so we assume that the current flow only when the inputs of this gate change, which means that the leakage currents are neglected. The current supplied by the \( V_{DD} \) bus consists of three components: differential gate capacitor current, charging current of the load capacitance, and short-circuit current. The first component will exist if the input changes state. This component is negative if the input increases, and is positive if the input decreases. The last two component exist only when the gate changes state. In previous studies [1-3], only the last components are considered.

**Model development:** We describe the current model by using a circuit as an example, which is shown in Fig. 1. Let the input

\[ B \]

\[ V_{DD} \]

\[ I_{12} \]

\[ V_V \]

\[ I_{13} \]

\[ I_{12} \]

\[ I_{23} \]

The current of this two-input NOR gate will be connected to \( V_{DD} \), so the NOR gate will not change state, regardless of the state in which the other input \( A \) is. If the primary input of the circuit increases from 0 to 5 V, then the output of the first inverter will decrease. As a result, the second inverter will change state, meanwhile the NOR gate will remain unchanged. There are five currents drawn from the \( V_{DD} \) bus, shown in this Figure. Therefore the total current \( I_{total} \) drawn from the \( V_{DD} \) bus is

\[ I_{total} = I_1 + I_2 + I_3 \]

(1)

where \( I_1 = I_{11} + I_{13} \), and \( I_2 = I_{12} + I_{13} + I_{23} \). Notice the negative part of \( I_1 \). Each current waveform can be represented as a triangle with four parameters \( (\tau_1, \tau_2, \tau_3, \phi) \). \( Q \) is the total charge transferred to/from the \( V_{DD} \) bus and is equal to the area of this triangle. These three time parameters are the times when the current waveform starts, ends, and reaches its peak value.
(i) **Differential capacitor current:** The charging flow to/from \( V_{DD} \) across the gate capacitance is calculated as \( Q = \int C \, dv. \) If the source of the MOS transistor is connected to \( V_{DD} \), e.g. \( M_1 \), the capacitance is \( C_{M1} \). If the source is not connected to \( V_{DD} \) directly, e.g. \( M_2 \), then the capacitance is either \( C_{M2} \) if there is a conducting path connecting the source of this MOS to \( V_{DD} \) or \( C_{M1} \) if there is no conducting path to \( V_{DD} \). \( T_1 \) and \( T_2 \) are the times at which the input signal begins and ends, respectively. Because the voltage is approximated as a ramp, \( T_1 \) is set as the time at which the voltage is \( \pm 2.5 \) V.

(ii) **Charging current:** The total charge transferred to the load capacitor is \( Q = V_{DD} \cdot C_{L} \). The charge can be calculated as \( Q = \sum_{i} C_{i} \cdot \Delta v_{i} \), where \( \Delta v_{i} \) is the voltage swing of the glitch. The accuracy of the current waveform calculation is strongly coupled with the voltage swing of the glitch.

(iii) **Short-circuit current:** The analytical solution of this current can be obtained only when the gate is a CMOS inverter gate under certain assumptions. Therefore the total current must be measured using SPICE as

\[
Q = \frac{I_{MAX} - Q_{OFF} - Q_{ON}}{T_{OFF}}
\]

where \( Q_{OFF} \) and \( Q_{ON} \) are the charges due to the differential and charging currents, respectively. \( T_1 \) and \( T_2 \) are the times when the difference between the input and the output are 4 or \(-4\) V assuming that \( |V_{in}| = |V_{out}| = 1V \). \( T_2 \) is the time at which the input and the output voltage are equivalent.

We attempt to calculate each current component when processing every event, and then the total current can be obtained by summing these current components. Fig. 2 shows the current waveforms of the circuit shown in Fig. 1. Each current item, labelled in Fig. 1, is plotted as a triangle with the dashed line. \( I_1 \) and \( I_2 \) are obtained by summing these triangles. Only \( I_1 \) and \( I_2 \) are plotted, because \( I_3 \) is equal to \( I_{MAX} \). The solid lines are the results obtained by using SPICE.

Glitch: The accuracy of the current simulation depends strongly on the voltage waveforms. A glitch may occur when two adjacent events are so close that the second event occurs before the first event ends. Glitches may draw significant amounts of current and should not be neglected. When calculating the current waveform resulting from the first event, we assume that this event can reach its final state, so that the whole current waveform can be obtained. However, because the second event occurs before the first event ends, the current waveform is cut at the time at which the second event occurs. We approximate the current waveform resulting from the second event according to the peak ratio \( V_{2}/V_{DD} \), where \( V_2 \) is the voltage swing of the glitch.

**Results and conclusions:** This model has been tested extensively for basic modules such as counters, decoders, adders and ALUs. Fig. 3 shows the current waveform comparison of an SN7483 adder with the SPICE result. The CPU time comparisons are summarised in Table 1. The CPU time consists of the length of time the timing simulator BTS was used and that the current calculation was carried out. Because BTS considers the efforts of the internal charges, the simulator is not as fast as other timing insulators, but the waveforms it obtains are more accurate. This is very important because the accuracy of the current waveform calculation is strongly coupled to that of the timing information. Three error values, \( DC \), \( Max-I \), and \( Max-T \), are also listed. The DC error is the relative error regarding the average current \( I_{AVE} \) and \( l_{MAX} \). \( Max-I \) is the relative error regarding the value of the peak current \( l_{MAX} \). \( Max-T \) is the absolute error regarding the time at which peak current occurs. The results are accurate.

A current model is presented which can be used to generate the time-domain transient current waveforms in the power bus lines. The simulated waveforms in general do not differ by more than 10% from those simulated by SPICE. Its speed is \( 10^{3} \) times faster than that of SPICE for circuits with hundreds of transistors, and the speed ratio is expected to be even more significant for larger-scale circuits. At the cost of smaller speed ratio, the results are more accurate, especially the times at which peak current occurs.

**Table 1** COMPARISONS BETWEEN BTS AND SPICE 3

<table>
<thead>
<tr>
<th>Circuit</th>
<th>DC</th>
<th>Max-I</th>
<th>Max-T</th>
<th>BTS</th>
<th>SPICE</th>
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<tr>
<td>%</td>
<td>S</td>
<td></td>
<td></td>
<td>s</td>
<td>S</td>
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<td>74381</td>
<td>0-56</td>
<td>8-52</td>
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<td>1483</td>
<td>1478-68</td>
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<tr>
<td>7483</td>
<td>1-71</td>
<td>-7-15</td>
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<td>282-37</td>
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<tr>
<td>74147</td>
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<td>-8-76</td>
<td>-9.04 \times 10^{-10}</td>
<td>1-107</td>
<td>121-55</td>
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<tr>
<td>INV \times 100</td>
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<td>7-45</td>
<td>-4.24 \times 10^{-12}</td>
<td>0-700</td>
<td>100-7</td>
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<tr>
<td>74381 \times 16</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>26-32</td>
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</table>

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**References**

Sensitivity of 0.1 μm MOSFETs to Manufacturing Fluctuations

R. Sitte, S. Dimitrijev and H. B. Harrison

Indexing terms: Field effect transistors, Semiconductor device manufacture

A sensitivity analysis of 0·1 μm MOSFETs to manufacturing fluctuations has been carried out. The analysis reveals that the electrical parameter sensitivity in deep submicrometre devices differs from the currently produced micrometre size devices, making a revision of the validity of conventional semiconductor manufacturing heuristics for future technology mandatory.

Introduction: Several 0·1 μm MOSFETs have been designed and manufactured [1–4], providing reason to suspect that commercial production at this level may come to fruition in the future. While the published results claim improved device electrical characteristics, these device dimensions raise the important practical question as to whether it will be possible to reproduce these devices in larger batches. The development of equipment and techniques has been necessarily directed towards improvement of the processing steps, which proved to be crucial to the proper functioning of the device. This involves gaining better control over those process parameter fluctuations, to which the electrical device parameters are more sensitive. With the down-scaling however, some physical effects may become more pronounced and dominant over others, changing the effect of manufacturing fluctuations on the device. To improve our understanding of deep submicrometre devices, a study on the device parameter sensitivity to random fluctuations of processing parameters has been carried out for 0·1 μm MOSFETs.

Analysis and results: The analysis was based on typical fluctuations found in semiconductor manufacturing, as shown in Table 1. It consisted of varying a processing parameter by two standard deviations (2σ) on either side of the recipe value, and simulating the device characteristics using the MINIMOS [5] device simulator. The simulation accuracy for small devices was verified previously by comparison with experimental results*. The processing parameters used were gate oxide thickness and charge, gate length, substrate concentration; and for each of the implants (threshold voltage adjustment and source/drain extension) dose, energy, annealing temperature and time. The simulations were repeated for each of the following electrical device parameters: threshold voltage, transconductance and drain current at VD = 0 (off-current).

The resulting device parameter values were linearly fitted, and the normalised values of the slopes, which are the sensitivity rates, were multiplied by the fluctuation range of the corresponding process parameters, to obtain the effective device parameter fluctuation. As a reference for comparisons, the effective fluctuations of a typical 1·5 μm device were also determined, and plotted together with the results of the 0·1 μm device in the histograms, which are shown in Fig. 1.

As can be seen from Fig. 1, the effective fluctuations of the device parameters, caused by the process parameter fluctuations, are larger in the deep submicrometre device in most of the cases. Undoubtedly, the fluctuations of the gate oxide thickness showed the largest influence on all three device parameters considered, producing four-times larger fluctuations of threshold voltage and transconductance in the deep submicrometre device, than in its micrometre sized counterpart.

The second most influencing process parameter is the channel length. Whereas the effect of the channel length fluctuations on the transconductance was similar in magnitude for both device sizes under scrutiny, its effect on threshold...


Table 1 Process Parameter Values Used in the Simulation

<table>
<thead>
<tr>
<th>Process parameter</th>
<th>Unit</th>
<th>Mean value</th>
<th>Standard deviation</th>
<th>Mean value</th>
<th>Standard deviation</th>
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<td>Channel length</td>
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<td>0.06</td>
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<td>Gate oxide thickness</td>
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<tr>
<td>Gate oxide charge</td>
<td>cm⁻² (× 10¹⁰)</td>
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<td>3.0</td>
<td>5.0</td>
<td>3.0</td>
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<tr>
<td>Substrate concentration</td>
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<td>1.0</td>
<td>0.1</td>
</tr>
<tr>
<td>Threshold voltage adjustment implant</td>
<td>Species</td>
<td>Dose</td>
<td>Energy</td>
<td>Annealing temperature</td>
<td>Annealing time</td>
</tr>
<tr>
<td>Boron</td>
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<td>0.011</td>
<td>50 5</td>
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<tr>
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<td>5</td>
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<td>1050</td>
<td>0.5</td>
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<td>2400</td>
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<td>1800</td>
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</tr>
<tr>
<td>Source and drain extension implant</td>
<td>Species</td>
<td>Dose</td>
<td>Energy</td>
<td>Annealing temperature</td>
<td>Annealing time</td>
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