24.7 A 63GHz VCO Using a Standard 0.25 μ m CMOS Process

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Millimeter-wave (MMW) VCO design is motivated by the ever-increasing frequency and bandwidth of data-communications. In the MMW domain, integrated VCOs are realized mainly using III-V compound devices or SiGe HBTs. In deep submicron CMOS technology oscillators at frequencies up to 51GHz are reported [1]-[2]. However, for frequencies higher than 30GHz, output power is low even though buffer amplifiers are used. Previous designs also utilized a 0.12 μ m CMOS process with copper interconnections and a low-k dielectric [1] or a modified 0.25 μ m CMOS with a high-resistivity substrate, thickened top metal and buried or epi layers [2]. This paper presents a push-push cross-coupled MMW CMOS VCO. It also serves to demonstrate the design feasibility for an oscillator whose output frequency is higher than the device $f_{\max}$. Verification of the device model and EM-simulation are included. This VCO achieves a measured output power of -4dBm, a tuning range of 2.5GHz, and a phase noise of -85 dBc/Hz at 1MHz offset without an output amplifier in a commercial 0.25 μ m CMOS process.

The commercial 0.25 μ m 1P5M CMOS process provides a single poly layer for the MOS gates and five aluminium metal layers for interconnection. The substrate conductivity is approximately 10S/m. The active devices have an f_T of 30GHz and an $f_{\max}$ of 44GHz at a 1.5V drain bias. MIM capacitors of 1fF/ μ m² are developed using oxide inter-metal dielectric. Two types of polysilicon resistors with several Ω s/ $\square$ and k Ω s/ $\square$ are provided with individual doses of ion-implantation.

To achieve high frequency operation, high output power and good phase noise simultaneously, the push-push cross-coupled oscillator topology in Fig. 24.7.1 is proposed. The push-push oscillator approach evolved to push oscillation frequency beyond the device $f_{\max}$. The core part is a cross-coupled LC-tank VCO, as shown in Fig. 24.7.2, with each NMOS of 16 fingers and total gate width of 64 μ m. The supply current is fed through the $\lambda/4$ -line to the VCO core and the supply voltage also serves as the coarse-tuning voltage (V_{coarse}) to broaden the tuning range. The cross-coupled LC-tank VCO oscillates at its fundamental frequency (f_0) and also generates the second harmonic frequency ($2f_0$). The fundamental frequency is cancelled and acts as a virtual ground at the output node. In the design of a push-push VCO, suppression of even-mode oscillations is crucial. Once an even mode oscillation occurs, unwanted fundamental signals add up in phase and degrade the quality of the desired signal. The combined 63GHz output signal is extracted through a blocking capacitor to the 50 Ω load in the middle of the resonant inductance. For phase noise consideration, the current source is removed from the cross-coupled pair [3]. The fine-tuning frequency is determined by the bias of varactors from the node V_{fine} . The NMOS varactors are laid out as a multi-finger structure to enhance the Q-factor.

One primary source of phase noise source lies in the low Q of the resonant inductor in the LC-tank [4]. The degradation of Q at high frequency is due mainly to the high loss substrate in CMOS. Coplanar waveguide (CPW) and asymmetrical coplanar strip (ACPS) [5] are used in the design to reduce the substrate loss. The $\lambda/4$ -line is implemented with CPW and the interconnection for the RF signals. To further reduce the metal loss, the parallel shunt connection of metal 4 and 5 is used for CPW and ACPS. ACPS lines are used as inductors instead of the spiral inductors.

The underground passes are used to suppress the coupled-slot-line mode of the CPW by equalizing the potential of the ground plane. A full-wave EM simulation tool, Sonnet [6], is used to estimate the impedances of the CPW and ACPS over the frequency of interest. The modified MOSFET model for simulation is based on the BSIM3v3 SPICE model with some passive components added to account for the parasitic effects in the RF range. The parasitic effect of each interconnection is carefully calculated and included in the post-layout simulation.

This CMOS VCO is designed, fabricated and tested via on-wafer probing. The VCO starts to oscillate with a 3.6mA bias current from a 0.7V supply. Figure 24.7.3 shows the output frequency and output power as the supply voltage, serving as the coarse tuning voltage V_{coarse} is varied. The output frequency ranges from 62 to 66.5GHz. The maximum output power (P_{out}) is -4 dBm with 66mA with a 1.8V supply. The fundamental rejection (P_{2f}/P_1) is higher than 25 dB over the entire operating range. The fine-tuning characteristics of the frequency and output power variations with respect to the fine-tuning voltage (V_{fine}) are shown in Fig. 24.7.4. The fine-tuning range is about 1GHz with a 2V variation in fine-tuning voltage and the output power variation is less than 1 dB over the fine-tuning range. The measured spectrum is shown in Fig. 24.7.5. The difference between the measured frequency and that predicted by the small signal simulation is less than 1GHz (1.6%). Figure 24.7.6 is the photomicrograph of the fabricated chip with an area of 450 x 700 μ m². To the best of the author's knowledge, this work is the first push-push CMOS VCO with adequate output power in the MMW spectrum.

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Figure 24.7.1: Circuit schematic of the 63GHz VCO.

Figure 24.7.2: Structure of the VCO core.

Figure 24.7.3: Coarse-tuning characteristics.

Figure 24.7.4: Fine-tuning characteristics.

Figure 24.7.5: Spectrum of the 63GHz VCO.

Figure 24.7.6: Micrograph of the VCO.

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