5.1 An Auto-I/Q Calibrated CMOS Transceiver for 802.11g

Yong-Hsiang Hsieh¹, Wei-Yi Hu², Shin-Ming Lin², Chao-Liang Chen², Wen-Kai Li², Sao-Jie Chen¹, David-J Chen¹

¹National Taiwan University, Taipei, Taiwan

²MuChip, Hsin-Chu, Taiwan

The design and implementation of a low-cost IEEE 802.11g super-heterodyne RF front-end CMOS transceiver IC is reported in this paper. Through the use of auto-tuning mechanism at both transmitting and receiving ends, this transceiver IC is able to reduce the phase mismatch to within one degree and gain mismatch to within 0.1dB. Implemented in a 0.25 μ m CMOS process, this chip delivers a 5.1dB receiver cascade NF, and a 7dBm transmitter output gain compression.

The trend of present WLAN market is to increase the data rate. IEEE 802.11g WLAN standard supports data rates up to 54Mb/s using OFDM. To achieve this desired performance upper bound, it is crucial to deliver close match of I and Q signal paths in both the modulator and the demodulator. According to [1], to achieve this goal, baseband signal processing is required to calibrate the transceiver gain and phase mismatch. In this paper, it is demonstrated that such an effort can be accomplished in front-end with no more than 5% hardware overhead for the calibration circuitry.

The overall architecture of the transceiver is demonstrated in Fig. 5.1.1. At the front-end of the receiver (RX), a single-ended input, two-stage LNA is followed by an image-reject mixer and poly-phase filter. An active combiner is used to drive the off-chip SAW filter. From IF to baseband, a VGA is followed by a I and Q down-conversion mixer and a fifth-order Bessel filter. The VGA and filter are reused in both the receiving and transmitting paths to reduce the total transceiver die area. A continuous feedback DC-offset cancellation loop is designed to remove the output DC-offset voltage.

The TX path begins with an input buffer, followed by an LPF and shares the rest of its blocks with the RX path. A traditional Gilbert-cell double-balance mixer is designed to up-convert the baseband signal to IF frequency. The TX output power range is determined by the VGA gain that varies from -23dBm to 2dBm. The TX shares the same SAW filter with the receiver using an on-chip active combiner, which is designed to have a differential output impedance of 200 Ω . A differential-to-single-ended Gilbert-cell mixer drives a two-stage preamplifier.

An integer-N PLL operates with a 1MHz reference frequency, which is derived from the system reference frequency generated by an external 40MHz crystal oscillator. Three additional capacitor arrays in parallel to the tank circuit are used to tune the RF VCO frequency up to 280MHz. The calibration of the center frequency is performed when the channel changes. The RF and IF VCOs have phase noises of -116dBc/Hz and -120dBc/Hz, respectively, at 1MHz offset.

Before the I/Q gain mismatch calibration in the modulator, a DC-offset cancellation process needs to be performed. From Fig. 5.1.1, a switch SW1 on both the I and Q paths switches the TX input buffer input from the baseband to the vector generator, and a test vector (0,0) is applied to the modulator. A peak detector on the IF output converts the local leakage power level into a DC voltage that is amplified by a gain cell and is applied to a S/H comparator, as shown in Fig. 5.1.2. The auto-I/Q calibration control logic changes 1 bit in the TX input buffer DAC to create an extra DC signal on the I path. If the extra DC on DAC output has the same polarity with the DC offset, the local leakage power on the peak detector input becomes bigger; otherwise, it becomes smaller. The S/H comparator gives information on the polarity of DC offset occurred on the I path. A binary search is performed on

the output values of the comparator to find the proper control code for the DAC to create a compensated DC offset. The I/Q path DC-offset cancellation is performed in the following sequence: I path $\rightarrow$ Q path $\rightarrow$ I path and finally Q path. A 40dBc TX local leakage can be achieved under this algorithm.

The TX I/Q mismatch calibration process is modified from that of [2] to fit the proposed structure. Test vector (0, A) or (A, 0) is applied to the TX input on different time slots and, different signal power levels caused by the I/Q-path gain mismatch will appear on the modulator output. The comparator output will give the information on which path of the modulator has less gain. A 4b gain-controlled DAC is used in the TX input buffer to compensate for the gain mismatch; the gain of TX input buffer is increased step by step on the smaller gain path. When the S/H comparator changes the output polarity, the I/Q path gain becomes balanced with 0.1dB resolution and the gain calibration stops.

After gain mismatch calibration, the test vector is changed to (A, A) or (A, -A) in different time slots. Local quadrature mismatch causes different output power levels on the modulator output at these time slots. An extra delay is added on the local buffer to balance the delay. When the comparator output changes its polarity, the calibration loop stops. A one degree phase error can be achieved with the proposed architecture. Figure 5.1.4 shows the TX output spectrum and constellation performance after the gain and phase auto calibration.

For the receiver I/Q mismatch calibration, a single tone is generated and is applied to the receiver demodulator. After down-conversion, a 5MHz signal appears on the demodulator I/Q output. Figure 5.1.3 shows both the gain and the phase imbalance detection and comparison mechanisms. During the RX gain mismatch calibration, RSW1 changes the input from I path into Q path in different time slots. The comparator samples the I path signal and hold it to compare with the Q path signal. A compensated gain is added to the proper path after the auto-I/Q calibration control logic senses the comparator output. A sequential search is used here and calibration will stop until the comparator changes the output polarity. A 0.1dB gain imbalance is achieved after this auto tuning.

As shown in Fig. 5.1.1, the single tone is generated as follows. A 5MHz quadrature signal, obtained by dividing the 40MHz reference clock by 8, is applied to the up-conversion mixer through SW2. A 379MHz signal is created after up conversion with an SSB suppression of higher than 40dBc. Finally, this single tone will loop back to the receiver through SW3.

For the RX quadrature mismatch calibration, I/Q signals are mixed together as shown in Fig. 5.1.3. When there is I/Q mismatch, a DC signal appears at the output of this mixer. The S/H comparator compares the DC operating point at the output of the gain buffer output with the DC level obtained after the mixing of the I/Q signals. The logic output of the comparator gives information on which path of the quadrature local signals shall add an extra delay to compensate the quadrature mismatch. An extra delay is implemented by the delay cell after the quadrature generator. A 1 degree quadrature mismatch is achieved after auto tuning.

The IC is fabricated in a 0.25 μ m 1P5M CMOS. The 3 μ m $\times$ 3.4 μ m die is housed in a 48-pin QFN package. Only 5% extra die area is needed for the auto-I/Q calibration circuit. The measurement results are summarized in Fig. 5.1.5. The die micrograph is shown in Fig. 5.1.6.

References:

- [1] K. Vavelidis et al., "A Dual-Band 5.15-5.35 GHz, 2.4-2.5 GHz 0.25 μ m CMOS Transceiver for 802.11 a/b/g Wireless LAN," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1180-1184, July, 2004.
- [2] M. Fualkner et al., "Automatic Adjustment of Quadrature Modulators," *IEEE Electronics Letters*, vol. 27, no. 3, pp. 214-216, Jan., 1991.

Figure 5.1.1: Transceiver diagram.

Figure 5.1.2: The architecture of TX detector and comparator.

Figure 5.1.3: The architecture of RX detector and comparator.

Data Rate	54Mbps
EVM	3.2%
Power	-4dBm

Figure 5.1.4: Measured TX output spectrum and constellation.

Parameter	Measured result
Supply Voltage	2.7V ~ 3.3V
Supply Current RX mode	150mA
Tx mode	120mA
RX chain noise figure	5.1dB
RX chain max gain/min gain	85dB/12dB
RX Chain IIP3 (min gain)	0dBm
TX OP1dB	7dBm
TX gain control range	25dB
I/Q amplitude error (after calibration)	0.1dB
I/Q phase error (after calibration)	1degree
TX EVM @-4dBm output power	3.2%
LO integration noise (10KHz to 10MHz)	1.7degree
Technology	0.25um 1P5M CMOS
Die size	10.2mm ²

Figure 5.1.5: Performance summary.

Figure 5.1.6: Chip micrograph.