8.3 An 80GHz Travelling-Wave Amplifier in a 90nm CMOS Technology

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A six-stage travelling-wave amplifier (TWA) using a bulk 90nm CMOS technology is presented. By utilizing gate-line capacitive-division technique and low-loss coplanar waveguides (CPWs), the TWA exhibits a measured peak gain of 7.4dB at 28GHz and a gradual gain roll-off with a 3dB bandwidth of 80GHz while maintaining input and output return losses better than 8dB over the entire frequency band. A gain-bandwidth product (GBW) of 190GHz is achieved in this work.

A typical TWA is composed of gate and drain artificial transmission lines coupled by the transconductances of the gain cells. Due to the design considerations such as maximum available gain, bandwidth, stability and input-output isolation, cascode stages are adopted for the implementation of the gain cells. To achieve high power gain, the parameters of the common-source stages are chosen to maximize the transconductance while the common-gate stages are designed for high output resistances. In this TWA design, 90nm MOSFETs are used for the gain cells. Simulation results indicate that the cascode gain cells can provide signal amplification for frequencies up to 100GHz.

Though the advanced CMOS transistors exhibit satisfactory characteristics at high frequencies, the cut-off frequency and the attenuation of the artificial transmission lines impose restrictions on the TWA implementation. As can be observed from Fig. 8.3.1, the gate-line and the drain-line are loaded with common-source and common-gate stages, respectively. For a high-gain design, large transistor sizes are used for the common-source stages to achieve the required transconductance of the gain cells. The increasing input capacitance limits the cut-off frequency of the gate-line, compromising the achievable bandwidth of the TWAs. In order to alleviate the restrictions on the gain-bandwidth product, the gate-line capacitive-division technique is used to reduce the capacitive loading of the gain cells. The concept of the capacitive-division is illustrated in Fig. 8.3.2, where C_{div} is the gate-line division capacitor and M is the capacitive-division ratio. With series connection of C_{div} , the effective capacitive loading on the gate-line is reduced to MC_{gs} , resulting in a higher cut-off frequency of the gate-line. In addition, the capacitive-division also reduces the frequency-dependent losses at the TWA input. The number of the gain cells can be further increased to achieve better gain-bandwidth product of the TWA. Figure 8.3.3 shows the simulation results of the TWA with various capacitive-division ratios. It is obvious that the gain-bandwidth can be maximized by properly selecting the value of M .

Other than the attenuation due to the line loading, the substrate loss of a bulk CMOS technology plays an important role in the performance degradation at high frequencies. CPWs are used for the input and output transmission lines to minimize the substrate losses. The CPWs are implemented by the top metal to reduce possible penetration of EM field through the lossy silicon substrate while the underground passes are used to suppress the coupled-slotline mode of the CPW by equalizing the potential of the ground planes.

Figure 8.3.4 shows the schematic of the TWA design. In the design of the gain cells, a 5Ω damping resistor (R_{gx}) in the gate of common-gate transistor is employed to improve the amplifier stability. The gate and drain transmission lines are comprised of 95Ω CPW sections and 50Ω termination resistors (R_g and R_d). Most of the passive elements in the circuit, such as CPWs, T-junctions and bypass MIM capacitors are simulated by a full-wave EM simulator, Sonnet, to ensure the model accuracy within the operating bandwidth, as the previously reported designs at lower frequencies [1]. The proposed cascode CMOS TWA is fabricated in a 90nm 1P9M standard RF CMOS process.

On-wafer probing is performed on the CMOS TWA for the S-parameter measurement. A bias-T is used at the output to provide the dc bias of the cascode gain cells while coupling the signals to the measurement instrument. The TWA consumes 120mW dc power from a 2.4V supply. Figure 8.3.5 shows the measured gain (S21), return losses (S11 and S22) and reverse isolation (S12) from 5 to 100GHz. As can be seen, it achieves a peak gain of 7.4dB with a 3dB bandwidth of 80GHz. The return losses are better than 8dB for the entire frequency range. Figure 8.3.6 shows the micrograph of the fabricated circuit with a chip area of $1.2 \times 0.6 \text{mm}^2$ including the testing pads. The performance of the proposed TWA is summarized in Fig. 8.3.7 together with results from previously published data for comparison [2-6].

Acknowledgements:

This work is supported in part by NTU-TSMC Joint-Development Project and National Science Council (NSC 93-2752-E-002-001-PAE and NSC-92-2213-E-002-033). The authors would like to thank National Nano-Device Laboratory (NDL), Taiwan, ROC, for the chip testing.

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Figure 8.3.1: A simplified equivalent circuit of the TWA.

Figure 8.3.2: The gate-line capacitive-division technique.

Figure 8.3.3: The gain-bandwidth characteristics of the TWA with various capacitive-division ratio M .

Figure 8.3.4: Schematic of the six-stage travelling-wave amplifier.

Figure 8.3.5: The measured S-parameters of the TWA.

Figure 8.3.6: Micrograph of the fabricated TWA (Chip size: 1.2mm x 0.6mm).

Continued on Page 590

Process	BW (GHz)	Gain (dB)	GBP (GHz)	S11/S22 (dB)	VDD (V)	P _{DC} (mW)	Chip Size (mm ²)	Ref.
0.1μm InP HEMT	180	5	320	-	-	-	2.2 x 1.0	[2]
SiGe HBT	81	13	360	<-16	5.5	495	1.3 x 1.7	[3]
0.12μm SOI	90	11	320	<-7/<-5	2.5	210	1.8 x 0.7	[4]
0.18μm CMOS	22	7.3	51	<-8/<-9	1.3	52	1.0 x 0.9	[1]
0.18μm CMOS	27	6	50	<-10	3.3	68	1.8 x 0.9	[5]
0.18μm CMOS	39	4	60	<-10	-	140	1.1 x 3.0	[6]
0.09μm CMOS	80	7.4	190	<-10/<-8	2.4	120	1.2 x 0.6	This work

Figure 8.3.7: Comparison of state-of-the-art TWAs.