24.1 A 1.2V 6.7mW Impulse-Radio UWB Baseband Transceiver

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Ultra-wideband (UWB) communication is a new wireless technology that transmits data over a wide bandwidth for low-power and short-range communication. Of the different proposals for UWB, impulse-radio based technology uses nano-second baseband pulses to achieve spread spectrum transmission [1]. Impulse transmission eliminates the need for up/down converters and frequency recovery loops in communication systems. The simple transceiver structure of impulse-radio UWB technology makes possible a low-cost and low-power solution. Furthermore, the fine timing resolution provided by very short pulses gives rise to accurate positioning capability. In view of the above, impulse-radio UWB has been selected as a potential candidate for the IEEE 802.15.4a wireless personal-area network standard [2]. This work focuses on the implementation of a low-power and low-complexity low-band impulse-radio UWB baseband transceiver.

Figure 24.1.1 shows the block diagram of the impulse-radio UWB communication system. The analog front-end includes a pulse generator, an LNA, a wideband amplifier, and a 32-phase interleaved ADC. In addition, a timing generator generates the 32-phase clock signals for the ADC. Since power and die area are the most critical issues, hardware simplicity is taken into account early in the design stage. A physical-layer packet format made up of regular preamble, coded preamble, and data symbols (see Fig 24.1.1) is proposed to facilitate receiver design. A direct-sequence spread spectrum (DSSS) technique is adopted to combat the narrowband interferences and noise in the low signal-to-interference-and-noise ratio (SINR) environments in which the proposed UWB system is supposed to work. The number of pulses transmitted to carry one bit of information, called the spreading factor, ranges from 1 to 1024. The regular preamble is composed of a sequence of pulses with alternating signs and it is intended to facilitate pulse position detection at the receiver. After the regular preamble, four coded preamble symbols (using the length-1024 Golay code) are transmitted. Of the four coded preamble symbols, the first three symbols are of the same polarity while the last symbol is sent with reversed polarity to indicate the end of the preambles. This preamble arrangement and packet format saves hardware resources and permits a more sophisticated synchronization mechanism than the solution in [3].

The block diagram of the proposed baseband transceiver chip is shown in Fig. 24.1.2. The transmitter generates regular preamble, coded preamble and data symbols in a packet for the pulse generator. At the receiving end, a 32-phase parallel interleaved ADC provides 32 1b interleaved signals at a 2GHz sampling rate. Note that the pulse repetition period is 16ns so there are 32 samples in one pulse repetition period. A bank of correlators and a peak searcher find the exact pulse position when the regular preamble is being received. During the coded preamble stage, a Golay code matched filter and a symbol boundary detector work together to search for the symbol boundary. Finally, a data recovery block recovers the data using a correlator. In addition, the receiver includes an early-late timing tracking loop that can overcome the timing offset between the receiver clock and the received signal.

Several design considerations exploit the nature of the low-SINR channel and high spreading factor of the UWB system to reduce the circuit complexity and power consumption. For instance, the resolution of the input ADC is set to one bit, which not only saves

power consumption but also greatly simplifies the correlator structure. Instead of using 8-tap correlators that cover the whole pulse duration, using one-tap correlators saves a total of 192 adders at the cost of some degradation in SNR. The block diagram of the correlator bank is shown in Fig. 24.1.3. Since all 32 correlator outputs are scanned out of the correlator bank serially, only one absolute value block is needed. Despite the fact that its auto-correlation is less than ideal, the Golay sequence is chosen as the spreading code instead of the conventional maximal-length sequence because of its low-complexity matched filter structure. Two other advantages of the Golay code matched filter are its ease of pipelining and allowance for different code lengths (Fig. 24.1.3). The matched filter is capable of processing code lengths from 2^{10} , 2^8 , down to 2^0 . Further analysis reduces the word lengths of the delay lines and 960 bits of memory are saved without any degradation in performance.

The baseband transceiver integrated 384k transistors in a $0.98 \times 1.07 \text{mm}^2$ core size using $0.18\mu\text{m}$ CMOS technology. A summary of the chip performance, the power consumption at 62.5MHz, and the maximum clock rates for different supply voltages are shown in Fig. 24.1.4. When the supply voltage changes from 1.8V to 1.2V, the core power dissipation (operating at 62.5MHz) ranges from 15.6mW to 6.7mW and the maximum clock rate runs from 163MHz down to 65MHz.

Figure 24.1.5 shows the measured (symbol) boundary detection probability and packet error rate (PER) versus the E_b/N_0 for the typical channel and a high-quality channel with root-mean square (RMS) delays of about 20ns and 10ns, respectively. The proposed baseband transceiver functions well above $E_b/N_0 = 22\text{dB}$, assuming an allowable PER of 10%. Link budget analysis shows that the link margin is more than 20dB when the system is operating at 61kbps transmission rate (1024 spreading factor) and 10m transmitter-receiver separation under the FCC regulation for UWB.

Figure 24.1.6 presents a comparison in complexity, die size, and power consumption of this IC and the work reported in [3]. The reduction in complexity for pulse-position detection is primarily due to our regular preamble design, which leads to enormous hardware simplification. The coded preamble in the packet format also makes the symbol boundary detection much easier and faster, requiring only a structured and low-complexity Golay code matched filter. Faster symbol synchronization in our design allows more coded preambles to be inserted in a packet, thus improving the packet detection probability. A clock gating technique that turns off the idle modules and delay registers is also adopted to reduce power consumption. In summary, the core size of this design is only 1/20 of that in [3] after process normalization, and the average power consumption is estimated to be less than 1/6 of that in [3] under similar conditions of data length in each transmission, supply voltage, operating frequency, and fabrication process. The chip microphotograph is shown in Fig. 24.1.7.

Acknowledgments:

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References:

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Figure 24.1.1: System block diagram and the proposed physical-layer packet format.

Figure 24.1.3: Block diagram of the correlator bank and Golay code matched filter.

Figure 24.1.5: Measured symbol boundary detection probability and PER performance of the baseband receiver IC.

Figure 24.1.2: Block diagrams of the baseband transmitter and receiver.

Figure 24.1.4: Power consumption and maximum clock rate at different supply voltages and chip summary.

Functionality	Hardware	[3]	This Work
Pulse position detection	Add/sub count	128x127	32x1
	Add/sub size	>5bit	12bit
Symbol boundary detection	Add/sub count	128x11	1x20
	Add/sub size	>12bit	2bit-11bit
	Acquisition time (pulse)	93x1023	8x1024
Implementation Result	Core area (mm ²)	~10 (0.13 μm)	~1 (0.18 μm)
	Power (normalized and estimated)	1	0.148

Figure 24.1.6: Comparison of complexity, die size, and power.

Figure 24.1.7: Chip microphotograph.