Fig. 7. Leakage current densities of stacked MIM capacitors as a function of the applied voltage.

resulting in space charge relaxation processes. The dielectric can also become a loss by dipolar relaxation of moving oxygen vacancies. Further work is on the way to determine the microscopic origin of the observed dielectric loss.

The leakage currents of single-layer Al_2O_3 and Pr_2O_3 MIM capacitors are shown in Fig. 5. Over the studied film thickness range, the leakage current of Pr_2O_3 is strongly affected by the film thickness, whereas the leakage mechanism of Al_2O_3 is weakly influenced. The current measurement in this range is limited by the sensitivity of the instrument. Because of the higher band gap of Al_2O_3 (~ 8.8 eV) [13], the leakage current density is lower than that of Pr_2O_3 . The estimated band gap of Pr_2O_3 is around 4.6 eV [14].

The observed leakage current characteristics of the stacked dielectrics are shown in Fig. 7. The dielectric stack of 4-nm Al_2O_3 /9-nm Pr_2O_3 /4-nm Al_2O_3 exhibits the lowest leakage current density of 5×10^{-9} A/cm² at 1 V. The increment of the Pr_2O_3 thickness leads to higher leakage current densities, which correspond to the loss tangent characteristics.

IV. CONCLUSION

The MIM capacitor with a dielectric stack composed of 4-nm Al_2O_3 /9-nm Pr_2O_3 /4-nm Al_2O_3 exhibits excellent electrical performances, such as high capacitance density, low dielectric loss, and excellent leakage current density. This laminated capacitor meets the requirements for passive MIM devices in RF applications. However, by increasing the Pr_2O_3 -film thickness, the loss tangent as well as the leakage current density rise.

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The Improvement of Polycrystalline Silicon TFTs Fabricated by Employing Periodic Metal Pads

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Abstract—Polysilicon films with regular-sized and large grains were fabricated by employing periodic metal (Cr–Al) pads as the heat sinks and with underlying silicon oxynitride (SiON) as the heat absorption layer. The poly-Si could grow to regular hexagonal grains after excimer laser annealing (ELA). The thin-film transistors (TFTs) fabricated by this method show uniform characteristics that are suitable for large-area applications. The TFT achieves a field-effect mobility of $270 \text{ cm}^2/\text{V} \cdot \text{s}$ and an ON-OFF current ratio exceeding 10^8 . It is found that the TFT with the smaller channel width and length results in a better subthreshold swing because it contains fewer grain boundaries and, thus, fewer defects. After comparing the performance of TFTs using either double-metal Cr–Al or single-metal Al photonic-crystal pads, it is found that the Cr could efficiently impede the diffusion of Al into Si during ELA.

Index Terms—Photonic crystal, polycrystalline silicon, thin-film transistor (TFT).

Manuscript received October 13, 2005; revised April 21, 2006. This work was supported by the National Science Council of Taiwan, R.O.C., under Contract NSC 93-2215-E-002-046. The review of this brief was arranged by Editor T. Skotnicki.

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Digital Object Identifier 10.1109/TED.2006.8778783

Fig. 1. Schematic diagram showing the structure used to fabricate regular and large-grain poly-Si by ELA. The periodic metal (Cr–Al) pads and SiON absorption layer were applied. (Color version available online at <http://ieeexplore.ieee.org>.)

(a)

(b)

Fig. 2. (a) Field emission (FE)-SEM and (b) AFM images of hexagonal poly-Si grains after ELA and Secco etching.

I. INTRODUCTION

Low-temperature poly-Si (LTPS) thin-film transistors (TFTs) fabricated by excimer laser annealing (ELA) have been widely applied in active matrix liquid-crystal displays (AMLCDs) [1] and active matrix organic light-emitting diodes (AMOLEDs) [2], [3]. The problem is that the uniformity of the poly-Si film could not be exactly controlled such that it requires a compensation design in the driving circuit of the AMLCD and AMOLED. The important issue about uniformity is the grain size distribution in the channel region. If the grain size is regular and large, the grain boundaries in the channel could be fixed and then the uniformity and mobility of TFT could be improved. Several

(a)

(b)

(c)

Fig. 3. TEM image of (a) bright-field view, (b) dark-field view, and (c) diffraction pattern from hexagonal poly-Si grains after ELA and Secco etching.

methods have been reported to improve the uniformity of the poly-Si film, such as sequential lateral solidification (SLS) [4], optical phase shift mask [5], grains controlled by floating structure [6], location control Si grain [7], and large-grain poly-Si (10 μm) TFTs fabricated by ELA through a thick SiON absorption layer [8].

In this brief, the regular- and large-grain poly-Si fabricated by employing periodic metal pads and underlying the SiON heat absorption layer is proposed. The poly-Si TFT fabricated by this method exhibits much better electrical performance than those fabricated by employing SiON heat absorption layer only and conventional poly-Si. Finally, it was found that the use of a double-metal structure (Cr–Al) in the photonic-crystal pads could efficiently decrease the leakage current of the TFT.

Fig. 4. Optical microscope (OM) image of the hexagonal poly-Si grain location inside the channel of the TFT ($W/L = 10/6$, $10/5$, and $8/4 \mu\text{m}/\mu\text{m}$). (Color version available online at <http://ieeexplore.ieee.org>.)

Fig. 5. Transfer curves of poly-Si TFTs with regular-grain poly-Si and different width-to-length ratios ($W/L = 10/6$, $10/5$, and $8/4 \mu\text{m}/\mu\text{m}$).

II. EXPERIMENTS

Fig. 1 shows the schematic diagram of this process. 500-nm SiON was first grown on the glass substrate with buffered oxide as the heat absorption layer by plasma-enhanced chemical vapor deposition (PECVD). Then, 10-nm silicon oxide (SiO_x) was deposited as the insulating layer. Moreover, 50-nm amorphous-silicon film was grown, and the hexagonal patterned-metal (Cr–Al, 25/300 nm) pads were deposited on top. The purpose of the metal pads is to reflect the laser light and create a heat sink. Then, the film was annealed by the excimer laser (KrF, duration time of 28 ns, $450 \text{ mJ}/\text{cm}^2$); this would melt the amorphous-silicon region without metal pads and the nucleated silicon crystal grows radically from the center of the metal (heat sink). They would touch each other at the middle of two metal pads and form the regular shaped poly-Si grain. Finally, the metallic (Cr–Al) pads were

TABLE I
COMPARISON OF TFT PERFORMANCE WITH REGULAR
POLY-Si AT DIFFERENT W/L RATIOS

W/L ($\mu\text{m}/\mu\text{m}$)	On/Off $V_D = 0.1 \text{ V}$	Mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	V_T (V)
10/6	2.7×10^6	156	5.8
10/5	2.3×10^6	171	5.9
8/4	2×10^8	270	6

Fig. 6. Comparison of transfer curves of TFTs with regular-grain poly-Si, using SiON absorption layer only, and using normal poly-Si.

removed by an etching solution. Finally, after depositing 120-nm oxide as the gate insulator and patterning the gate metal, the TFT is completed.

III. RESULTS AND DISCUSSION

Fig. 2(a) and (b) displays the scanning electron microscopy (SEM) and atomic force microscopy (AFM) images of the poly-Si film with regular grains, respectively. A hexagonal lattice with very clear boundaries were observed (radius of the pad $r = 0.75 \mu\text{m}$ and distance between two pads $a = 5 \mu\text{m}$) after ELA, removing the metal pads and Secco etching. This proves that the poly-Si grains are very uniform and form regular shape.

Transmission electron microscopy (TEM) was used to analyze the quality of the grains. Fig. 3(a)–(c) displays the bright-field view, dark-field view, and diffraction pattern of the hexagonal grain, respectively. Fig. 3(b) shows that grains grow radically from the edge of central amorphous Si and have the sub-grain inside. In addition, through the diffraction pattern of Fig. 3(c), the quality of the grain turns out to be better than that of poly-Si.

Fig. 4 shows the location of the regular grains inside the TFT channel with different channel-width-to-length ratios ($W/L = 10/6$, $10/5$, and $8/4 \mu\text{m}/\mu\text{m}$). The grain boundaries and central amorphous Si are observed clearly. Fig. 5 shows the transfer curves of TFTs with different W/L ratios. As shown, the TFT with smaller channel width and length results in a better subthreshold swing because it contains fewer grain boundaries and, thus, fewer defects. Table I lists the comparison of these three TFTs with different W/L ratios ($W/L = 10/6$, $10/5$, and $8/4$). The mobility of the TFT with $W/L = 8/4$ could reach $270 \text{ cm}^2/\text{V}\cdot\text{s}$, and the threshold voltage (V_T) is 6 V.

Fig. 6 shows the transfer curves of three poly-Si TFTs with regular grains, grains fabricated by using SiON absorption layer only,

TABLE II
COMPARISON OF TFT PERFORMANCE ($W/L = 8/4$) USING
DIFFERENT TECHNOLOGIES

Poly-Si	On/ Off $V_D = 0.1V$	Mobility ($cm^2/V \cdot sec$)	V_T (V)
Regular grain	2×10^8	270	6
Absorption layer only	10^7	20	6.2
Normal	10^6	11	6.5

Fig. 7. Comparison of the statistical percentage variations of the (a) threshold voltage V_T and (b) mobility (μ) of poly-Si TFTs with three different designs, i.e., regular-grain poly-Si, using SiON absorption layer only, and using normal poly-Si.

and conventional poly-Si by direct ELA. It is clear that the poly-Si TFT with regular grains exhibits the best subthreshold swing and its ON-OFF current ratio exceeds 10^8 . Table II lists the comparison of these three TFTs. The poly-Si TFT with regular grain exhibits the best electrical properties; its mobility is ten times higher than that with SiON absorption layer only ($20 \text{ cm}^2/V \cdot s$) and 30 times higher

Fig. 8. Transfer curves of poly-Si TFTs with regular grains fabricated by employing either Cr-Al or Al metal pads with bias $V_D = 0.1$ and 1 V .

than that with conventional poly-Si ($11 \text{ cm}^2/V \cdot s$). It proves that this process could significantly improve the device performance.

Fig. 7(a) and (b) displays the statistics about the percentage variations of the threshold voltage (V_T) and mobility (μ) of the three poly-Si TFTs ($W/L = 8/4 \text{ } \mu\text{m}/\mu\text{m}$) with regular grains, grains fabricated by using SiON absorption layer only, and conventional poly-Si by direct ELA, respectively. From Fig. 7(a) and (b), the poly-Si TFT with regular grains at the same location, such as $W/L = 8/4 \text{ } \mu\text{m}/\mu\text{m}$ in Fig. 4, could get the smallest variation among all TFTs. It indicates that the uniformity of the electrical performance could be improved substantially by this process.

In order to identify the residue in the grain, the energy dispersive X-ray analysis was applied to analyze the residue. The residue of Al in hexagonal grains fabricated without the Cr layer is about 2.57 at.%, and the background Al concentration in the glass substrate is about 2.39 at.%. The residue of Al in hexagonal grains fabricated with the Cr layer is close to the background, and we did not detect any residue of Cr. This could identify that the Cr layer could impede the diffusion of Al into the Si layer effectively. Fig. 8 shows the transfer curves of the poly-Si TFT with regular grains fabricated by employing either double-metal Cr-Al or single Al pads at $V_D = 0.1$ and 1 V . It also shows that the TFT ($W/L = 8/4$) fabricated by Cr-Al pads could attain lower leakage current than that fabricated by employing single Al pads. It means that the Cr could effectively impede the Al to alloy with Si and lower the leakage current.

IV. CONCLUSION

The regular-grain poly-Si has been fabricated successfully by employing periodic metal (Cr-Al) pads. The TFT with width-to-length ratio $W/L = 8/4$ exhibits the best performance, i.e., the ON-OFF current ratio exceeds 10^8 , achieving a mobility of $270 \text{ cm}^2/V \cdot s$, which is a substantially improved uniformity in electrical performance and is much better than those of the poly-Si TFTs fabricated using SiON absorption layer only or conventional poly-Si prepared by direct ELA.

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Asymmetry in Gate Capacitance–Voltage (C – V) Behavior of Ultrathin Metal Gate MOSFETs With HfO_2 Gate Dielectrics

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Abstract—Anomalous asymmetry (which here means “beyond that to be expected classically”) between accumulation and strong inversion was observed in the measured capacitance–voltage (C – V) curves of metal gate nMOSFETs with ~ 1 nm equivalent oxide thickness (EOT) HfO_2 layers and was analyzed and extrapolated to still smaller devices and to pMOS devices using self-consistent Poisson–Schrödinger simulations. The experimental devices were fabricated via atomic layer deposition (ALD) of HfO_2 on stress-relieved preoxide (SRPO), followed by tantalum carbon alloy metal gate deposition. Simulations suggest two underlining mechanisms for this anomalous asymmetry, namely 1) differing degrees of quantum mechanical carrier penetration into the dielectric associated with the differing electron and hole barriers and 2) differing degrees of quantum confinement within the substrate, which result from differing electron and hole bandstructures in the Si. Both mechanisms result in greater capacitance when the quantum-confined surface carriers are electrons than when they are holes. Simulations indicate that this effect can produce asymmetries between pMOS and nMOS devices under strong inversion for the same physical gate stack that will become increasingly important as the trend toward smaller devices and use of high- κ dielectrics continues: perhaps approximately 10% reduction in pMOS strong-inversion capacitance relative to that of nMOS devices for 0.5 nm EOT high- κ gate stacks.

Index Terms—Barrier penetration, gate capacitance, high- κ gate dielectrics, metal gates, quantum confinement.

Manuscript received April 7, 2006. This work was supported in part by the Texas Advanced Materials Research Center (Texas AMRC), Freescale Inc., the Micron Foundation, and the Texas Advanced Technology Program. The review of this brief was arranged by Editor S. Kimura.

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Digital Object Identifier 10.1109/TED.2006.878013

I. INTRODUCTION

The International Roadmap for Semiconductors (ITRS) [1] predicts/calls for continuing reductions in the equivalent oxide thickness (EOT) of MOS device gate dielectrics, with EOTs of ~ 0.4 – 0.5 nm expected for high-performance applications by 2016. High dielectric constant (high- κ) materials and metal gates are being developed to overcome detrimental gate leakage and polydepletion effects, respectively, as MOS devices are scaled down. However, as dielectric EOTs decrease, quantum mechanical effects become increasingly important for gate capacitance [2]–[3]. In this brief, experimentally observed “anomalous” (here essentially meaning “beyond that to be expected classically”) asymmetry in the capacitance–voltage (C – V) behavior between strong inversion is identified in metal gate HfO_2 nMOSFETs on (100) Si substrates. Then, through self-consistent Poisson–Schrödinger simulation, the physical mechanisms for anomalous asymmetry are identified, and the effects of these mechanisms are extrapolated to smaller devices and to pMOS devices. Results indicate that the experimentally observed anomalous asymmetry will also translate to a reduction in the strong inversion capacitance of pMOS devices as compared to nMOS devices with the same physical gate stack, which is a difference that increases with decreasing oxide thickness and use of high- κ gate stacks. First, however, we begin with discussion of the experimental and modeling approaches.

II. EXPERIMENTS AND MODELING

The device fabrication followed a standard CMOS process flow on bulk (100) Si until the atomic layer deposition (ALD) of HfO_2 . Wafers were deposited on stress-relieved preoxide (SRPO) formed by growing a relatively thick thermal oxide at high temperature (higher than the SiO_2 glass flow temperature) for stress relief, followed by an etch back to 10 Å using 700:1 HF [4]. The HfO_2 with various thicknesses was then deposited at 300 °C using ALD. The precursors are HfCl_4 and D_2O [5]. After a postdeposition anneal of the high- κ dielectric, a tantalum carbon alloy metal gate was deposited. A commercial CMOS process technology [6] with the source/drain annealed at 1000 °C was used to fabricate the metal gate/high- κ stack nMOSFETs on bulk Si.

The C – V measurements for each were performed at 100 kHz on arrays of 28 TaC/ HfO_2 /p-Si devices measuring 10 μm by 10 μm (length by width) for a total area of 2800 μm^2 per array. The gate leakage current density is rather low (< 20 A/cm 2) for these high- κ devices (the primary purpose of using high- κ dielectric) even for the thinnest EOT (1.02 nm) device. Therefore, the impact of the gate leakage current on the C – V measurements is minimal as demonstrated by the well-behaved C – V curves.

In the C – V simulation study, the Poisson and Schrödinger equations were solved self-consistently, allowing for wave function penetration into the gate dielectric. Effective-mass approximations (EMAs) were made for both electrons and holes in the Si substrate/body [7]. The interface normal effective masses used for the electrons are $0.92 m_e$ (where m_e is the free electron rest mass) and $0.19 m_e$ for the “longitudinal” and “transverse” valleys with degeneracies of 2 and 4, respectively, for a {100} surface orientation [7]; and $0.16 m_e$ for the light hole band and $0.49 m_e$ for the heavy hole band, respectively [8]. Although the use of the EMAs for holes lacks some precision, this approximation is sufficient to capture the essential physics. For modeling purposes (as a control, lacking definitive alternatives, particularly for the HfO_2 gate stack) EMAs also were made for both SiO_2 and HfO_2 , with the carrier tunneling effective masses taken to be $0.5 m_e$ in all cases. The band offsets used for the conduction band ΔE_C and valence band ΔE_V at the dielectric-Si interface were 3.15