Stability improvement of deuterated amorphous silicon thin-film transistors characterized by modified Schottky-contact gated-four-probe method

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A modified Schottky-contact gated-four-probe structure was applied to study the stability of the hydrogenated and deuterated amorphous silicon (*a*-Si:D) thin-film transistors under various bias conditions. It was found that after 10 V bias stress, the density of gap states generated in both the upper and lower part of the mobility gap of deuterated amorphous silicon is two to twenty times less than those of hydrogenated silicon. Besides, less density of states at the lower part of mobility gap of *a*-Si:D is generated after 20, -10, and -20 V bias stress. © 2003 American Vacuum Society. [DOI: 10.1116/1.1545752]

I. INTRODUCTION

Recently, the hydrogenated amorphous silicon (*a*-Si:H) thin-film transistors (TFTs) have been studied extensively since they have widespread applications such as liquid-crystal displays. One of the interesting stability issues in *a*-Si:H is using deuterium to replace hydrogen. Several reports^{1–7} suggest that replacing hydrogen with deuterium in amorphous silicon tends to slow the decay of photoconductivity. Recently, the hot electron degradation in a silicon metal–oxide–semiconductor field-effect transistor has also found to be greatly reduced by passivating the silicon–silicon dioxide interface using deuterium instead of hydrogen.⁸ Sugiyama *et al.*⁹ have demonstrated that a deuterated amorphous silicon (*a*-Si:D) solar cell is more stable than an *a*-Si:H one under normal operation. Besides, Wei *et al.*¹⁰ have demonstrated that the stability of an amorphous TFT is improved by using *a*-Si:D instead of *a*-Si:H as the active layer. Wei *et al.*¹¹ and Shih¹² have proposed the mechanism responsible for the improvement of the film stability. However, the distribution of defect states after bias stress is less clear. Chen *et al.*¹³ have proposed a gated-four-probe *a*-Si:H TFT structure which allows the determination of the intrinsic performance of an *a*-Si:H TFT without any influence from source and drain series resistances. Chiang *et al.*¹⁴ have demonstrated a Schottky-contact gated-four-probe *a*-Si:H TFT structure which can be used to study both electron and hole conduction characteristics before and after bias stress.

In this article, both *a*-Si:H and *a*-Si:D TFT's are prepared by using modified Schottky-contact gated-four-probe structure which provides a study of both electron and hole conduction characteristics before and after bias stress without influence from source and drain series resistances. In the modified Schottky-contact gated-four-probe TFT structure, both source and drain contacts consist of the ohmic and Schottky regions. When the device is operated in the accumulation mode (positive gate bias), the source and drain ohmic contact regions allow the electron current to pass through, but when operated in depletion mode (negative gate

bias), the hole current tends to flow through the Schottky contact regions. There are two additional probes placed between the source and drain electrodes to perceive the voltage difference along the active channel. The channels were made either of *a*-Si:H or *a*-Si:D, their current–voltage (*I*–*V*) characteristics were compared to find out the defect distribution after bias stress.

II. EXPERIMENT

Figure 1 shows the device structure of a modified Schottky-contact gated-four-probe *a*-Si:H(D) TFT. First, a 75 nm thick Cr was electron-beam evaporated on 7059 glass. After being patterned and wet etched, 300 nm thick undoped *a*-SiN_x:H or *a*-SiN_x:D layer was then deposited on Cr by plasma-enhanced chemical vapor deposition, followed by the 50 nm thick undoped *a*-Si:H or *a*-Si:D layer, finally, a 10 nm thick *a*-Si:H or *a*-Si:D layer doped with 5000 ppm PH₃ was deposited. The substrate temperature, rf power density, and chamber pressure during deposition were 250 °C, 0.11 W/cm², 0.45 Torr, respectively. The gas flow rates for *a*-SiN_x:H deposition were 1 (SiH₄) and 19 (NH₃) sccm, for *a*-SiN_x:D were 1 (SiD₄) and 19 (ND₃) sccm, for undoped *a*-Si:H layer were 2 (H₂) and 5 (SiH₄) sccm, for an undoped *a*-Si:D layer were 2 (D₂) and 5 (SiD₄) sccm, for *n*-type doped *a*-Si:H layer were 0.8 (H₂), 5 (SiH₄), and 1.2 (PH₃) sccm and for *n*-type doped *a*-Si:D layer deposition were 0.8 (D₂), 5 (SiD₄), and 1.2 (PH₃) sccm, respectively. The sample was then patterned and reactive ion etched, followed by the thermal evaporation of 200 nm thick Al(Si). Finally, the Al(Si) was patterned and wet etched to define the source, drain, and probe A and B regions. The active channel length (*L*) and space between probe A and B (*L'*) are 40 and 20 μm, respectively. The Schottky-contact region of the source, drain, and probes A and B are all 2.5 μm wide. There is an overlap of the 5 μm wide ohmic contact region between the source, drain, and gate electrodes.

The electrical characteristics of a Schottky-contact gated-four-probe *a*-Si:H(D) TFT was measured using HP 4156A. First, the *I*–*V* characteristics, transfer curves, and the device parameters, $G = I_{DS}/(V_A - V_B)$ and $V_{G\text{eff}} = V_G - (V_A + V_B)/2$,¹⁴ were measured before bias stressing. Second, dur-

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FIG. 1. Device structure of a modified Schottky-contact gated-four-probe *a*-Si:H(D) TFT.

ing bias stressing, constant gate voltage was applied to the TFT for 200 s. The source, drain, and probes A and B were all set to ground to assure a uniform vertical electrical-field distribution along the channel during bias stressing. Third, the bias stress was stopped, and the drain current and the voltages of the extra two terminals were measured at constant gate bias with different drain voltages. Fourth, the same bias stress condition and measurements were repeated up to 10 000 s.

III. THEORY

In the charge control model¹⁵ for an *a*-Si:H(D) TFT performance, the concentration of free carriers, n_f , induced in the conduction channel is given by

$$n_f = C_i [V_G - V_T - V_C(x)]/q, \quad (1)$$

where C_i is the geometrical capacitance of the gate insulator, V_G is the applied gate bias, V_T is the effective threshold voltage, $V_C(x)$ is the channel potential, and q is the electronic charge. The dependence of the charge in the depletion layer on the channel surface potential has been neglected in this approximation. Based on the gradual channel approximation, the drain current then can be expressed as

$$I_{DS} = C_i \mu_{FE} (dV_C(x)/dx) [V_G - V_T - V_C(x)] W, \quad (2)$$

where W is the channel width and μ_{FE} is the field-effect mobility. Equation (2) can be rewritten as

$$I_{DS} dx = (C_i \mu_{FE} W) [V_G - V_T - V_C(x)] dV_C(x). \quad (3)$$

A modified Schottky-contact gated-four-probe structure shown in Fig. 1 was used to exclude the effect of source/drain series resistances during I - V measurement. One should notice that there are two additional narrow metals which form Schottky barrier electrodes (probes A and B) placed between the source and drain contacts to probe the potential at $X = X_A$ and $X = X_B$, respectively. Since no current flows through probes A and B during the I - V measurement, no voltage develops across the metal contacts A and B.

Thus, what we measure is the real bulk potential at $X = X_A$ and $X = X_B$ without distortion. Besides, the width of probes A and B should be as narrow as possible to avoid the influence of these probes on the electrical field inside the conducting channel. Also, the metal on the source/drain region reaches out to touch the channel forming Schottky contacts again. This design is used to improve the hole conduction during inversion.

To exclude the effect of source/drain series resistances, Eq. (3) is integrated from $X = X_A$ to $X = X_B$. It yields

$$I_{DS}(X_B - X_A) = C_i \mu_{FE} W (V_B - V_A) [V_G - V_T - (V_B + V_A)/2], \quad (4)$$

where V_A and V_B are the probe potential at $X = X_A$ and $X = X_B$, respectively. This equation can be rewritten as

$$I_{DS} = C_i \mu_{FE} (W/L') (V_{G\text{eff}} - V_T) \Delta V, \quad (5)$$

where $\Delta V = V_B - V_A$, $V_{G\text{eff}} = V_G - (V_B + V_A)/2$, and $L' = (X_B - X_A)$ or

$$G' = C_i \mu_{FE} (V_{G\text{eff}} - V_T), \quad (6)$$

where $G' (= I_{DS} L' / W \Delta V)$ is the effective normalized channel conductance.

In experiments, for a fixed applied gate voltage (V_G), the channel conductance (G) between probes A and B and the effective gate bias voltage ($V_{G\text{eff}}$) can be given by $G = I_{DS} / (V_A - V_B)$ and $V_{G\text{eff}} = V_G - (V_A + V_B)/2$.¹²

IV. RESULTS AND DISCUSSION

A Schottky-contact gated-four-probe *a*-Si:H(D) TFT was fabricated. Figures 2(a) and 2(b) show the drain current I_{DS} versus drain voltage V_{DS} characteristics and square root of I_{DS} versus gate bias V_{GS} plot of an *a*-Si:H TFT, respectively. Figures 3(a) and 3(b) display the similar plot for an *a*-Si:D TFT. The on-off ratio of an *a*-Si:H TFT is about a factor of 6 and the threshold voltage for electrons and holes is 8.6 and -27 V, respectively. The field-effect mobility for electrons and holes is 0.44 and 3.3×10^{-5} cm²/V s, respectively. The on-off ratio of an *a*-Si:D TFT is over a factor of 6. The threshold voltage for electrons and holes is 6.0 and -28 V, respectively, and the field-effect mobility for electrons and holes is 0.50 and 6.1×10^{-4} cm²/V s, respectively.

Figures 4(a) and 4(b) show the characteristic curves of the channel conductivity (G) versus effective gate voltage ($V_{G\text{eff}}$) of a Schottky-contact gated-four-probe *a*-Si:H TFT before and after bias stress for 10 and 20 V, respectively. The right-hand side branch of the G - $V_{G\text{eff}}$ characteristic curve represents the electron current, whereas the left-hand side one shows the characteristics of the hole current. The sub-threshold slopes for electrons (S_E) and holes (S_H) are 1.3 and 4.7 voltage per decade (V/dec), respectively, before stress, S_E and S_H change to 1.4 and 5.2 V/dec, respectively, after 10 000 s bias stress at 10 V. The threshold voltage shift for electrons (ΔV_{TE}) and for holes (ΔV_{TH}) is 0.22 and -1.1 V, respectively. An increase in ΔV_{TE} accompanying with decrease in ΔV_{TH} indicates that the interface state creation dominates the instability of devices, whereas decreases in

FIG. 2. (a) I_{DS} versus V_{DS} characteristics, (b) square root of I_{DS} as a function of gate bias V_{GS} of a -Si:H TFT.

both ΔV_{TE} and ΔV_{TH} with subthreshold swing indicate charge trapping in the a -SiN_x:H layer at or near the a -Si:H/ a -SiN_x:H interface dominates the instability. The increase in subthreshold slope for hole current can be explained by an increase in the density of states (DOS) near the valence band mobility edge, as well the increase in S_E indicates an increase in DOS near the conduction band mobility edge. Charge density trapping in the a -SiN_x:H layer at or near the a -Si:H/ a -SiN_x:H interface (n_t) could be calculated through $n_t = C_i(\Delta V_{TE} + \Delta V_{TH})/2q$,¹⁶ with C_i presenting the insulator capacitance per unit area, in our case, it is 2.2×10^{-8} F/cm². Average n_t of $6.1 \times 10^{10}/cm^2$ are trapped in the insulator after 10 000 s bias at 10 V. By using $S = kT \ln 10/q(1 + q^2 N_{SS}/C_i + \sqrt{q^2 \epsilon_{Si} N_{ds}/C_i})$,¹⁷⁻¹⁹ where C_i , ϵ_{Si} , and q represent the insulator capacitance per unit area, the silicon dielectric constant, and absolute value of the electron charge, one gets the defect density in the conducting channel of an a -Si TFT, $n_{ds} = N_{ds} \times E_G$, through subthreshold (S), interface trapped defect density, $n_t = N_{SS} \times E_G$, and optical gap of a -Si:H(D) E_G , 1.7 eV. Since S_E and S_H change from 1.3 to 1.4 V/dec and 4.7 to 5.2 V/dec, respectively, after a 10 000 s bias stress at 10 V, the DOS increases from 3.31×10^{18} to $3.87 \times 10^{18}/cm^3$ and 4.72×10^{19} to $5.79 \times 10^{19}/cm^3$ near the conduction and valence band mobility

FIG. 3. (a) I_{DS} versus V_{DS} characteristics, (b) square root of I_{DS} as a function of gate bias V_{GS} of a -Si:D TFT.

edge, respectively. In Fig. 4(b), the ΔV_{TE} and ΔV_{TH} are 1.9 and -7.5 V after 10 000 s bias stress at 20 V, respectively. The S_E value changes slightly from 1.3 to 1.4 V/dec and 5.0 to 6.2 V/dec for the S_H value. Increase in S_E and S_H value of $G-V_{G\text{eff}}$ curve could be associated with increases in the DOS of $5.3 \times 10^{17}/cm^3$ near the conduction band mobility edge and $2.9 \times 10^{19}/cm^3$ near the valence band mobility edge, respectively. And, the threshold voltage shift represents a density of $3.9 \times 10^{11}/cm^2$ trapped in the a -SiN_x:H layer at or near the a -Si:H/ a -SiN_x:H interface. The results shown in Figs. 4(a) and 4(b) indicate that the state creation dominates the instability for 10 and 20 V bias stress.

Figures 5(a) and 5(b) show the $G-V_{G\text{eff}}$ characteristic curves of a Schottky-contact gated-four-probe a -Si:D TFT before and after bias stress for 10 and 20 V, respectively. In Fig. 5(a), the ΔV_{TE} and ΔV_{TH} values after 10 000 s bias stress are 0.06 and -3.7 V, respectively. A small increase of the S_E value from 1.0 to 1.05 V/dec is observed and the S_H value increases slightly from 3.3 to 3.33 V/dec. The increase in the S_H and S_E values could indicate the increase of the DOS with a density of 4.2×10^{17} and $2.0 \times 10^{17}/cm^3$ near the valence and conduction band mobility edge, respectively. The shift of threshold voltage could be associated with $2.5 \times 10^{11}/cm^2$ positive charge trapped in the a -SiN_x:D layer at

FIG. 4. $G-V_{G\text{eff}}$ characteristics of Schottky-contact gated-four-probe $a\text{-Si:H}$ TFT before and after bias stress at gate bias of (a) +10 V and (b) +20 V.

or near the $a\text{-Si:D}/a\text{-SiN}_x\text{:D}$ interface. A smaller increase in the S_H value of an $a\text{-Si:D}$ TFT comparing with $a\text{-Si:H}$ TFTs shown in Fig. 4(a) indicates that the probability of generating the DOS near the lower part of mobility gap of $a\text{-Si:D}$ is smaller, that is consistent with what we reported before.^{11,12}

On the other hand, in Fig. 5(b), changes in the S_E and the S_H values after 10 000 s bias stress can be observed from 0.8 to 1.1 V/dec and 2.7 to 2.75 V/dec, respectively. The ΔV_{TE} and ΔV_{TH} values are 1.6 and -5.5 V, respectively. The increase in S_E and S_H values could be associated with an increase of the DOS with a density of 1.1×10^{18} and $5.7 \times 10^{17}/\text{cm}^3$ near the conduction and valence band mobility edge, respectively. And, the shift of threshold voltage could indicate the electron density of $2.7 \times 10^{11}/\text{cm}^2$ trapped in the $a\text{-SiN}_x\text{:D}$ layer at or near the $a\text{-Si:D}/a\text{-SiN}_x\text{:D}$ interface.

Comparing Figs. 4(b) and 5(b), it is concluded that the reason why the stability is improved when hydrogen is replaced by deuterium after 20 V bias stress comes mainly from a decrease in the generation of the DOS in the lower part of mobility gap of $a\text{-Si:D}$. Moreover, the results in Figs. 4(a) and 5(a) indicate that extra DOS's are generated in both higher and lower part of mobility gap after 10 V bias stress,

FIG. 5. $G-V_{G\text{eff}}$ characteristics of Schottky-contact gated-four-probe $a\text{-Si:D}$ TFT before and after bias stress at gate bias of (a) +10 V and (b) +20 V.

however, the generation of the DOS in an $a\text{-Si:D}$ TFT is less.

Figures 6(a) and 6(b) show the $G-V_{G\text{eff}}$ characteristics of a Schottky-contact gated-four-probe $a\text{-Si:H}$ TFT before and after bias stress after -10 and -20 V, respectively. The S_E value increases from 1.3 to 1.6 V/dec and the S_H value changes from 4.9 to 5.7 V/dec after 10 000 s bias stress as shown in Fig. 6(a). There is also an observable increase in the S_E and S_H values from 1.3 to 1.4 V/dec and 4.8 to 6.4 V/dec, respectively, as shown in Fig. 6(b). The ΔV_{TE} and ΔV_{TH} are -0.73 and -0.81 V after 10 000 s -10 V bias stress, respectively, and are -0.85 and -2.9 V after 10 000 s -20 V bias stress, respectively. The decrease in both ΔV_{TE} and ΔV_{TH} indicate the trapping of positive charges with density 1.1×10^{11} and $2.6 \times 10^{11}/\text{cm}^2$ in the $a\text{-SiN}_x\text{:H}$ layer at or near the $a\text{-Si:H}/a\text{-SiN}_x\text{:H}$ interface after 10 000 s bias stress at -10 and -20 V, respectively. Increases in the S_E and the S_H values are also observed, which indicate an increase in the DOS near both the conduction and valence band mobility edges. The DOS near the conduction band mobility edge increases with a density 1.8×10^{18} and $5.4 \times 10^{17}/\text{cm}^3$ after -10 and -20 V bias stress, respectively,

FIG. 6. $G-V_{G\text{eff}}$ characteristics of Schottky-contact gated-four-probe $a\text{-Si:H}$ TFT before and after bias stress at gate bias of (a) -10 V and (b) -20 V.

whereas 1.8×10^{19} and $3.9 \times 10^{19}/\text{cm}^3$, respectively, near the valance band mobility edge.

The results observed in Figs. 6(a) and 6(b) after a negative bias stress for -10 and -20 V show that the positive charge trapping in the $a\text{-SiN}_x\text{:H}$ layer or near the $a\text{-Si:H}/a\text{-SiN}_x\text{:H}$ interface dominates the instability of a TFT, that is consistent with the charge trapping model^{20,21} in which the negative bias results in charge trapping in the insulator.

Figures 7(a) and 7(b) show the $G-V_{G\text{eff}}$ characteristics of a Schottky-contact gated-four-probe $a\text{-Si:D}$ TFT before and after bias stress for -10 V and -20 V, respectively. The S_E value increases from 0.91 to 1.3 V/dec and 0.99 to 1.3 V/dec after $10\,000$ s bias stress as shown in Figs. 7(a) and 7(b), respectively. On the other hand, S_H keeps the same value at 2.9 V/dec and changes from 3.0 to 3.05 V/dec as shown in Figs. 7(a) and 7(b), respectively. It is observed that the ΔV_{TE} are -0.30 and -0.42 V after $10\,000$ s bias stress as shown in Figs. 7(a) and 7(b), respectively, and on the other hand, the ΔV_{TH} are -3.3 and -5.5 V as shown in Figs. 7(a) and 7(b), respectively. The results shown in Figs. 7(a) and 7(b) indicate that the trapping of positive charges in the $a\text{-SiN}_x\text{:D}$

FIG. 7. $G-V_{G\text{eff}}$ characteristics of Schottky-contact gated-four-probe $a\text{-Si:D}$ TFT before and after bias stress at gate bias of (a) -10 V and (b) -20 V.

layer or near the $a\text{-Si:D}/a\text{-SiN}_x\text{:D}$ interface dominates the instability after -10 and -20 V bias stress, with a density of 2.5×10^{11} and $4.1 \times 10^{11}/\text{cm}^2$, respectively. There is also an observable increase in subthreshold value S_H indicating an increase of the DOS with a density $6.3 \times 10^{17}/\text{cm}^3$ near the valance band mobility edge after -20 V bias stress and an increase in the DOS with a density of 1.7×10^{18} and $1.3 \times 10^{18}/\text{cm}^3$ near the conduction band mobility edge after -10 and -20 V bias stress, respectively. Comparing Figs. 6 and 7, it is concluded that replacing hydrogen by deuterium in active layer of a TFT device could improve the stability for -10 V and -20 V bias stress due to first reducing the DOS at the lower part of the mobility gap and second, diminishing the probability of generating the DOS near the valance band mobility edge.

Figures 8(a) and 8(b) show the ΔV_{TE} of the Schottky-contact gated-four-probe $a\text{-Si:H(D)}$ TFT as a function of bias stress time. It is observed that the ΔV_{TE} of an $a\text{-Si:H}$ TFT follows a power-law time dependence after $+20$, -20 , and -10 V bias stress as shown in Figs. 8(a) and 8(b), which is consistent with what Powell *et al.*²² have proposed. The same phenomenon is also observed in an $a\text{-Si:D}$ TFT. It is

FIG. 8. ΔV_{TE} of the Schottky-contact gated-four-probe $a\text{-Si:H(D)}$ TFT as a function of stress time during (a) $+20$ V and -20 V and (b) -10 V bias stress.

concluded that the threshold voltage shift for electrons in both $a\text{-Si:H}$ and $a\text{-Si:D}$ TFT's exhibits a power-law time dependence after $+20$, -20 , and -10 V bias stress. It is observed in Fig. 8 that the threshold voltage shift curve for an $a\text{-Si:D}$ TFT after -10 and -20 V bias stress bends down. The initiation of a negative trapped charge in the $a\text{-SiN}_x\text{:D}$ layer or near the $a\text{-Si:D}/a\text{-SiN}_x\text{:D}$ interface could be the reason responsible for this phenomenon.

V. CONCLUSIONS

It is concluded that the interface state creation, not charge injection into the insulator, dominates the instability of an $a\text{-Si:H}$ TFT after 10 and 20 V bias stress and the threshold voltage shift for electrons shows a power-law time dependence during 20 V bias stress. There is an increase in the DOS near the valence and conduction band mobility edge after both 10 and 20 V bias stress. Compared to $a\text{-Si:H}$, less the DOS is generated in the lower and upper part of mobility gap of $a\text{-Si:D}$ after 10 V bias stress, and there is an increase of the DOS near the conduction band edge and less DOS near the valence band edge in active layer of an $a\text{-Si:D}$ TFT

after 20 V bias stress. The threshold voltage shift for electrons of an $a\text{-Si:D}$ TFT also exhibits power-law time dependence as do $a\text{-Si:H}$ TFT's after 20 V bias stress.

These results show that the mechanism responsible for the improvement of stability when using deuterium instead of hydrogen after 10 and 20 V bias stress is first the decrease in the DOS in the lower part of mobility gap of $a\text{-Si:D}$, and second, diminishing the probability of generating the DOS in the lower part of mobility gap of $a\text{-Si:D}$.

The trapping of positive charges in the $a\text{-SiN}_x\text{:H}$ layer at or near the $a\text{-Si:H}/a\text{-SiN}_x\text{:H}$ interface dominates the instability of an $a\text{-Si:H}$ TFT after -10 and -20 V bias stress. There is also an increase in the DOS in both the upper and lower part of the mobility gap of $a\text{-Si:H}$. The trapping of positive charges dominates the instability of an $a\text{-Si:D}$ TFT in the same condition. It is observed that the DOS in the lower part of the mobility gap of $a\text{-Si:D}$ does not change after -10 V bias stress but slightly increases after -20 V bias stress. The DOS in the upper part of the mobility gap of $a\text{-Si:D}$ increases after both -10 and -20 V bias stress. The threshold voltage shift for electrons of both $a\text{-Si:H}$ and $a\text{-Si:D}$ TFT's exhibits power-law time dependence for -10 and -20 V bias stress.

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