Position Sensorless Control for Four-Switch Three-Phase Brushless DC Motor Drives

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Abstract—This paper proposes a position sensorless control scheme for four-switch three-phase (FSTP) brushless dc (BLDC) motor drives using a field programmable gate array (FPGA). A novel sensorless control with six commutation modes and novel pulsewidth modulation scheme is developed to drive FSTP BLDC motors. The low cost BLDC driver is achieved by the reduction of switch device count, cost down of control, and saving of hall sensors. The feasibility of the proposed sensorless control for FSTP BLDC motor drives is demonstrated by analysis and experimental results.

Index Terms—Brushless dc (BLDC) motor, four-switch three-phase (FSTP) inverter, field programmable gate array (FPGA), sensorless control.

I. INTRODUCTION

RECENTLY, the brushless dc (BLDC) motor is becoming popular in various applications because of its high efficiency, high power factor, high torque, simple control, and lower maintenance. Conventionally, BLDC motors are excited by a six-switch inverter as shown in Fig. 1. However, cost-effective design is becoming one of the most important concerns for the modern motor control research. Some researchers [1]–[6] developed new power inverters with reduced losses and costs. Among these developments, the three-phase voltage source inverters with only four switches, as shown in Fig. 2, is an attractive solution. In comparison with the usual three-phase voltage-source inverter with six switches, the main features of this converter are twofold: the first is the reduction of switches and freewheeling diode count; the second is the reduction of conduction losses.

J.-H Lee *et al.* [4] and B.-Kuk Lee *et al.* [5] both developed BLDC motor drives with trapezoidal back electromotive force (EMF) using the four-switch three-phase (FSTP) inverter: The four-space-vector scheme was used in [4], and in [5] the six commutation modes based on current control. They used position sensors to achieve commutation control of BLDC motors. However, position sensors make the total system more expensive, larger in volume, and less reliable. On the other hand, sensorless control for six-switch three-phase BLDC motors has had many successful applications.

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Fig. 1. Conventional six-switch three-phase inverter.

Fig. 2. Configuration of four-switch three-phase inverter.

Fig. 3. FPGA-based sensorless FSTP BLDC motor configuration.

Almost all sensorless control schemes [7]–[11] for six-switch three-phase BLDC motors have to detect the zero-crossing point of voltage waveforms from unexcited windings to estimate the rotor position, but it is impossible to achieve sensorless control schemes for four-switch three-phase BLDC motors by using the conventional four-space-vector strategy [4], since no floating

Fig. 4. S_x commutating modes of voltage PWM scheme for FSTP inverter: (a) Mode I (X,0); (b) Mode II (1,0); (c) Mode III (1,X); (d) Mode IV (X,1); (e) Mode V (0,1); (f) Mode VI (0,X).

winding exists. In contrast, if six commutation modes presented in [5] is used in the four-switch inverter, then there are four floating phases during the operating period. Hence, the position information can be detected from the floating line. This paper presents a novel sensorless control scheme for the FSTP BLDC motors based on [5].

On the other hand, with the rapid progress in microelectronics, field programmable gate array (FPGA) is more and more flexible, programmable and lower in cost, is therefore more and more widely used by recent researchers [12]–[15]. In order to achieve a low cost BLDC control, the Xilinx 3S100E FPGA is used to replace the microprocessor or DSP to implement the sensorless FSTP inverter scheme, as shown in Fig. 3.

II. NOVEL PWM SCHEME FOR FSTP BLDC MOTOR DRIVES

For BLDC motors with a trapezoidal back EMF, rectangular stator currents are required to produce a constant electric torque

[16]. The proposed voltage pulsewidth modulation (PWM) scheme for FSTP inverter requires six commutation modes which are (X,0), (1,0), (1,X), (X,1), (0,1) and (0,X), as shown in Fig. 4. The symbols in parenthesis denote the switch ON/OFF states of S_a^U , S_a^L , S_b^U and S_b^L (phases A and B). “X” denotes the OFF state for both the high- and low-side switching devices in the same leg, “1” denotes the ON state for the high-side switching device, and “0” denotes the ON state for the low-side switching device. There are two modes need to be noted. In Mode II, if the FSTP BLDC motor drive uses the conventional voltage PWM scheme as shown in Fig. 5, two stages corresponding to (1,0) and (X,0) in Mode II, respectively, are shown in Fig. 6(a) and (b). This conventional voltage PWM scheme provides a discharging loop between the capacitor and the low-side switch, and causes non-rectangular stator current waveforms which are harmful for constant torque, as shown in Fig. 6(c). Similar situations occur in Mode V. This paper

Fig. 5. Conventional voltage PWM scheme for FSTP BLDC motor.

proposes a novel voltage PWM to overcome this drawback, as shown in Fig. 7. There are three stages corresponding to (1,0), (X,0), and (X,X), respectively, in Mode II for the novel voltage PWM scheme, as shown in Fig. 8(a)–(c). Experimental results show that the stator current waveforms of the FSTP inverter using this novel voltage PWM scheme is rectangular, as shown in Fig. 8(d). Similar situations apply to Mode V.

The new stage (X, X) of this novel PWM scheme in Modes II and V is introduced to turn off all power devices to prevent the capacitor discharging from the low-side switch. Furthermore, the supply voltages in Modes II and V are double of those in the other four Modes while the PWM duty cycles in Modes I, III, IV and VI are double of those in the Mode II and V. We call this novel voltage PWM scheme as the asymmetric PWM scheme for FSTP BLDC motor drives. The commutation sequence and the PWM duty are shown in Table I.

III. SENSORLESS SCHEME

A. Back EMF Waveform

The FSTP BLDC motor drives using the novel voltage PWM scheme have two phases to detect the back EMF, but the split capacitors cause the voltage waveform of back EMF to be triangular like. The voltages detected from phases A and B become two triangular like waveforms, and the voltage of the uncontrolled phase (phase C) becomes $V_{DC}/2$, as shown in Fig. 9. Furthermore, the stator current waveform of the floating phase is rectangular, as shown in Fig. 8(d). Thus, it is impossible to detect the freewheel diode conducting current by the conventional zero-crossing method. Therefore, the conventional sensorless methods for BLDC motors using six-switch three-phase inverter could not be directly used in the FSTP BLDC motors. Fortunately, after observing a lot of experimental results, we found that there we two waveform crossings between phase A and B voltage waveforms which can be used to estimate the rotor position.

B. Novel Sensorless Control Scheme

If we install rotor position sensors (Hall sensors) into BLDC motors, when we observed the voltage waveforms of phases A

Fig. 6. Operation stages of FSTP inverter using conventional PWM scheme in Mode II: (a) stage (1,0), (b) stage (X,0), and (c) the experimental results of stator current waveforms.

and B, we found that two waveform crossings matched the two Hall signals (101 and 010) at the same time, respectively, as shown in Fig. 9. Therefore, we propose to use the two crossings for rotor position estimation for sensorless commutation purposes. We detect the first crossing (P1) and set the crossing timing counter to be 0. When we detect the second crossing (P2) and if the crossing timing counter is N , then the time difference, T , between two crossings can be estimated, and we reset time counter to zero.

Because there are two commutations (e.g., Mode V and Mode VI) between two crossings (P1 and P2), we can estimate

Fig. 7. Novel voltage PWM scheme for FSTP BLDC motor.

the timing of the two commutations, T_{C1} and T_{C2} , as follows. In constant speed operation, since the time difference of every commutation is constant, the first estimated commutation (T_{C1}) is equal to $T/3$, and the second estimated commutation (T_{C2}) is $2T/3$. Because there are only four crossings in one revolution, the rotor speed, ω , is equal to $\pi/hbox{2T}$. The time difference between the two crossings is equal to the crossing counter (N) multiplied by the period of the timing counter, which is 10^{-6} (s). In summary, we have

$$T = (N - 0) \times 10^{-6} \quad (1)$$

$$T_{C1} = \frac{T}{3} \quad (2)$$

$$T_{C2} = \frac{2T}{3} \quad (3)$$

$$\omega = \frac{\pi}{2T} \quad (4)$$

C. Starting Technique

The first step to start the sensorless drive is to get the initial rotor position. Since only in Modes II and V the BLDC motor is supplied by whole dc bus, the inverter could supply enough power to drive the rotor to an expected position. Therefore, for starting we simply excite the motor in Modes II or Mode V to force rotor to rotate in the specified direction.

IV. EXPERIMENT RESULTS

A. Experimental Setup

The motor used in the experimental set-up is produced by Troy in Taiwan, and its parameters are shown in Table II. The crossings of the two controlled voltages (V_V , V_U) which are filtered by low pass filters (LPF), are detected by a comparator. The proposed algorithm is implemented with the Xilinx 3S100E that is built in the Xilinx Spartan-3E sample pack. Fig. 10 shows the whole experimental system configuration. The split capacitor bank must be large enough that it can be treated as a voltage source. The voltage across capacitors and the voltage ripple are applied across the switch. It is reasonable to allow 5% voltage

Fig. 8. Operation stages of FSTP using novel PWM scheme in Mode II: (a) stage (1,0), (b) stage (X,0), (c) stage (X,X), and (d) the experimental results of stator current waveforms.

TABLE I
SWITCHING SEQUENCE OF THE NOVEL ASYMMETRIC VOLTAGE PWM SCHEME

Modes	Hall status	Active Phase	Floating Phase	Switching Devices
Mode I	010	Phase B and C	Phase A	S_b^L
Mode II	110	Phase A and B	Phase C	S_a^U and S_b^L
Mode III	100	Phase A and C	Phase B	S_a^U
Mode IV	101	Phase B and C	Phase A	S_b^U
Mode V	001	Phase A and B	Phase C	S_a^L and S_b^U
Mode VI	011	Phase A and C	Phase B	S_a^L

Fig. 9. Voltage waveforms for BLDC motor using FSTP inverter and the relationship between waveform crossings and Hall sensor signals.

TABLE II
PARAMETERS OF THE TESTED MOTOR

Variable name	Value
Number of poles	4
Number of slots	6
Rated speed	3000 rpm
Rated torque	0.392 Nt-m
Rated current	1 A
Rated power	120 W
Winding resistance per phase	5.17 Ω
Inductance across one phase to the other two phases	24 mH
Back EMF constant	0.28383 V/(rad/sec)

Fig. 10. Configuration of experimental FSTP sensorless BLDC drive system.

ripple in the voltages across C1 and C2 [17], [18]. The relationship between the capacitors' ripple voltage and the current in the capacitors is

$$i_C = C \frac{\Delta V_C}{\Delta t} \quad (5)$$

$$C = \frac{i_C \Delta t}{\Delta V_C} = \frac{i_C}{\omega \Delta V_C} \quad (6)$$

The rated current is 1 A, the carrier is 4 kHz and the supply voltage is 320 V, so the capacitor must be larger than

$$C \geq \frac{1}{4000 * 0.05 * 160} = 31.25 \mu\text{F} \quad (7)$$

We used two 330 μF capacitors in our experiment, because the capacitors had to supply startup current.

TABLE III
DEVICE UTILIZATION SUMMARY OF FPGA

Logic Utilization	Used	Available	Utilization
Total Number Slice Registers	260	1,920	13%
Number used as Flip Flops	257		
Number used as Latches	3		
Number of 4 input LUTs	523	1,920	27%
Number of occupied Slices	377	960	39%
Total Number 4 input LUTs	623	1,920	32%
Number used as logic	523		
Number used as a route-thru	99		
Number used as Shift registers	1		
Number of bonded IOBs	28	108	25%
Number of GCLKs	2	24	8%
Total equivalent gate count for design	7,318		

B. Experiment Results

Table III shows how much logic resource of FPGA is used to implement the whole system, and as shown in the table every item is below 40%. It means one can select a smaller and cheaper FPGA (e.g., S350) to further reduce the cost, or one can also build up a microcontroller Intellectual Properties (IP) into FPGA to implement more sophisticated control algorithm.

The detailed schematic diagram of the sensorless control shown in Fig. 11 consists of four blocks: startup procedure, sensorless_module, speed_calculator, and asymmetric PWM generator. The full system is implemented in Xilinx FPGA, XC3S100E or XC3S50.

In the sensorless_module, we use one XOR logic circuit to produce triggers for the rising and falling edges of the comparator. The trigger will enable the latch to catch the time interval from the timing counter, and then reset the timing counter. T_{C1} is equal to the timing interval multiplied by $1/3(Q16 : 1/3 = 65535/3 = 21845)$, and T_{C2} is double of T_{C1} . The detailed circuit is shown in Fig. 12 and the timing simulation in Fig. 13. In Fig. 13, the "comp" is the input signal from the comparator, the "xor_comp" the trigger for the latch and timing counter, "count" the time interval between two crossings, and "hall_sless" the estimated communication mode. From the results of timing simulation, we can observe that the latch grabs time interval when xor_comp rises, and the operating time of the two estimated commutation modes is equal to the third of the time interval.

The speed response of the FPGA-based sensorless control for FSTP BLDC motor drives is shown in Fig. 14. From the figure we can observe that the rotor speed is accelerated to the specified speed (720 rpm) because the novel sensorless scheme can estimate the correct rotor position. Then, we change speed command from 720 rpm to a higher speed of (2000 rpm). As demonstrates the motor runs stably at both high and low speeds under open loop position sensor less control.

Fig. 11. Schematic diagram of the sensorless FSTP inverter control IC.

Fig. 12. Logic circuit of the trigger for latch and estimated commutations.

Fig. 13. Timing simulation of the trigger for latch and estimated commutations.

Fig. 14. Speed response of the proposed sensorless FSTP BLDC motor scheme.

V. CONCLUSION

This paper has presented a novel FPGA-based sensorless control scheme for four-switch three-phase brushless dc motor drives. In the scheme, a novel asymmetric PWM scheme using six commutation modes in the FSTP inverter is proposed. The position information is estimated from the crossings of voltage waveforms in floating phases, and a low cost FPGA is utilized to implement the algorithm. Because the stator current waveforms of the FSTP inverter using this novel voltage PWM scheme are rectangular, the motor will operate smoothly and the torque ripple will be at the same level as reported in [5]. However, the two estimated commutations maybe cause commutation torque ripple. The experimental results show that the scheme works very well. With the developed control scheme and the lowest cost implementation, the proposed scheme is suitable for commercial applications.

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