Enhancement in Ultrathin Oxide Growth by Thermal-Induced Tensile Stress

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Abstract—Rapid-thermal oxide grown under the condition that a certain portion of the substrate wafer was covered by another wafer with special shape was studied. It is interesting to find that in the ultrathin oxide regime, the thickness of oxide with covered wafer is even larger than that without. Thermal-induced tensile stress is believed to be the origin of the above enhanced oxidation rate. A novel ultrathin oxide grown at a low temperature of 800 °C is demonstrated. The capacitance–voltage and current–voltage characteristics of MOS capacitors with oxides grown with and without cover wafers under the same oxide thickness were compared.

Index Terms—Tensile stress, thermal oxidation, thermal stress, ultrathin oxide.

I. INTRODUCTION

DURING the rapid growth of nanotechnology development, mechanical stress-related problems have become a key topic in the semiconductor process. There are many studies discussing the effects of stress nowadays. For example, the effect of stress on the dielectric properties of barium strontium titanate thin films was studied by applying stress during measurement [1], the leakage component can be caused by the interaction of residual stress which is dependent on the relative position of poly-Si gate at isolation edge [2], the effect of internal stress in bulk silicon is important to device performance [3], and the luminescence characteristics of compound semiconductors were affected by mechanical stress [4]. Besides, the external mechanical stress effect on the oxidation rate during thermal oxidation had also been extensively studied. It was believed that the spacing among atoms would be changed when the stress was applied during oxidation. Intrinsic stress during thermal oxidation is due to the mismatch of molecular volume and thermal expansion coefficients between Si and SiO₂ [5]–[8]. It was also mentioned that the tensile stress will pull the spacing among atoms so that the oxidation will become easier and faster [9]. Yen found that the linear rate constant is deformation dependent and the parabolic rate constant is stress dependent [10]. The oxidation rate is reduced under mechanical compressive stress and enhanced under tensile stress.

Thermal stresses are also discussed for both uniform and nonuniform temperature distribution cases. There had been several experimental approaches for the studies of thermal

stress introduced during the rapid-thermal process. Moslehi had shown that the ramp rate and processing temperature were involved for temperature nonuniformity and plastic deformation for 100-nm diameter wafers [11]. Benetini *et al.* had shown that plastic deformation could occur during the rapid-thermal processing of 50-nm diameter prepatterned silicon wafers [12]. Vandenabeele *et al.* had shown direct experimental evidence that pattern-induced temperature nonuniformity could cause plastic deformation for 150-mm silicon wafers with simple field oxide patterns [13]. In this paper, we examined the thermal stress on wafer during the rapid-thermal process. We had designed an experiment for creating tensile stress by nonuniform-thermal distribution. Thermal stress was created to wafer by putting a cover wafer over the substrate wafer so that the substrate wafer may sustain either uniform or nonuniform-thermal load during oxidation. The tensile stress will enlarge the spacing among atoms and therefore make oxidation easier and faster. The oxide-thickness distribution, capacitance–voltage (*C*–*V*) and current–voltage (*I*–*V*) characteristics of devices on the areas with and without covered wafers were studied.

Finally, by taking the merit of tensile stress that would enhance the oxidation, a novel experiment of oxidation at a low temperature of 800 °C was demonstrated to successfully grow ultrathin oxide. It was useful for the need of low-thermal budget in future ultra large scale integration (ULSI) technology.

II. EXPERIMENT

Three-inch P-type silicon wafers with a resistivity of 1–5 Ω·cm were used in this paper. In the first experiment, wafer was cleaned with the standard RCA process. A rectangular-shaped wafer was put upon the center of a 3-in wafer as the cover wafer during oxidation in the rapid-thermal processor. It is noted that the cover wafer is just placed over the substrate without bonding. The rough surface of the backside of the cover wafer provides enough resistance to prevent the cover wafer from sliding during oxidation if the flow rate of inlet gas is not too high. Oxygen atoms are still able to penetrate through the gap between the two rigid bodies of cover wafer and substrate. The limited supply of oxygen as described above is just suitable for the growth of ultrathin gate oxide. Fig. 1(a) shows the schematic diagram of wafer position with rectangular cover wafer. Wafer was oxidized in 100-torr oxygen at 950 °C for 40 s. After Al film deposition, MOS capacitors with an area of 150 × 150 μm² were formed by conventional photolithography. Current density versus voltage (*J*–*V*) curves were measured by HP4140 and *C*–*V* curves were measured with HP4280. In the second experiment,

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Fig. 1. Measurement areas of the wafers oxidized with (a) rectangular and (b) square cover wafers in 100 torr at 950 °C for 40 s (or 50 s).

Fig. 2. Distributions of (a) inverse capacitance and (b) flat band voltage of the wafer covered by rectangular-shaped wafer oxidized in 100 torr at 950 °C for 40 s.

a square-shaped wafer was put upon the side of a 3-in wafer during oxidation in a rapid-thermal processor, as shown in Fig. 1(b). After Al film deposition and photolithography, J - V and C - V characteristics were measured.

Taking the advantage of stress that tensile stress would help oxidation being easier, an experiment of oxidation at low temperature was designed. Wafer was cleaned by standard RCA process similarly. A rectangular-shaped wafer was put upon the center of a 3-in wafer during oxidation in rapid-thermal processor, as shown in Fig. 1(a). The wafer was oxidized in 100-torr oxygen at 800 °C for 40 s. Generally, it is quite difficult for the growth of oxide under 800 °C without stress. The devices in the areas with and without cover wafers were investigated.

III. RESULTS AND DISCUSSIONS

A. Distribution of Thickness and V_{FB}

C - V characteristics were measured from the MOS devices on the wafers in the first experiment. Fig. 1(a) shows the measurement area. Here, we use the inverse capacitance at $V_{FB} - 1$ V as the representative of the thickness, as shown in Fig. 2(a). The distribution of flat band voltage in absolute value is shown in Fig. 2(b). It has been obviously shown that the oxides under covered part were thicker than the other part. It is suggested that the uncovered part was heated and the volume becomes larger. On the other hand, the covered part was

Fig. 3. Distribution of inverse capacitance of the wafer covered by square-shaped wafer oxidized in 100 torr at 950 °C for 40 s.

less heated and its volume was less changed. The difference of thermal expansions between these two parts let the uncovered part to pull the covered part. The tensile stress was therefore produced in the covered part, so the spacing among atoms in covered part was pulled and made the lattice of silicon being match to the lattice of silicon oxide. Therefore, the oxidation rate becomes fast and easy. This phenomenon was rechecked by another experiment. And the results are similar to those shown in Fig. 2. It was confirmed that the oxides in covered area are thickened by the stress effect. According to the report of Deaton and Massoud [14], the oxidation rate at the edge

Fig. 4. (a) Original $C-V$ curves, (b) two frequencies extracted $C-V$ curves fitted with theoretical one considering quantum mechanical effect, and (c) $J-V$ curves of the devices on the wafer oxidized at 950 °C for 40 s with stress and on the wafer oxidized at 950 °C for 60 s without stress under the same EOT of 22 Å.

of wafer can be enhanced by the thermally induced tensile stress. A tensile stress of 1×10^7 dyn/cm² will induce an increase of about 2 Å at 900 °C [14]. In this case, it was found that the oxide-thickness difference between the covered and uncovered parts as extracted from the measured capacitances of them was about 10 Å provided that the dielectric constant of oxide is still 3.9. Since the dielectric constant of the oxide grown in the covered part is different from that of normal one, the actual oxide-thickness difference as mentioned above is overestimated. Nevertheless, the expected tensile stress in the covered part might be larger than 1×10^7 dyn/cm².

It is concerned that the shape of cover wafer would influence the result of oxidation, so another experiment of using a square-shaped wafer, as shown in Fig. 1(b), as the cover wafer was carried out to reconfirm the observation. Fig. 3 shows the distribution of inverse capacitance at $V_{FB} - 1$ V as the representative of the thickness. One can see that the thickness of oxide in covered area is thicker than uncovered one. It is noted that the uniformity of inverse capacitance as observed in Figs. 2(a) and 3 is poor. It is known that for a silicon wafer oxidized in a rapid-thermal process, the oxide-

thickness distribution is stress dependent and is also orientation dependent [14]. The sustained stress distribution across the covered part of substrate in this paper is obviously dependent on the temperature distribution, which is related to the shape of covered wafer, and also on the oxidation condition, such as the oxidation temperature, pressure, and time. It is believed that the above stress distribution is nonuniform. Since the observation of the enhanced oxidation rate in covered part is reproducible, it is reasonable to believe that the thermal stress as induced by the temperature difference between the covered and uncovered parts is the major source for the above observation. The portion of the covered part suffers from the tensile stress and is easy to be oxidized in the very early of oxidation. Namely, wafers can be oxidized easily by using tensile stress.

B. Reliability of Oxides in Stressed and Unstressed Areas

The qualities of oxides play a very important role in the characteristics of devices. If the quality of oxide in covered area is as good as or better than the oxide in uncovered area under the same equivalent oxide thickness (EOT), one can use the

above method of oxidation to replace the conventional one. We examined the reliability of devices in covered and uncovered areas with same EOT. Control wafer was oxidized in 100 torr at 950 °C for 60 s without cover wafer. The devices with an EOT of 22 Å were chosen from the part of covered wafer and the control one. Fig. 4(a)–(c) show original C – V curves, two frequencies extracted C – V curves filled with theoretical one considering quantum mechanical effect, and J – V curves of the samples on the wafer oxidized in 950 °C for 40 s with stress and on the wafer oxidized without stress in 950 °C for 60 s, under the same EOT of 22 Å. The thicknesses of the two samples are confirmed by comparing the extracted C – V curves with quantum mechanical C – V ones, as shown in Fig. 4(b). From the original C – V curves, it is noticed that the flat band voltages of all samples are almost the same. Second, stressed samples and unstressed samples appeared different characteristics obviously in the accumulation region. C – V curves of stressed samples seemed to be normal, while those of unstressed ones exhibit dramatic attenuation. There had been many studies on the attenuation of C – V curves. The reasons include polydepletion effect, parasitic effect in short channel device [9], and quantum mechanical effect [10], etc. In this case, it was suggested that the high leakage of oxide, as represented by a resistance R_p in parallel with C_{ox} , is the dominate effect. In other words, the more severe the attenuation, the worse the oxide quality.

From the leakage currents in J – V curves, as shown in Fig. 4(c), it was observed that although some stressed samples show bad characteristics due to the effect of nonuniform distribution of stress, some stressed samples exhibit lower leakage current than unstressed ones under the same EOT. From the above discussion, it is noted that some samples of oxide under stress have better qualities than the unstressed ones. It is noted that the stressed samples show nonuniform and unexpected characteristics, some are better than unstressed samples and some are worse than unstressed ones. Although the control of stress is complicated and is worthy of investigating, an idea of using the advantage of stress for ultrathin oxide growth application is arisen.

C. Growth of Oxide at Low Temperature

Since tensile stress would enlarge the spacing among atoms so that the oxidation would become easier, it is believed that the wafer with tensile stress is able to oxidize even at a relative low temperature. In this experiment, wafer was oxidized in 100 torr oxygen at only 800 °C for 40 s. The distribution of thickness, i.e., inverse capacitance, was shown in Fig. 5. C – V curves were examined only on some samples at special positions on wafer as indicated in Fig. 5 and were shown in Fig. 6. C – V curves of samples in uncovered areas, i.e., positions a, c, d, and f give no information about the thickness. However, the growth of oxide occurs in the covered area, i.e., positions b and e, clearly. That is to say that one can grow ultrathin oxides at low temperature by utilizing thermal stress.

IV. CONCLUSION

Tensile stress can make oxidation to be easier, and is used to grow ultrathin oxide at low temperature. In the first experiment,

Fig. 5. Distribution of inverse capacitance of wafer oxidized at 800 °C for 40 s with rectangular-cover wafer.

Fig. 6. C – V curves of stressed samples at positions of a, b, c, d, e, and f as indicated in Fig. 5.

the thermal tensile stress was produced by applying cover wafer over substrate wafer during oxidation. It has been obviously observed that the thicknesses under covered part are thicker than the other part. In the second experiment, we take use of thermal tensile stress to grow oxide at low temperature. It was found that the uncovered area is unable to grow oxide, but the covered area is able. It is believed that the proposed oxidation technology is useful for the preparation of ultrathin oxides in ULSI node. However, the stressed samples show nonuniform and unexpected characteristics.

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