Temperature-induced voltage drop rearrangement and its effect on oxide breakdown in metal-oxide-semiconductor capacitor structure

Tsung-Miau Wang and Jenn-Gwo Hwu^{a)}

EE-II, R.446, Department of Electrical Engineering/Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, Republic of China

(Received 30 August 2004; accepted 29 November 2004; published online 26 January 2005)

This work studies the breakdown (BD) characteristics of metal-oxide-semiconductor (MOS) capacitors at various temperatures. The oxide thickness and temperature significantly affect the probability of BD. BD does not easily occur in ultrathin silicon dioxide when biased in the positive substrate injection region of MOS(*p*). However, the BD frequency increases dramatically with the oxide thickness or the temperature. The phenomenon was explained by temperature effect. When the temperature increases, the voltage drop across the silicon dioxide increases; on the contrary, the voltage across the (deep) depletion region in the Si substrate declines. Also, the enhancement of percolation and the increase in the number of interface states result in the more severe degradation of the silicon dioxide. Also, a thicker oxide has more Dit, and so undergoes degradation more easily. Finally, the *C*–*V* characteristics of the MOS capacitor in the (deep) depletion region are also discussed in order to understand the mechanisms among temperature, thickness, and percolation effect. © 2005 American Institute of Physics. [DOI: 10.1063/1.1850199]

INTRODUCTION

As electronic devices continue to be scaled down, breakdown (BD) is an important issue in the evaluation of the integrity of such devices, and has attracted much attention.^{1–3} Two types of breakdown—hard breakdown (HBD) and soft breakdown (SBD)—are usually considered.^{4,5} However, when the thickness of the silicon dioxide is below 5 nm, SBD dominates^{6,7} and causes the devices to fail when used in the analog circuits; failure does not severely damage digital circuits.^{8–10} Although many studies investigated SBD, many mechanisms are confusing and discussion is lacking.^{11–13} Temperature and thickness are usually the key factors considered in studies of BD.^{12–14} In this work, for a metal-organic-semiconductor (MOS)(*p*) capacitor fabricated on a *p*-type Si substrate, the probability of SBD increases with temperature when biased in the saturation current region under substrate injection. That is to say, the SBD depends on temperature in this case. The increase in the probability of SBD follows from the fact that increasing the temperature increases both the number of minority carriers and Dit when the positive substrate injection region is biased. Therefore, the number of charges across the silicon dioxide increases so the voltage drop across the oxide increases, and finally SBD occurs. Besides, increasing the temperature will cause percolation, which is also a main cause of oxide degradation.² However, this phenomenon is not observed in the accumulation region under gate injection, where only HBD occurs, affecting the intrinsic properties of the oxide.¹⁵ Namely, BD depends on the polarity. Finally, the *C*–*V* characteristics are presented and support the above explanation. At high temperature, the unsmooth *C*–*V* curves indicate the trapping or

detrapping of thermionic electrons in the interface, and consequently, the degradation of the oxide^{14,16} caused by the increase of Dit. The *C*–*V* properties also indicate the occurrence of percolation in the depletion region.

EXPERIMENT

After standard Radio Corporation of America (RCA) cleaning and HF dipping, *p*-type (100) silicon wafers with a resistivity of 1–5 Ω cm were separately oxidized in a rapid thermal processor at 850 °C for 5, 10, and 15 s in oxygen at 50 Torr to yield oxides of different thicknesses. They were labeled chip 1, chip 2, and chip 3, respectively. Aluminum was evaporated onto each wafer, and the metal gates were patterned by conventional photolithography. The underside of each wafer was coated with an aluminum film to form MOS(*p*) capacitors after backside oxides were removed. The

FIG. 1. The *J*–*V* characteristics of the MOS(*p*) capacitors of chip 1 measured at various temperatures. HDB occurred at the same gate voltage when biasing in the accumulation region but no SBD occurred when biasing in the saturation region. The breakdown properties are polarity dependent.

^{a)}Also at: Department of Electronic Engineering / Department of Electrical Engineering, National United University, Miaoli, Taiwan, Republic of China; electronic mail: hwu@cc.ee.ntu.edu.tw

FIG. 2. The J - V characteristics of the MOS(p) capacitors of chip 2 measured at various temperatures. HDB occurred at the same gate voltage when biasing in the accumulation region but SBD occurred only at 90 °C when biasing in the saturation region. The breakdown properties are polarity and temperature dependent.

final oxide thicknesses of chips 1, 2, and 3 were 2.6, 2.9, and 3.1 nm, respectively, as determined by quantum mechanism fitting of C - V curves.

RESULTS AND DISCUSSION

Figures 1, 2, and 3 demonstrate the temperature dependence of the typical I - V characteristics of the MOS(p) capacitors for chips 1, 2, and 3, respectively. In Fig. 1, the oxide thickness is 2.6 nm and SBD does not occur when the saturation current region is biased under positive substrate injection at temperatures of 30, 60, or 90 °C. That SBD does not easily occur is one of the intrinsic properties of thin oxide because the electrons will tunnel through the thin oxide easily and the voltage across the oxide is not sufficiently high to induce oxide breakdown. Moreover the data in Fig. 1 indicate that SBD is independent of temperature for such a thin oxide. However, HDB almost occurs at the same gate voltage at various temperatures when the accumulation region is biased under negative gate injection. This finding

FIG. 3. The J - V characteristics of the MOS(p) capacitors of chip 3 measured at various temperatures. HDB occurred at the same gate voltage when biasing in the accumulation region but SBD occurred at 60 and 90 °C when biasing in the saturation region. Distinct polarity and temperature dependencies of the breakdown properties are shown.

FIG. 4. The schematic band diagrams for a MOS(p) capacitor with the thin oxide biased at positive substrate injection region under low and high temperatures.

implies that the observed HDB is caused by the same mechanism when the oxides are biased negatively. In Fig. 2, the oxide thickness is 2.9 nm and SBD occurs in the positive substrate injection region at a temperature of 90 °C. In the accumulation region, temperature-independent HDB is still observed. In Fig. 3, the oxide thickness is 3.1 nm and SBD occurs at temperatures of 60 and 90 °C when the saturation region is biased. A higher temperature corresponds to an earlier occurrence of SBD. Similarly, temperature-independent HDB is still observed in the accumulation region.

From Figs. 1–3, two clear regularities are observed: (1) increasing the temperature increases the probability of SBD in the saturation region but not of HDB in the accumulation region, and (2) SBD occurs more easily when the oxide is thicker and the saturation region is biased. In the positive substrate injection region, the voltage drops across the oxide and the Si substrate. The voltage drop across the thicker oxide is larger since the tunneling current less easily flows through the oxide. Therefore, a thicker oxide suffers from a large change of the oxide field if the carriers in the substrate are changed. In summary, Figs. 4 and 5 present two energy-band diagrams for thin and thick oxides, respectively. Figure 4 shows the band diagrams of the n -type metal-oxide semiconductor (NMOS) system with the thinner oxide at various temperatures. The solid line relates to low temperature while the dashed line relates to high temperature. Deep depletion is common when the oxide is thin enough and the positive substrate injection region is biased. Restated, thin oxide cannot sustain most of the applied voltage because tunneling occurs easily. Therefore, a large portion of the voltage drop is across the deep depletion region in the Si substrate. Since the oxide tunneling probability becomes large when the oxide becomes thin, the supply of minority carriers in the Si substrate may not be quick enough to reach thermal equivalent, so the current becomes saturated, as revealed by the I - V characteristics. When the temperature increases, the width of the (deep) depletion decreases and the voltage drops change;¹⁴ the voltage drop across the silicon dioxide in-

FIG. 5. The schematic band diagrams for a MOS(*p*) capacitor with the thick oxide biased at positive substrate injection region under low and high temperatures.

creases but that across the (deep) depletion region decreases. Increasing the voltage drop increases the electrical field, enhancing the degradation of the oxide. Fortunately, this phenomenon is not serious when the oxide is thin enough. In Fig. 5, the same concept applies to the thicker oxide. A deep depletion is observed even when the oxide is thicker, since the positive substrate injection current is saturated, as demonstrated in Fig. 3. The oxide is thicker than that in Fig. 4, so tunneling through the oxide is less easy than through the thinner oxide. Therefore, the voltage drop across the oxide differs from that described above. As for the thin oxide, as the temperature increases, the depletion width decreases and the voltage drop changes. Namely, the voltage drop across the oxide increases but the voltage drop across the depletion region declines. The change of the voltage drop in the thick oxide exceeds that in the thin oxide since the tunneling probability is smaller in the thick oxide. Therefore, BD is more likely in the thick oxide as temperature increases. Figures 6, 7, and 8 present the time zero dielectric breakdown (TZDB) data for chips 1, 2, and 3, respectively. The voltage was swept from zero bias to 5 or -5 V, and the breakdown voltages were recorded. The I - V characteristics of 25 devices were measured at each temperature and the breakdowns were recorded when the currents appear as current jumps during sweep. For instance, the I - V characteristics of 25 devices were measured on chip 1 at 90°C as the voltage was swept from 0 to 5 V, then the I - V characteristics of another 25 devices were measured on chip 1 at 60°C as the voltage was swept from 0 to 5 V. Statistical data are shown, from which some important information can be gained. Figure 6 plots the BD characteristics of chip 1. In the accumulation region, the intrinsic oxide breakdown causes HBD to occur at almost the same voltage, almost independent of temperature. However, in the saturation region, SBD barely occurs at all for two reasons: (1) the oxide is too thin and (2) the induced oxide degradation is not severe. For chip 2, as shown in Fig. 7, the

FIG. 6. The cumulative number of TZDB data for chip 1. HBD is independent of the temperature conditions in the gate injection region and no obvious SBD occurred in the substrate region.

frequency of SBD depends strongly on the temperature. At a low temperature, such as 30°C , SBD never occurs but when

FIG. 7. The cumulative number of TZDB data of chip 2. HBD is temperature independent while SBD is affected by the temperature conditions. The polarity and temperature dependencies of the breakdown properties are shown.

FIG. 8. The cumulative number of TZDB data of chip 3. HBD is still temperature independent while SBD is strongly affected by the temperature conditions. The higher temperature will enhance the degradation of the oxide and make the breakdown occur earlier.

FIG. 9. The C - V characteristics of the MOS(p) capacitors with the thick and thin oxides measured at low and high temperature. The unsmooth curves were found in the heated samples. The phenomenon implies that the charge trapping is unstable in the interface.

at a high temperature, such as 90 °C, over half of the devices break down. This phenomenon becomes more apparent as the oxide becomes thicker. In Fig. 8, SBD occurs when the temperature exceeds 60 °C. Briefly, increasing the temperature promotes the degradation of the oxide, and especially that of a thicker oxide.

Figure 9 plots the C - V characteristics of oxides of three thicknesses at room temperature and at 80 °C at 100 kHz. When the depletion region is biased at room temperature, the C - V curves are smooth, regardless of whether the oxide is thin or thick. However, as the temperature increases, like at 80 °C, the curves cease to be saw toothed, indicating that thermionic electrons may bombard the interface of SiO_2/Si , causing electron trapping in the interface. This fact may explain the instability of the C - V curves as the temperature increases. The thermionic electrons induce the degradation of oxide by percolation. And the percolation phenomenon is believed to be one of the main causes of SBD events in the saturation region.

The C - V properties of the fresh and stressed samples were compared. Figure 10 plots the C - V curves before and after constant voltage stressing (1 V) at room temperature

FIG. 10. The C - V characteristics of the samples in chip 1 before and after positive-bias temperature stress. The C - V curves do not change seriously when the oxide is thin, whether the temperature is high or low.

FIG. 11. The C - V characteristics of the samples in chip 3 before and after positive-bias temperature stress. The C - V curves change seriously when the oxide is thick, whether the temperature is high or low. The increases of Dit and the occurrence of percolation mechanism are origins for the above phenomenon.

and 90 °C for 200 s. The C - V characteristics of chip 1 seem almost unchanged, regardless of the temperature. However, for the thick chip 3, as depicted in Fig. 11, the C - V curves vary greatly. For the thin oxide, even after stressing at high temperature, the degradation caused by percolation is not severe. Therefore, the C - V properties are almost unaffected after stressing. Although a high temperature causes the emission of thermionic electrons that damage the interface, for a thin oxide, the degradation is not serious. The suboxide of the thin oxide is known to be thin but that of the thick oxide is thick.¹⁷ The suboxide region can be considered to be the origin of Dit. Dit promotes the degradation of the oxide and is the precursor to percolation that results in SBD when the saturation region is biased. In Fig. 11, the C - V properties of chip 3 with a thicker oxide differ greatly between the two temperatures. The capacitance after stressing at room temperature is much higher because Dit is increased. However, the capacitance after stress at 90 °C initially increases and then declines as the bias voltage increases. When the voltage is small at around zero, the increase in Dit dominates the behavior. However, when the gate voltage is large, the leakage current through the percolation path in the oxide dominates. The device exhibits deep depletion since its oxide is too leaky. This result indicates that a higher temperature and a thicker oxide promote the serious percolation problem that degrades the oxide.

CONCLUSIONS

Temperature and oxide thickness are regarded as factors that importantly determine oxide breakdown. Increasing the temperature accelerates the degradation of the oxide and causes SBD, especially when the oxide is thick. A high temperature changes the voltage drop, shifting it from the depletion region to the oxide. A high voltage across the oxide results in a large change in the electric field and the occurrence of percolation that triggers SBD. The above observations are more obvious when the oxide is thicker. The C - V characteristics are consistent with the BD mechanisms pro-

posed in this study. The effect of temperature must be considered in evaluating the BD behavior of an ultrathin gate oxide.

- ¹E. Y. Wu and R.-P. Vollertsen, *IEEE Trans. Electron Devices* **49**, 2131 (2002).
- ²E. Y. Wu, J. Suñé, and W. Lai, *IEEE Trans. Electron Devices* **49**, 2141 (2002).
- ³M. Houssa, T. Nigam, P. W. Mertens, and M. M. Heyns, *J. Appl. Phys.* **84**, 4351 (2004).
- ⁴W. Mizubayashi, Y. Yoshida, H. Murakami, S. Miyazaki, and M. Hirose, *IEEE Electron Device Lett.* **25**, 305 (2004).
- ⁵E. Miranda, J. Suñé, R. Rodríguez, M. Nafria, F. Martín, and X. Aymerich, *Jpn. J. Appl. Phys., Part 1* **38**, 2223 (1999).
- ⁶E. M. Vogel, M. D. Edelstein, and J. S. Suehle, *J. Appl. Phys.* **90**, 2338 (2001).
- ⁷E. Miranda, J. Sune, J. R. Rodriguez, M. Nafria, and X. Aymerich, *Reliability Physics Symposium Proceedings, 1998* (unpublished), p. 42.
- ⁸T. Nigam, S. Martin, and D. Abusch-Magder, *Reliability Physics Symposium Proceedings, 2003* (unpublished), p. 417.
- ⁹R. Thewes, R. Brederlow, C. Schlunder, and P. Wiczorek, *Tech. Dig. - Int. Electron Devices Meet.* **1999**, 81.
- ¹⁰W. Mizubayashi and S. Miyazaki, *Jpn. J. Appl. Phys., Part 1* **43**, 6925 (2004).
- ¹¹M. Depas, T. Nigam, and M. M. Heyns, *IEEE Trans. Electron Devices* **43**, 1499 (1996).
- ¹²E. Y. Wu, J. M. McKenna, W. Lai, E. Nowak, and A. Vayshenker, *IEEE Electron Device Lett.* **22**, 603 (2001).
- ¹³J. S. Suehle, E. M. Vogel, B. Wang, and J. B. Bernstein, *Reliability Physics Symposium Proceedings, 2000* (unpublished), p. 33.
- ¹⁴A. Yassine and R. Hijab, *1997 IEEE International Integrated Reliability Workshop (IRW) Final Report*, (unpublished), p. 56.
- ¹⁵H.-T. Huang, M.-J. Chen, C.-W. Su, J.-H. Chen, C.-S. Hou, and M.-S. Liang, *IEEE Trans. Electron Devices* **48**, 1275 (2001).
- ¹⁶A. Meinertzhagen, C. Petit, D. Zander, O. Simonetti, T. Maurel, and M. Jourdain, *J. Appl. Phys.* **91**, 2123 (2004).
- ¹⁷Y.-P. Lin and J.-G. Hwu, *Jpn. J. Appl. Phys., Part 1* **40**, 6788 (2001).