Ultrathin Aluminum Oxide Gate Dielectric on N-Type 4H-SiC Prepared by Low Thermal Budget Nitric Acid Oxidation

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Abstract—MOS capacitors with an ultrathin aluminum oxide (Al_2O_3) gate dielectric were fabricated on n-type 4H-SiC. Al_2O_3 was prepared by room-temperature nitric acid (HNO_3) oxidation of ultrathin Al film followed by furnace annealing. The effective dielectric constant of $k \sim 9.4$ and equivalent oxide thickness of 26 Å are produced, and the interfacial layer and carbon clusters are not observed in this paper. The electrical responses of MOS capacitor under heating and illumination are used to identify the conduction mechanisms. For the positively biased case, the conduction mechanism is shown to be dominated by Schottky emission with an effective barrier height of 1.12 ± 0.13 eV. For the negatively biased case, the gate current is shown to be due to the generation–recombination process in depletion region and limited by the minority carrier generation rate. The feasibility of integrating alternative gate dielectric on SiC by a low thermal budget process is demonstrated.

Index Terms—Aluminum oxide, deep depletion, generation–recombination current, minority carrier, MOS, nitric acid, Schottky emission, SiC.

I. INTRODUCTION

SILICON carbide (SiC) is used in high-power and high-temperature applications [1]–[3] due to its wide bandgap (3.23 and 3.0 eV for 4H- and 6H-SiC), high breakdown field (3–5 MV/cm), and large thermal conductivity (3.7–4.9 W/cm·°C) [4]. Moreover, the intrinsic carrier concentration (n_i) of 4H-SiC is in the order of 10^{-7} cm $^{-3}$ at room temperature while that of Si is 10^{10} cm $^{-3}$, i.e., 17 orders larger than 4H-SiC. This intrinsic property leads to a very small carrier generation–recombination rate in SiC and makes it capable of nonvolatile memory device applications [5], [6]. For SiC-based metal–oxide–semiconductor (MOS) devices, the breakdown voltage, on-resistance, operation temperature, and transconductance are of essential concern. In particular, the gate oxide used in SiC-based MOS devices is important to device performance such as channel mobility and device reliability

[7]. It had been shown that there exist some C-rich regions adjacent to the SiO_2 –SiC interface formed by thermal oxidation and volatilization of CO molecules [8], and the residual carbon atoms can enhance the scattering events to degrade the channel mobility. For another consideration of long-term reliability, the electrical field sustained by gate oxide is generally less than 3 MV/cm to prevent the catastrophic dielectric breakdown before the reversible avalanche breakdown occurs in bulk SiC [2].

There are comprehensive studies focused on the preparation of SiO_2 gate oxide on SiC, and the interfacial quality together with carbon related topics are the most crucial factors. For the dry/wet O_2 -oxidation followed by Ar annealing processes, the complex Si–C–O compounds and the incomplete removal of carbon atoms degrade the interfacial quality and oxide reliability [9]. For the nitridation processes including direct thermal oxidation in nitrogen-contained gas and post-oxidation annealing, both nitric oxide (NO) and nitrous oxide (N_2O) are shown to be more effective in interface trap passivation and carbon removal. It was proposed that interface states could be passivated by the strong $\text{Si}\equiv\text{N}$ bonds which shift the energy levels of interface states in the bandgap [9]–[12]. Furthermore, the incorporated N atoms aid removing carbon clusters more effectively by creating the C–N bonds [9], [10]. The NO annealing also improves the inversion channel mobility of MOSFETs fabricated on 4H-SiC by reducing the interface state density [13]. In regard to the aforementioned techniques for conventional SiO_2 gate oxide, the thermal oxidation of SiC substrate and the removal of carbon clusters generally need enormous thermal budget, i.e., long-running high-temperature process (> 1000 °C for hours).

Aluminum oxide (Al_2O_3) is a widely investigated gate dielectric with benefits in many aspects [14]–[17] and it can be formed in diluted nitric acid (HNO_3) [18], but fewer studies had been made for Al_2O_3 on SiC. Lazar *et al.* proposed Al_2O_3 – SiO_2 gate stack deposited on 6H-SiC by metal–organic remote plasma chemical vapor deposition (RPCVD) with low temperature oxide (LTO) as interfacial layer, and the fabricated MOS capacitor exhibits excellent current–voltage (I – V) and capacitance–voltage (C – V) behaviors with reduced net oxide charge [19]. Gao *et al.* constructed the interfacial structural model and band alignments of the atomic layer chemical vapor deposited Al_2O_3 –SiC system, and the extracted interface state density can be one order of magnitude lower than thermal oxide [20]. In this work, ultrathin Al_2O_3 gate dielectric was grown on n-type 4H-SiC by a novel room temperature HNO_3 oxidation process. Material analyzes were carried out and the electrical

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properties were characterized. The fabricated MOS capacitor exhibits satisfactory I - V and C - V properties. The conduction mechanisms in positively and negatively biased regions are explored by the temperature and illumination responses of MOS capacitors.

II. EXPERIMENTS

The 4H-SiC wafer with a nitrogen-doped n^- epi-layer on n^+ substrate purchased from CREE Research Inc. was used in this paper. The wafer was 8.03° off orientated with a resistivity of $0.02 \Omega \cdot \text{cm}$. The thickness and doping concentration of the epi-layer were $10 \mu\text{m}$ and $2.6 \times 10^{15} \text{ cm}^{-3}$, respectively. The wafer was first immersed in the mixture of H_2SO_4 and H_2O_2 for 15 min and then followed by the standard SC-1 and SC-2 RCA procedures. After the last HF dip step, the wafer was promptly loaded in the evaporation chamber and the pure Al (99.999%) was thermally evaporated onto the SiC surface with a thickness of $20 \text{ \AA}$ at a base pressure of 1×10^{-6} torr. The as-deposited Al film was oxidized immediately in diluted HNO_3 ($\text{HNO}_3 : \text{H}_2\text{O} = 1 : 19$) at room temperature. Post-oxidation annealing (POA) was performed at 650°C for 3 min in N_2 to densify the obtained gate dielectric, and the gate material was also thermally evaporated by using 99.999% pure Al. The $150 \times 150 \mu\text{m}^2$ pattern transformation as well as gate formation were performed by photolithography and wet etching, respectively. Finally, Al back contact was thermally evaporated after the removal of native oxide by buffered oxide etchant (BOE).

I - V and C - V properties of the fabricated MOS capacitors were characterized by an HP 4140B pA meter and an HP 4284A precision LCR meter, respectively. The equivalent oxide thickness (EOT) was extracted by using accumulation capacitance measured at 100 KHz. The high temperature measurements were implemented on a thermal chuck up to 250°C .

III. RESULTS AND DISCUSSIONS

A. HRTEM Result and Chemical Bonding Analysis

Fig. 1 shows the high-resolution cross-sectional transmission electron microscope (HRTEM) image of the fabricated MOS structure. The Al_2O_3 film remains amorphous and shows uniform thickness. The physical thickness and EOT are 90 and $37.25 \text{ \AA}$, respectively. The effective dielectric constant of Al_2O_3 can be estimated to be 9.4 which is close to the theoretical value ($k \sim 10$). It also can be observed that the interfacial layer (IL) and the carbon cluster are not found in Fig. 1. The IL growth for high- k material deposition is generally inevitable and will diminish the effective dielectric constant of the gate insulator itself. The absence of these interfacial species and the nearly ideal dielectric constant indicate the suppression of Al_2O_3 -SiC interfacial reaction by the low thermal budget process. It is known that the lowest binding energy of a crystal is proportional to its energy bandgap, hence, the IL formed by Al evaporation, oxidation, and subsequent POA is difficult to grow in Al_2O_3 -SiC system than in Al_2O_3 -Si one.

The compositions of the obtained Al_2O_3 gate dielectric and Al_2O_3 -SiC interface are analyzed by X-ray photoelectron spectrum (XPS). Both the peaks of Al-silicate (Al-Si-O) with

Fig. 1. HRTEM picture of Al_2O_3 gate dielectric MOS capacitor. The dash lines indicate the interfaces of Al gate- Al_2O_3 and Al_2O_3 -SiC substrate. A 90 $\text{\AA}$ gate dielectric with smooth interfaces and uniform thickness is observed.

Fig. 2. XPS results of (a) Si 2p, (b) C 1s, and (c) Al 2p spectra of Al_2O_3 gate dielectric.

a binding energy near 102.7 eV and suboxide (Si-O) with a binding energy around 103.5 eV are not emerged in the Si 2p spectrum as shown in Fig. 2(a). However, the positions associated with Al-silicate and suboxide bonding units exhibit a weak intensity which is slightly higher than the background signal. This behavior corroborates the existence of bridging O atoms in the Al_2O_3 -SiC transition region and is consistent with the model proposed by Gao *et al.* which claims that Al_2O_3 network is connected with SiC by the O atoms [20]. The C-C component ($\sim 284.5 \text{ eV}$) is insignificant as shown in Fig. 2(b) which suggests the absence of carbon cluster. Lin *et al.* reported that metallic Al and native Al_2O_3 caused by natural oxidation in atmosphere coexist in the as-deposited Al film, and they can be oxidized into stoichiometric Al_2O_3 by anodization [21]. The Al 2p spectrum illustrated in Fig. 2(c) confirms that Al evaporated on SiC can also be converted into Al-O structures by room temperature HNO_3 oxidation. It can be concluded from the XPS results that the evaporated ultrathin Al film can be

Fig. 3. C - V curves measured at room temperature of Al_2O_3 on 4H-SiC for bidirectional sweep. The theoretical one is also shown for comparison. The insert shows the local magnification of deep depletion region.

completely oxidized by the well-controlled room temperature HNO_3 oxidation without the growth of IL and carbon cluster.

B. C - V and I - V Characteristics

The high-frequency C - V curves measured at room temperature together with the theoretical result are plotted in Fig. 3. The insert shows the local magnification of the deep depletion region of the C - V curves. It can be clearly seen that the C - V curves exhibit deep depletion behavior rather than inversion because of the insufficient supply of the minority carrier, which is resulted from the very low n_i of SiC. The C - V hysteresis is originated from the polarization of interface traps by charging and discharging during gate bias bidirectional sweep. The flatband voltage (V_{FB}) split of C - V hysteresis in Al_2O_3 -SiC system is only 21 mV that suggests a satisfactory interfacial quality in between, which is consistent with the slightly stretched C - V curves as compared to the theoretical one. The theoretical and experimental values of V_{FB} for Al gate are 0.1 and 0.61 V, respectively, the effective negative oxide fixed charge density can thus be calculated to be $3.77 \times 10^{12} \text{ cm}^{-2}$. The negative oxide charge is known to exist in Al_2O_3 grown by various processes, and the charge density extracted from the positively shifted V_{FB} is comparable with that reported by H. R. Lazar *et al.* [19]. The negative oxide fixed charge could also be provided by interface traps because these states will act as fixed charges when they are not located in the majority carrier bandedge [22].

Gate current density versus gate voltage (J_G - V_G) relationship of Al- Al_2O_3 -SiC system is demonstrated in Fig. 4. The negatively biased J_G , i.e., the deep depletion region, is supplied by minority carriers generated by interface states, SiC bulk traps in the depletion region, and diffused from back contact. The effects of these three components on gate current and the correlations between process control and deep depletion current level are given in [14]. The “nearly-saturated” current behavior indicates that evaporated Al film can be suitably oxidized in diluted HNO_3 without IL growth and serious damage to SiC substrate even after high temperature POA. It must be pointed out that the negatively biased current level of Al_2O_3 -SiC system is lower than that in Al_2O_3 -Si system [14] due to the lower n_i and the absence of IL, i.e., the fewer process-induced bulk traps. The effective oxide breakdown field in positively biased region, i.e.,

Fig. 4. J - V curve measured at room temperature of Al_2O_3 on 4H-SiC. The effective breakdown field is 5.77 MV/cm. The positively biased current is dominated by Schottky emission as shown in the inset.

Fig. 5. Relationships between gate current density, temperature, and effective oxide field. The Schottky barrier height extracted from the slope is 1.12 eV.

accumulation region, calculated by using EOT is 5.77 MV/cm, which is comparable with Si_3N_4 on 4H-SiC [7]. To identify the positively biased conduction mechanism of Al_2O_3 on n-type 4H-SiC, the temperature dependencies on J_G are explored. The J_G of MOS capacitor conducted by Schottky emission as shown in the inset of Fig. 4 can be expressed as follows [23].

$$J \propto A^* T^2 \exp \left[-\frac{q}{kT} \left(\phi_B - \sqrt{\frac{qE}{4\pi\epsilon}} \right) \right] \quad (1)$$

where

$$A^* \equiv \frac{4\pi q m^* k^2}{h^3} \quad (2)$$

is the effective Richardson constant, q the electron charge, m^* the effective electron mass in Al_2O_3 ($\sim 0.11 m_o$, [14]), k the Boltzmann's constant, h the Planck's constant, T the temperature, ϕ_B the Schottky barrier height, E the effective electrical field, and ϵ the permittivity of gate insulator. It can be observed in Fig. 5 that J_G 's increase with temperatures ranging from 150 to 250 °C in the positively biased region. This implies that J_G is conducted by Schottky emission and the effective Schottky barrier height extrapolated from the slope is 1.12 ± 0.13 eV. This barrier height would not be large enough for SiC MOS devices; therefore, the growth of an initial SiO_2 layer, i.e., Al_2O_3 - SiO_2 -SiC structure, may be useful to increase the gate stack-SiC barrier height and improve the interfacial properties. The positively biased J_G is comparable with SiO_2 on Si under

Fig. 6. C - V curves of negatively biased operated in depletion region under dark and illumination conditions of Al_2O_3 on 4H-SiC. The curve under illumination still shows deep depletion rather than inversion.

Fig. 7. J - V curves of Al_2O_3 on 4H-SiC measured under dark and illumination conditions. The curve under illumination is enhanced by three orders in negatively bias region due to minority carrier generation.

the same EOT due to the smaller conduction band offset in Al_2O_3 -SiC system.

C. Minority Carrier Response for Illumination and Heating

Minority carriers in semiconductors can be excited by illumination which generates electron-hole pairs in bandgap or by heating which increases n_i . The negatively biased C - V curves under dark and illumination conditions are illustrated in Fig. 6. These curves were measured at room temperature and their accumulation capacitances were similar. The illumination case, however, shows deep depletion behavior though the minority carrier generation rate is enhanced. The carrier generation under illumination is still not strong enough to convert the SiC surface to strong inversion mode because of the very low n_i of SiC at room temperature (on the order of 10^{-7} cm^{-3}). This fact suggests that most of the applied gate voltage is dropped across the depletion region to broaden the depletion width and stabilize the voltage across the gate dielectric. The deep depletion phenomenon under illumination can also be confirmed by the saturated current behavior. Fig. 7 shows the J_G - V_G curves under dark and illumination conditions. The negatively biased J_G changes by three orders under illumination while that in positively biased region keeps the same. The positively biased J_G is dominated by the Schottky barrier height but not sensitive to the majority carrier concentration, it is consequently not affected by illumination. In the negatively biased region, both the majority

Fig. 8. J - V curves of Al_2O_3 on 4H-SiC operated in negatively biased region for different temperatures. The current levels keep saturation and increase with temperatures.

and minority carriers should be taken into account. For the majority carrier (electron), the voltage drop across the gate dielectric is too small to bring about the Fowler-Nordheim (F-N) tunneling and the direct tunneling is also difficult to occur because of the thicker dielectric physical thickness. The Al- Al_2O_3 barrier height had been reported to be 1.6 eV which is large enough to obstruct electron tunneling from Al gate across the gate dielectric [14]. Accordingly, the negatively biased J_G is enhanced by the minority carriers generated in the broadened depletion region by illumination but the device continues operating in deep depletion mode. The results of Figs. 6 and 7 mean that the negatively biased J_G is controlled by the minority carrier generation rate while the positively biased one is independent of the majority carrier concentration and is confined by the Schottky barrier.

To further identify the conduction mechanism of Al_2O_3 -SiC system, the high temperature current behavior is also investigated. The n_i of SiC can be represented by the following equation [4]:

$$n_i = 3.95 \times 10^{15} \times T^{3/2} \exp\left(\frac{-E_g}{2kT}\right) \quad (3)$$

where E_g is the bandgap of 4H-SiC and is almost invariant for our measuring scope. It can be found from (3) that n_i is strongly temperature dependent and has a 10-orders-increase for temperatures ranging from 50 to 250°C. The negatively biased J_G - V_G curves measured at high temperatures are shown in Fig. 8. As can be seen, the saturated current behavior indicates that the gate currents at evaluated temperatures are still limited by minority carrier generation rate. According to the Shockley-Read-Hall theory, the minority carrier generation rate is proportional to n_i [24], hence, the negatively biased J_G increases monotonously with temperatures. The current component provided by generation-recombination process in depletion region (J_{rg}) of MOS capacitor can be described as follows [25]:

$$J_{rg} = \frac{qn_i w}{\tau} \left[\exp\left(\frac{q\phi_s}{2kT}\right) - 1 \right] \quad (4)$$

where w is the depletion width, τ the minority carrier lifetime, and ϕ_s the difference between the electron and hole quasi-Fermi levels. Since the inversion layer does not exist under deep depletion condition, the $\exp(q\phi_s/2kT)$ term responsible for inver-

Fig. 9. Negatively biased gate current density versus intrinsic carrier concentration for different temperatures. The slope of 0.978 in log-log scale indicates that gate current is controlled by intrinsic carrier concentration.

sion charge should be ignored and the J_{rg} can be represented by the qn_iw/τ term. The correlations between $\log(J_G)$ at -4 V and $\log(n_i)$ are examined in Fig. 9. The straight line fit in log-log scale yields a slope of 0.978 which corresponds to the relationship by

$$J_{G,-4V} \propto n_i^{0.978}. \quad (5)$$

The slope of 0.978 indicates that J_G is directly proportional to n_i and, therefore, dominated by the generation-recombination process in the depletion region. It must be mentioned that the current components provided by interface states and back contact are normally existed and can still contribute minority carriers into total gate current. The gate current is thus partially composed of carriers provided by interface states and back contact but mainly conducted by J_{rg} . The analysis of Figs. 8 and 9 prove that negatively biased J_G of Al-Al₂O₃-4H-SiC system is limited by n_i (intrinsic property) and conducted by J_{rg} with recombination process.

IV. CONCLUSION

An n-type 4H-SiC MOS capacitor with ultrathin Al₂O₃ gate dielectric prepared by room temperature HNO₃ oxidation of ultra-thin Al film is demonstrated in this work. The evaporated ultrathin Al film can be suitably oxidized and the IL as well as carbon clusters are not produced in this process. The EOT of 26 Å and an effective dielectric constant of 9.4 are achieved. The fabricated MOS capacitor shows a slight charge trapping behavior and a negative oxide fixed charge density of $3.77 \times 10^{12} \text{ cm}^{-2}$. Schottky emission with an effective barrier height of $1.12 \pm 0.13 \text{ eV}$ is shown to be the dominant carrier transport mechanism in the positively biased region. For the negatively biased case, J_G is found to be limited by the minority carrier generation rate and is conducted by generation-recombination current in the depletion region. The proposed process technology with a very low thermal budget is believed to be helpful for the preparation of gate dielectric on SiC.

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