Growth-Then-Anodization Technique for Reliable Ultrathin Gate Oxides

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Innovation of growth-then-anodization technique is introduced in this work to prepare high-quality ultrathin gate oxides. In repeated direct-current anodization (RDC-ANO) process, the first oxides were prepared by DC5V-ANO with thin and thick thickness followed by rapid thermal anneal. The repeated anodizations were carried out by various dc voltages and also followed by the same anneal. It was found that when the voltage of the repeated ANO is higher than that of the first ANO, the RDC-ANO oxides will superior to the one time grown DC-ANO ones provided that the first oxide thickness is thin enough. The electrical improvements include reduced leakage, higher time-zero dielectric breakdown (TZDB), and time-dependent dielectric breakdown (TDDb) endurance. In rapid thermal oxide followed by anodization process, the anodization technique of direct current superimposed with alternating-current anodization (DAC-ANO) is applied to repair the traps of thermally grown ultrathin gate oxides. Effects of anodization time and thermal oxide thickness are inspected. It was experimentally observed that the quality of thermal oxides is well improved by this proposed growth-then-anodization method. The electrical improvements include reduced leakage, better uniformity and less stress-induce-leakage-current (SILC) behavior.

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Metal-oxide-semiconductor field-effect-transistor (MOSFET) is the most important device in ultralarge scale integration (ULSI) circuits. Due to the excellent stability, uniformity, and simple fabrication process, silicon dioxide (SiO₂) has been used as the gate dielectric of MOSFETs for more than 40 years since MOSFET had been introduced to VLSI technology. As the size of device scales down to obtain high density and performance, the thickness of SiO₂ also needs to scale down. Based on the International Technology Roadmap for Semiconductor (ITRS), the equivalent oxide thickness (EOT) should be 1.5 nm in 2005.¹ However, as the growth temperature of thermally grown ultrathin oxides is reduced for better control, many traps, and pinholes are generated resulting in unreliable properties. It is generally accepted that the defects in the oxide significantly enhance the gate leakage current, which in turn degrade the device performance and eventually cause device failure.^{2,3} It is believed that the gate leakage current density higher than 1.0 A/cm² is a limited value of the leakage current.⁴ Thus, the conventional furnace and rapid thermal oxidation (RTO) are not perfect enough to grow ultrathin gate oxides in the next generation complementary metal oxide semiconductor (CMOS) technology, and the oxide reliability becomes a serious issue.⁵ We proposed a method called growth-then-anodization to identify the weak spots in growing ultrathin gate oxide and repair them by selective anodization to solve this problem. It is believed that anodization exhibits the self-readjustment nature of current conduction through the weak path in the oxide.⁶ To understand the characteristic of anodic oxide clearly, a process with multiple oxidations, called repeated anodization process (RDC-ANO), is designed. At the first dc anodization step (DC-ANO), some weak leaky paths are existed in oxide, and it is supposed that the followed anodization could repair the weak paths and reconstruct the oxide. As a result, we can find that the RDC-ANO oxides can provide the improvements in oxide thickness uniformity and in electrical performance, including reduced leakage and enhanced breakdown endurance. Another process of combining the conventional RTO and anodization is designed to make the anodization technique practical in CMOS technology. The process is denoted as rapid thermal oxide followed by anodization process (ANO/RTO). By controlling the applied voltage and anodization time in the process, it is ensured that current during anodization flows almost entirely through only the weak spots in the formed oxide. Thus, the thermal oxide treated with anodization shows de-

creased leakage current and improved reliability without increasing the oxide thickness. This growth-then-anodization is effective to improve the integrity of ultrathin gate oxides.

Experimental

The 3 in. boron-doped P-type (100) silicon wafers with a resistivity of 1-10 Ω cm were used in this work. After standard RCA cleaning, the oxidation is carried out by growth-then-anodization technique. The anodization was processed in D.I. water, and Pt was used as the cathode. Two processes were investigated in this work, one is repeated anodization and another is rapid thermal oxidation followed by anodization technique.

In the repeated anodization process, two recipes were used to grow the SiO₂ layer. The SiO₂ layers were prepared by DC 5V with 18 min for samples denoted as A, and dc 5 V with 25 min for samples denoted as B. Rapid thermal post-oxidation anneal (POA) is performed in N₂ ambient at 900°C, 200 Torr for 20 s after SiO₂ was grown. The repeated DC-ANO was carried out as soon as possible to avoid the possible contamination to the SiO₂ layer, and this is very important to oxide quality. To densify the anodic oxide, POA in N₂ ambient at 900°C, 200 Torr for 20 s was adopted again. The

Figure 1. Oxide thickness vs. anodization time for DC10V-ANO, DC5V-ANO, and DC3V-ANO oxides.

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Table I. Notation for samples prepared by repeated DC anodizations.

Samples	First DC-ANO	Repeated DC-ANO
A	DC 5 V	No
RDC3V-ANO-A	18 min	DC 3 V, 50 min
RDC5V-ANO-A	11 Å	DC 5 V, 18 min
RDC10V-ANO-A		DC 10 V, 9 min
B	DC 5 V	No
RDC3V-ANO-B	25 min	DC 3 V, 20 min
RDC5V-ANO-B	16 Å	DC 5 V, 12 min
RDC10V-ANO-B		DC 10 V, 3 min

relationship between the oxide thickness and the growing time with various anodization voltages was shown in Fig. 1. According to it, sample A is about 11 Å and sample B is about 16 Å. The repeated dc anodizations of samples A were prepared by dc 3 V (50 min), 5 V (18 min), and 10 V (9 min) and denoted by RDC3V-ANO-A, RDC5V-ANO-A, and RDC10V-ANO-A, respectively, as shown in the Table I. And the repeated dc-anodizations of samples B were prepared by dc 3 V (20 min), 5 V (12 min), and 10 V (3 min) as denoted by RDC3V-ANO-B, RDC5V-ANO-B, and RDC10V-ANO-B, respectively. The increasing thickness in repeated dc anodization was about 12 Å in sample A and 7 Å in sample B, and the total thickness we got in the experiment was about 23-24 Å. For sample A, the increased thickness in the repeated dc anodization and the thickness in the first dc anodization were controlled to be almost the same, while for samples B the increased thickness in the repeated dc anodization was thinner than the thickness in the first dc anodization.

In the rapid thermal oxidation followed by anodization process, a O_2 pressure of 20 Torr at 750°C for 5 s, denoted as RTO (21 Å), and 10 Torr at 700°C for 5 s, denoted as RTO (19 Å), had been processed. Then an ac oscillation, 0.7 V, in accompany with a positive voltage, 1 V, was used in the anodization process. Three various anodization times of 1, 5, and 10 min were used to repair the traps in the thermal oxide prepared by RTO. For the case of 21 Å, these three samples were denoted as DAC1m-ANO/RTO (21 Å), DAC5m-ANO/RTO (21 Å), and DAC10m-ANO/RTO (21 Å), respectively; in another case of 19 Å, they were denoted as DAC1m-ANO/RTO (19 Å), DAC5m-ANO/RTO (19 Å), and DAC10m-ANO/RTO (19 Å), respectively, which were shown in the Table II. POA was then treated to all samples in N_2 ambient (200 Torr) at 850°C for 20 s. The thickness of gate Al was fixed at 2000 Å and the MOS capacitors of size $150 \times 150 \mu m$ were formed by conventional photolithography. The back oxide was removed with buffered HF solution and Al was formed as the back contact. The MOS current-voltage (I-V) curves were measured with an HP-4140, and the capacitance-voltage (C-V) curves with an HP4280. The extracted capacitance C_{ext} was obtained from the two-frequency correction method developed by Hu.⁷

Table II. Notation for samples prepared by RTO first and followed by DAC anodizations.

Samples	RTO	DAC-ANO
RTO (19 Å)	10 Torr, 700°C, 5 s	No
DAC1m-ANO/RTO (19 Å)	19 Å	1 min
DAC5m-ANO/RTO (19 Å)		5 min
DAC10m-ANO/RTO (19 Å)		10 min
RTO (21 Å)	20 Torr, 750°C, 5 s	No
DAC1m-ANO/RTO (21 Å)	21 Å	1 min
DAC5m-ANO/RTO (21 Å)		5 min
DAC10m-ANO/RTO (21 Å)		10 min

Figure 2. Gate current density at $V_g - V_{FB} = -1$ V vs. anodization voltage characteristics of the RDC10V-ANO-A, RDC5V-ANO-A, and RDC3V-ANO-A oxides.

Results and Discussion

Repeated anodization process.—A sample with 22 Å was prepared by dc 5V anodization to contrast with the repeated oxidation samples and was denoted as DC5V-ANO. The gate current density at $V_g - V_{FB} = -1$ V vs. anodization voltage characteristics were shown in Fig. 2. The measurements were performed on at least 16 capacitors for each sample. The average gate leakage current densities at the gate voltage of $V_g - V_{FB} = -1$ V are 8.35×10^{-4} , 1.26×10^{-2} , and 6.96×10^{-2} A/cm² for samples RDC10V-ANO-A, RDC5V-ANO-A, and RDC3V-ANO-A, respectively. The RDC10V-ANO-A sample exhibits the smallest gate leakage current and the best oxide quality for repeated anodization with sample A.

The average gate leakage current densities, 2.86×10^{-2} , 3.21×10^{-2} , and 3.31×10^{-2} A/cm² for samples RDC10V-ANO-B, RDC5V-ANO-B, and RDC3V-ANO-B, respectively, as the gate voltage were biased at $V_g - V_{FB} = -1$ V were shown in Fig. 3. It was found that the gate leakage current densities in Fig. 3 are almost of the same level. However, sample RDC10V-ANO-B exhibits the best oxide quality because of its thinnest oxide thickness. It is clearly observed that the effect of high repeated anodization voltage for samples B is not as significant as samples A. This is probably due to the thicker initial oxide of samples B than that of A.

Figure 3. Gate current density at $V_g - V_{FB} = -1$ V vs. anodization voltage characteristics of the RDC10V-ANO-B, RDC5V-ANO-B, and RDC3V-ANO-B oxides.

Figure 4. The Weibull plots of TZDB characteristics of the RDC10V-ANO-A, RDC5V-ANO-A, RDC3V-ANO-A, DC5V-ANO, RDC10V-ANO-B, RDC5V-ANO-B, and RDC3V-ANO-B oxides.

For breakdown endurance evaluation, the Weibull distributions of time-zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB) were shown in Fig. 4 and 5, respectively. The V_{FB} of each sample was calculated by the C-V method and has been taken into account in calculating the oxide field. A constant field of -14 MV/cm (*i.e.*, the thickness of 24 Å was stressed by a constant V_G of -3.36 V) was given in TDDB. In the TZDB characteristics as shown in Fig. 4, sample RDC10V-ANO-A exhibits improvement over DC5V-ANO oxide. For the TDDB performance as shown in Fig. 5, sample RDC10V-ANO-A is still apparently the most resistant one among all the samples. Sample RDC5V-ANO-A also shows better uniformity in distribution than DC5V-ANO. The other repeated anodization samples are even less resistant to the electrical stress than DC5V-ANO oxide.

The preferable reliability of sample RDC10V-ANO-A shows that the leakage paths can be suitably repaired during repeated anodization. The compensation effect by anion redistribution seems effective at a voltage higher than the first anodization one. This is why 10 V repeated anodization is effective in oxide quality improvement for

Figure 5. The Weibull plots of TDDB characteristics of the RDC10V-ANO-A, RDC5V-ANO-A, RDC3V-ANO-A, DC5V-ANO, RDC10V-ANO-B, RDC5V-ANO-B, and RDC3V-ANO-B oxides.

Figure 6. The distribution of gate capacitance of DAC1m-ANO/RTO (19 Å), DAC5m-ANO/RTO (19 Å) and DAC10m-ANO/RTO (19 Å) biased at the gate voltage of -1.5 V. The inset shows the C-V curves of the above devices. All of the curves are extracted by two-frequency method.

sample RDC10V-ANO-A. However, when the initial oxide thickness is larger, such as 16 Å for sample B, the improvement of the repeated anodization process is suppressed. It is therefore suggested that an even higher repeated anodization voltage is needed to efficiently improve the quality of sample B. As the results, we suggest that anodization of a grown gate oxide can repair the traps in oxide.

Rapid thermal oxide followed by anodization process.—The inset of Fig. 6 shows the gate capacitance (C_g) vs. gate voltage (V_g) characteristics of the MOS capacitors. The measurements were performed on at least 25 devices for each condition, and the Weibull distributions of these gate capacitances, which were used to show the uniformity, were adopted in Fig. 6. The thickness of oxide can be got by two frequencies C-V measurement, and the result of the thickness is 19 Å. In Fig. 6, it was observed that sample DAC1m-ANO/RTO (19 Å) has the highest gate capacitance. It means that the oxide thickness of DAC1m-ANO/RTO (19 Å) is thinner than the other two, and the gate capacitance of DAC5m-ANO/RTO (19 Å) and DAC10m-ANO/RTO (19 Å) are almost the same. The J-V characteristics of these samples were shown in the inset of Fig. 7. It was observed that the J_s decreases with anodization time. The Weibull plots were used in Fig. 7 to show the uniformity of the gate leakage current at the gate voltage of -2.5 V. The results indicate that the optimum anodization time in the case of 19 Å is 10 min. In comparison, the optimum anodization time in the case of 21 Å is 5 min. As the result, it can be determined that the optimum anodization time decreases with the thermal oxide thickness. A possible reason for the different optimum anodization time is that an oxide grown at a lower oxidation temperature, such as 700°C for 19 Å, exhibits a higher density of traps in oxide. Thus, the needed time to repair the traps in oxide grown in low temperature is longer than that grown in high temperature.

Samples DAC5m-ANO/RTO (21 Å) and DAC10m-ANO/RTO (19 Å) were chosen to compare with samples RTO (21 Å) and RTO (19 Å), which were not repaired by DAC anodization. The C-V curve of sample RTO (19 Å) shown in Fig. 8 is seriously deformed. This is because, even after two frequencies correction, the sample RTO (19 Å) has serious attenuation. The leakage current of sample RTO (19 Å) is around 18.2 A/cm ^{2} at -2 V of gate voltage, and it is too high to determine the exact thickness by two frequencies C-V method. The value of 19 Å is quoted from the compared one of DAC-ANO/RTO for reference. The J-V curves of RTO (19 Å), DAC10m-ANO/RTO (19 Å), RTO (21 Å) and DAC5m-ANO/RTO

Figure 7. The distribution of gate current density of DAC1m-ANO/RTO (19 Å), DAC5m-ANO/RTO (19 Å) and DAC10m-ANO/RTO (19 Å) biased at the gate voltage of -2.5 V. The inset shows the J-V curves of the above devices.

(21 Å) were shown in the inset of Fig. 8, and it can be found that the difference of J_g between RTO (19 Å) and DAC10m-ANO/RTO (19 Å) is larger than that between RTO (21 Å) and DAC5m-ANO/RTO (21 Å). The results support the conclusion that the oxide quality improvement increases as the thickness of oxide decreases. This is because the thinner oxide had to be grown in lower temperature and more traps were created, and the effect of anodization in thinner oxide was therefore more significant than the thicker one.

The detailed C-V curves of RTO (21 Å) and DAC5m-ANO/RTO (21 Å) are compared in Fig. 9. It was observed that although the C-V curves extracted from two frequencies were almost the same, the C-V curves in 1 MHz were much different. The difference between 1 MHz and two-frequency extracted C-V curves for DAC5m-ANO/RTO (21 Å) is smaller than that of RTO (21 Å). This is another way to demonstrate the efficiency of the repairing of traps during anodization. The uniformity of capacitance was shown in Fig. 10 by Weibull plot. Sample DAC5m-ANO/RTO (21 Å) shows better uniformity than sample RTO (21 Å), owing to the self-

Figure 8. The C-V curves of RTO (19 Å), DAC10m-ANO/RTO (19 Å), RTO (21 Å) and DAC5m-ANO/RTO (21 Å). All of the curves are extracted by two-frequency method. The inset shows the J-V curves of the above devices.

Figure 9. The 1 MHz and two-freq. extracted C-V curves of RTO (21 Å) and DAC-ANO/RTO (21 Å).

readjustment nature of current conduction through the weak path in the oxide during anodization.

There is no obvious occurrence of breakdown in these ultrathin oxides because of the happening of the direct tunneling. As the result, TDDDB was replaced with constant field stress-induced-leakage-current (SILC) to examine the reliability of ultrathin oxides. The difference of current densities of samples RTO (21 Å), DAC5m-ANO/RTO (21 Å) and DAC10m-ANO/RTO (19 Å), between fresh and stressed, at the gate voltage of -2.5 V with various stressed fields were shown in Fig. 11. The thermal oxides treated with anodization present better reliability than RTO ones. It is supposed that there were many weak spots generated in thermal oxide during RTO resulting in unreliable properties. The compensation effect by anion redistribution during voltage switching in followed DAC anodization repairs the weak spots in the oxide.

Conclusion

In this work, a novel growth-then-anodization technique for growing reliable ultrathin gate oxides is adopted. The techniques include the process of repeated anodization and rapid thermal oxide followed by anodization. From the process of repeated anodization, the characteristic of anodic oxides grown by multiple oxidations are

Figure 10. The distribution of gate capacitance of RTO (21 Å) and DAC-ANO/RTO devices biased at the gate voltage of -2 V.

Figure 11. $J_g(\text{stressed}) - J_g(\text{fresh})$ vs. stressed field at negative bias for RTO and DAC-ANO/RTO devices.

explored, and it is believed that anodization of grown oxide can repair the traps in oxide. Through the process of rapid thermal oxidation followed by anodization, the effectiveness of the anodization

technique is again confirmed in improving the quality of the existing thermal oxide, and it can be incorporated with CMOS technology.

From the results, it was found that if the anodization time and voltage were optimized, the growth-then-anodization technique could improve the electrical characteristics of gate oxide no matter what the growth methods were used at the first. And the results support that the improvement is more effective as the initial thickness of oxide is thinner.

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