Electrical characteristics of ultra-thin gate oxides (<3 nm) prepared by direct current superimposed with alternating-current anodization

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Abstract

Ultra-thin gate oxides with thickness smaller than 3 nm were prepared by anodic oxidation (anodization) in de-ionized water under direct-current biasing superimposed with alternating-current signal (DAC-ANO). It is experimentally observed that the DAC-ANO oxides after suitable high temperature annealing have better electrical characteristics than conventional rapid thermal oxides (RTO). Other advantages of DAC-ANO oxides include lower leakage current, higher time-zero dielectric breakdown and time-dependent dielectric breakdown endurance, and less stress-induced leakage current. The charge trapping behavior under high field stress is less significant in DAC-ANO oxides than in RTO ones. The improved reliability of DAC-ANO oxides can be explained by the nature of AC switching effect. DAC-ANO oxide is a potential candidate in the application of ultra-thin gate oxide to deep sub-micron devices.

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1. Introduction

Silicon dioxide (SiO₂) has been used as the gate dielectric of metal-oxide-semiconductor field-effect-transistor (MOSFETs) for years due to its good stability, reliability, uniformity, and simple fabrication process. As the dimension of devices scales down to obtain a higher packing density and a better device performance, the oxide thickness also needs to be thinner. According to the International Technology Roadmap for Semiconductor (ITRS), the oxide thickness will be reduced to 1.5 nm in 2005. However, reduced oxide thickness brings several challenges such as increased gate leakage current and serious dopant penetration. It is believed that the

gate leakage current of 1.0 A/cm² is a limit for the advanced CMOS technology [1].

To solve the problems mentioned above, we study an alternative oxidation process called anodization (ANO), i.e., anodic oxidation, which is featured as a room-temperature process for preparing ultra-thin SiO₂ gate dielectric. Unlike the conventional furnace oxidation or rapid thermal oxidation (RTO), ANO has lower thermal budget, less thermal stress and negligible dopant penetration [2–4]. In addition, the ANO oxides followed by rapid thermal nitridation are of better electrical properties than RTO oxides. The incorporated nitrogen would relieve the strained interfacial bonding and suppress interface trap generation [5]. According to our previous work, the negative oxide-trapped charge in ANO oxides is the origin of lower leakage current and higher breakdown endurance in comparison with thermal oxides. These pre-trapped negative charges induced by ANO will increase the effective barrier height and

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retard the electron injection from the metal gate. The tunneling probability is therefore reduced so that the leakage current of ANO oxides is decreased [3]. The negative oxide trapped charge in ANO oxides comes from the redistribution of anion and self-compensation effect of AC oscillation during the oxide growth. In our previous work, it was found that the alternating-current ANO under suitable AC frequency can redistribute the anions in electrolyte and repair the leaky paths in oxides [4]. Another essential concern of ultra-thin gate oxides used in modern ULSIs is the reliability. Because the oxide thickness is less than 20 Å, the time-zero dielectric breakdown (TZDB) and time-dependent dielectric breakdown (TDDB) tests are hard to implement owing to the catastrophic increase in gate leakage current. The electrical stress-induced leakage current (SILC) behavior is therefore the major means for evaluating the reliability of ultra-thin gate oxides. The tunneling mechanism of SILC had shown to be one of the important reliability issue. It had been reported that SiO₂ grown by wet-oxidation had been identified to be more reliable than that obtained by dry-oxidation due to the strengthened O₃≡Si–OH bond [6]. The SILC is also verified as an oxide wear-out with increasing oxide trap density [7]. As a matter of fact, oxides with lower trap generation rate can meet the need for long-term reliability in device operation.

In this work, we demonstrate the characteristics of ultra-thin SiO₂ grown by DC superimposed with AC ANO (DAC-ANO) technique. The AC signal was superimposed with DC voltage so that the net applied voltage is kept at positive during ANO. DAC-ANO oxides are found to be less leaky than RTO ones. The reliability of DAC-ANO oxides, including TZDB, TDDB, and SILC are also better than RTO oxides. The charge trapping behavior under constant voltage stress is also studied. It is suggested that DAC-ANO oxide is a potential candidate of highly reliable ultra-thin gate oxides.

2. Experiments

In the DAC-ANO experiments, the power supply that produces DC voltage and the function generator that provides AC signal are connected in series to the silicon wafer during ANO. The DAC-ANO experimental setup system and the voltage setting profile are shown in Fig. 1. The DC bias was fixed at +15 V and the superimposed AC signal was adjusted to have an amplitude of 5 V and a switching frequency of 200 Hz. The platinum plate was used as the cathode. The ANO time for DAC-ANO was 20 min. The reaction of ANO of p-Si can be described as follows [8]. First, the DI water dissociates into H⁺ and (OH)[−] ions

Fig. 1. (a) The schematic diagram of the DAC-ANO experimental setup system. (b) Designed voltage profiles applied to the silicon wafer in the DAC-ANO experiment.

Next, the electrochemical potential difference between the silicon and the electrolyte prompts the holes supplied from the bulk of semiconductor to the semiconductor–electrolyte interface. These holes excite the silicon atoms on the silicon surface to a higher energy state

where h^+ denotes the holes supplied from the bulk of semiconductor. The dissociated (OH)[−] ions then bond with Si²⁺ to become silicon hydroxide

The silicon hydroxide is in turn transferred to SiO₂ and release hydrogen

The overall reaction can thus be expressed by combining Eqs. (1)–(4) as follows:

Three-inch, Boron-doped (100) P-type silicon wafer with a resistivity of 1–10 Ω cm was adopted as the sub-

strate of MOS capacitors. Standard RCA cleaning was carried out. Before the oxidation process, the native oxide was removed by diluted HF. The oxidation was then implemented by DAC-ANO or RTO. All samples underwent rapid thermal post-oxidation-anneal (RTA) in N_2 ambient (200 Torr) at 850 °C for 20 s to densify the oxides. Aluminum film with a thickness of around 3000 Å was thermally evaporated on the oxides as the gate material. The photolithography and wet etching were performed to define the $150\ \mu\text{m} \times 150\ \mu\text{m}$ square patterns. Finally, the native oxide on the backside of the wafer was removed by buffered oxide etchant and aluminum was soon evaporated to form the back contact.

Current–voltage (I – V) and capacitance–voltage (C – V) characteristics were measured by HP4140B pA meter and HP4284 precision LCR meter, respectively. Oxide thickness was extracted by fitting the C – V curve after two-frequency, i.e., 1 M and 100 KHz, correction [9] under the consideration of quantum mechanical effect [10]. All measurements were done at room temperature.

3. Results and discussion

Fig. 2 shows the gate current density versus gate voltage (J – V) characteristics of the DAC-ANO and RTO oxides with different oxide thickness. Obviously, the leakage current of DAC-ANO oxides is smaller than that of RTO oxides. It is noted that the leakage current of DAC-ANO 18 Å oxides is approximately one order of magnitude lower than that of RTO 20 Å oxides. The inset shows the C – V curves of the samples shown in Fig. 2. The capacitance dropping in the strong accumulation region of RTO 20 Å oxide is originated from the excess leakage current, which decreases the parallel capacitance

Fig. 2. The J – V characteristics of the DAC-ANO and RTO oxides. The inset shows the gate capacitance versus gate voltage (J – V) characteristics of the DAC-ANO and RTO oxides.

Fig. 3. The average current density at $V_{OX}(V_G - V_{FB}) = -1\text{ V}$ versus oxide thickness for DAC-ANO and RTO oxides.

of MOS capacitor. Variations in gate leakage current under the oxide voltage $V_{OX}(=V_G - V_{FB})$ of -1 V for DAC-ANO and RTO samples are shown in Fig. 3. Each symbol represents the average value of measurements over 20 devices. Evidently, the leakage currents of DAC-ANO oxides are lower than those of RTO oxides with thickness ranging from 18 to 29 Å. The reduced leakage current of DAC-ANO oxides can be attributed to the AC switching effect. The voltage of DAC-ANO switches between 10 and 20 V with an average of 15 V. At the moment of voltage switching, the $(OH)^-$ ions can redistribute and re-select their directions. Therefore, the redistributed $(OH)^-$ ions will move toward the leaky path and repair the imperfect bonds in the oxides. The “self-compensation” effect due to $(OH)^-$ ion redistribution enhances the quality and uniformity of DAC-ANO oxides.

Reliability of DAC-ANO and RTO oxides are characterized by TZDB, TDDB, and SILC. The Weibull distributions of TZDB for DAC-ANO and RTO oxides are shown in Fig. 4. It is found that DAC-ANO oxides can sustain higher electrical field than RTO ones. The larger breakdown field confirms that there are fewer pinholes formed in the DAC-ANO oxides. The results of constant field TDDB test for these oxides are shown in the inset of Fig. 4. The time-to-breakdown t_{BD} 's under an electrical field of -9 MV/cm of DAC-ANO oxides are all longer than 1000 s while those of RTO oxides range from 30 to 1000 s. The t_{BD} distribution reveals that the uniformity of DAC-ANO oxides seems to be much better than that of RTO ones. Another possible origin of the worse uniformity of RTO oxides is the nonuniform thermal stress caused by the heat sinking due to susceptor contacts and gas flow [11]. Although the ANO oxides are generally porous [8], the DAC-ANO oxides after proper RTA have the advantages of fewer pinholes

Fig. 4. The Weibull plots of TZDB characteristics for DAC-ANO and RTO oxides. The inset shows the Weibull plots of TDDDB characteristics of DAC-ANO and RTO oxides under stress field of -9 MV/cm.

Fig. 5. The J - V curves of DAC-ANO and RTO oxides before and after a constant field of -7 MV/cm for 200 s. The inset shows the J - V curves of DAC-ANO and RTO oxides before and after a constant field of -12 MV/cm for 200 s.

and better uniformity resulting from the self-compensation effect. Their reliability is therefore significantly enhanced.

Fig. 5 demonstrates the J - V curves of DAC-ANO and RTO oxides before and after constant electrical field stressing. The stress time is 200 s and the stress field is -7 MV/cm. According to the results shown in Fig. 5, the DAC-ANO oxide is much less leaky and the gate leakage current remains unchanged after stress. When the stress field increases to -12 MV/cm, the oxides exhibit a worse SILC phenomenon owing to the energetic electron injection as shown in the inset of Fig. 5. Fig. 6 shows the increment of gate leakage current after electrical stress

Fig. 6. $J(\text{stressed}) - J(\text{fresh})$ at $V_G = -2.5$ V versus stressed oxide field E_{ox} for DAC-ANO and RTO oxides.

versus stressed field ranging from -2 to -12 MV/cm. It is observed that the SILC increment of DAC-ANO oxides is less than that of RTO oxides, especially for high electrical field stress. Since the SILC occurs mainly due to the trap-assisted tunneling, it is suggested that there is less trap generation in DAC-ANO oxides than in RTO ones under the same electrical field. This verifies that the imperfect bonds in DAC-ANO oxides can be repaired by the $(OH)^-$ ions through the AC switching effect and the subsequent RTA treatment. The reduced SILC phenomenon of DAC-ANO oxides may be due to the presence of the Si-OH bond that stabilizes the structure of the obtained oxides [6].

Next, we focus on the charge trapping behavior during constant field stress. Fig. 7(a) shows the current variation for DAC-ANO 23 and 18 Å oxides under different stress fields. First, the gate current densities decrease with time for both 23 and 18 Å oxides at an electrical field of -5 MV/cm. The decreased current density implies that the tunneling current may introduce electron trapping under low field stress. In other words, electron trapping causes the effective barrier height to be higher, thus decreasing the current. Second, it is found that the gate current density in thicker oxide, i.e., 23 Å, increases at the field of -10 MV/cm. In such an electrical field, the electrons gain sufficient kinetic energy and suffer from collisions with atoms in the oxides, in which the traps are created. It is believed that the increased traps will enhance the trap-assisted tunneling current, which corresponds to a positive SILC behavior. But for the thinner oxides, the gate current still decreases due to the increased effective barrier height resulted from the generation and filling process of the neutral oxide traps [6]. According to the results of moderate electrical field stressing, electron trapping takes place in thinner DAC-ANO oxides rather than in thicker ones under the same stress field. This thickness dependence of SILC behavior

Fig. 7. The gate current variation $J(t) - J(0)$ versus stress time during different constant field stresses for (a) DAC-ANO 23 Å and DAC-ANO 18 Å oxides and (b) DAC-ANO 23 Å and RTO 23 Å oxides.

may mainly come from the longer tunneling path that contributes more collisions in thicker oxides. Finally, at a higher electrical field of -14 MV/cm, the tunnel electron gains enough energy to generate the electron–hole

pair in the bandgap and creates the “hot” hole in the valence band subsequently. These holes will be injected into the oxide by the electrical field to produce more traps within the oxide [12]. The trap-assisted tunneling current is therefore increased by more traps existing in the bulk oxide. It is believed that the trap generation dominates the SILC behavior under high field stress, and tunneling current introduces electron trapping under low field stress in the DAC-ANO oxides. Fig. 7(b) shows the charge trapping behavior of RTO oxides. At lower stress field of -5 MV/cm, the trapping behavior is the same as that for DAC-ANO ones. However, under higher stress fields (-10 and -14 MV/cm), the gate current densities and the current deviations in RTO oxides are both larger than those for DAC-ANO ones. It can be concluded from the SILC behavior that the traps are liable to form in RTO oxides than in DAC-ANO ones under the same electrical field stressing. The slighter oxide degradation of DAC-ANO oxides can be ascribed to the redistribution of anions caused by the AC switching effect to enhance its bonding structure. A summary of the above observations is shown in Table 1. As can be seen, the variation in gate leakage current of DAC-ANO oxides under low field stress is negative and quite small. Among oxides with different thickness, it is suggested that SILC events will carry out more easily in thicker oxides. For different fabrication processes, the SILC phenomenon is more serious in RTO oxides. According to the results shown in Table 1, the DAC-ANO oxides are more reliable than RTO ones.

4. Conclusion

In this work, the DAC-ANO technique is demonstrated for growing ultra-thin SiO_2 with precise controllability of the growth condition. The experimental results show that the DAC-ANO oxides exhibit lower

Table 1
SILC behavior of DAC-ANO and RTO oxides with different oxide thicknesses and under different stress fields

E_{STRESS} (MV/cm)	23 Å		SILC	18 Å		SILC
	J_{SILC} (A/cm ²)	ΔJ_G (A/cm ²)		J_{SILC} (A/cm ²)	ΔJ_G (A/cm ²)	
DAC						
–5	–0.06326	–0.0044	–	–0.02667	–0.0657	–
–10	0.34044	0.07955	+	–0.07111	–0.11555	–
–14	15.1	0.57777	+	4.79111	0.8	+
RTO						
–5	–0.00281	–0.0063	–			
–10	0.66669	0.4	+			
–14	9.45	1.01	+			

J_{SILC} is defined as $J(\text{stressed}) - J(\text{fresh})$ at $V_G = -2.5$ V and ΔJ_G is defined as $J(100 \text{ s}) - J(0)$ under constant field stress. The symbols +/– represent the increasing/decreasing of gate current density after electrical stress.

leakage current and improved breakdown endurance compared with RTO oxides. The SILC behavior of DAC-ANO and RTO oxides are also explored. The DAC-ANO oxides show better SILC behavior including less current variation and lower current level than RTO oxides. The less trap generation in DAC-ANO oxides implies that it is more stable under constant field stress than thermal oxides. The DAC-ANO oxides are candidates for the preparation of high reliable ultra-thin gate oxides.

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