Improved stability of deuterated amorphous silicon thin film transistors

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To improve the bias-induced degradation in hydrogenated amorphous silicon thin film transistor, the hydrogen in the amorphous silicon film should be replaced by deuterium. The stability of deuterated amorphous silicon thin film transistors, i.e., the shifts of threshold voltage and subthreshold swing, is indeed improved compared to that of the hydrogenated ones. This result is consistent with the improvement of the light-induced degradation in deuterated amorphous silicon films and this improvement can be explained by the efficient coupling between the Si–D wagging mode and the amorphous silicon phonon mode. © 1999 American Institute of Physics.
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I. INTRODUCTION

Thin film transistors (TFTs) have attracted wide attention in recent years because of their potential applications in many different areas.^{1–3} However, the most popular application of TFTs is to use them as the drivers in the active-matrix liquid crystal display (AMLCD). The active layer of the TFT is mainly made of either a hydrogenated amorphous silicon (*a*-Si:H) or polycrystalline silicon and the *a*-Si:H TFT still dominates the large area LCD market. The *a*-Si:H TFTs have a long-lasting problem constraining their usability, that is, they are unstable under bias stress. This instability comes from two sources: one is the charge trapping inside the insulating layer, i.e., silicon nitride (*a*-SiN_x:H) layer;⁴ and the other is the creation of metastable defects, i.e., silicon dangling bonds, in the *a*-Si:H active layer and at the *a*-Si:H/insulator interface.⁴ Therefore, it seems quite reasonable that we should improve the TFT stability by optimizing the silicon nitride quality and improving the *a*-Si:H structure to reduce the creation rate of Si dangling bonds. The creation of metastable defects in *a*-Si:H was known for a long time. In 1977, it was first observed that extended illumination of *a*-Si:H with visible light produced a serious decrease in photoconductivity (the Staebler–Wronski effect).⁵ This degradation became one of the most important topics in the studies of the *a*-Si:H materials. And it was found that the degradation was due to the increase of the metastable defects in the films. Also found was that the metastable defects could be created in the dark by charge injection (forward bias) or temperature stress.^{6–8} Therefore, if the degradation of the *a*-Si:H under illumination can be reduced, the degradation of *a*-Si:H TFT under bias may also be slowed down.

From 1990 to 1991, there were several reports^{9–11} showing that the incorporation of deuterium instead of hydrogen in amorphous silicon tended to slow down the decay of its photoconductivity. The improved stability in deuterated amorphous silicon (*a*-Si:D) was attributed to different structure grown by plasma enhanced chemical vapor deposition (PECVD), while the details of the microstructure change of *a*-Si:D films were not mentioned. In 1995, the hot electron degradation in Si metal–oxide–semiconductor field effect

transistors was found to be greatly reduced by passivating the Si/SiO₂ interface with deuterium instead of hydrogen.¹² In 1997, Sugiyama, Yang, and Guha¹³ demonstrated that an *a*-Si:D solar cell was more stable than an *a*-Si:H cell under normal operation. Our group also demonstrated that an *a*-Si:D film was more stable than an *a*-Si:H film under illumination and proposed a possible model¹⁴ which attributed the improvement to the highly efficient coupling between localized Si–D wagging modes ($\sim 510\text{ cm}^{-1}$) and extended Si–Si lattice vibration modes ($\sim 495\text{ cm}^{-1}$). The energy released from electron or hole capture at silicon dangling bonds causes localized vibrations of nearby Si–D bonds. The energy dissipates quickly to the background lattice and a higher recombination rate at local sites is required in deuterated *a*-Si than in hydrogenated amorphous silicon to accumulate enough energy to break the nearby weak bonds. Therefore, the *a*-Si:D film becomes more stable. Since the creation mechanism of metastable states in the channel region of *a*-Si:H or *a*-Si:D TFTs by hot electrons is similar to that in *a*-Si:H(D) films by illumination, it is expected that the *a*-Si:D TFT may also exhibit lower creation rate of metastable states in the channel and therefore, the degradation problem of the TFT can be improved. In this article, we demonstrate that the degradation of *a*-Si:D TFT is indeed slowed down.

II. EXPERIMENTS

Figure 1 displays the fabrication processes of amorphous silicon TFTs. The substrate used is Corning 7059 glass. First, the 80 nm Cr was evaporated on the glass substrate and the 50-nm-thick n^+ *a*-Si:H was deposited on the Cr as shown in Fig. 1(a). After deposition, the n^+ *a*-Si:H was etched by reactive ion etching (RIE) and the Cr metal was patterned by wet etching to form the source and drain contact pads, as shown in Fig. 1(b). Before removing the photoresist (PR), a liquid phase deposited silicon dioxide (PLD-SiO₂) was grown to planarize the surface.¹⁵ The preparation procedure of LPD-SiO₂ solution are described elsewhere.^{15,16} Samples were immersed in the growth solution to grow SiO₂ until the step between n^+ *a*-Si:H and glass substrate was filled up, as

FIG. 1. Flow chart of the TFT fabrication processes.

shown in Fig. 1(c). A 100 nm *a*-Si:H was deposited by PECVD after removing the PR as shown in Fig. 1(d). The *a*-Si:H layer was used as the active layer in the TFT. Then D₂ or H₂ plasma was used to treat the *a*-Si:H layer. The plasma treatment processes are as follows: The *a*-Si:H films were annealed at 550 °C in N₂ environment for 5 min to expel all the hydrogen atoms out of the films. Then the annealed films were treated separately by H₂ and D₂ plasma until their electrical properties (dark and photoconductivities) were recovered. The plasma treatment conditions are: substrate temperature 300 °C, chamber pressure 6 Torr, gas flow rate 3 sccm, power density 0.1 W/cm², rf frequency 13.56 Hz and the treatment time is 3 h. Three different active layers were prepared, i.e., the as-deposited *a*-Si:H, plasma treated (PT) *a*-Si:H, and PT *a*-Si:D. Then the active layers were mesa etched by RIE as shown in Fig. 1(e) to reduce the gate leakage current from gate electrodes to source/drain electrodes. The etching conditions are: CF₄ 36.5 sccm, O₂ 4 sccm, pressure 30 mTorr and the power density 0.4 W/cm². After etching, a 200 nm LPD SiO₂ was deposited at 50 °C and gate electrodes (Cr) were vacuum evaporated and patterned. The final TFT device structure was shown in Fig. 1(f). The current–voltage characteristics of the three types of TFTs were measured, their on/off current ratio, threshold voltage, subthreshold swing, etc., were extracted. Then the TFTs were stressed by varying the gate (V_{gs}) and drain (V_{ds}) bias from 0 to 40 V. The stress time was varied from 500 to 10 000 s. After stress, the changes of threshold voltage and subthreshold swing of the TFTs were recorded in order to find out the most stable devices.

III. RESULTS

The drain current (I_d) versus drain voltage (V_{ds}) characteristics of as-deposited *a*-Si:H, PT *a*-Si:H and PT *a*-Si:D TFTs are shown in Figs. 2(a), 2(b), and 2(c), respectively.

FIG. 2. Drain current (I_d) vs drain voltage (V_{ds}) characteristics of (a) as-deposited *a*-Si:H, (b) PT *a*-Si:H, and (c) PT *a*-Si:D TFTs before bias stress.

Apparently the *a*-Si:D TFT exhibits the highest drain current at the same gate and drain biases. The relations between square root of I_d and V_{ds} of the same TFT biased in the saturation region ($V_{gs} = V_{ds}$) are shown in Fig. 3(a). The field effect mobility evaluated from the slope are about 0.13, 0.14, and 0.20 cm²/V s for the as-deposited *a*-Si:H, PT *a*-Si:H, and PT *a*-Si:D TFTs, respectively. These are typical values for TFTs with SiO₂ as the gate insulator. The threshold voltages extracted from the intercept of V_{ds} axis are about 5.2, 4.3, and 3.8 V for the as-deposited *a*-Si:H, PT *a*-Si:H, and PT *a*-Si:D TFTs, respectively. Because the gate insulator LPD-SiO₂ is grown near the room temperature (50 °C), the defect state density inside the LPD-SiO₂ is probably larger than that in SiO₂ grown at high temperature. The threshold voltages of these TFTs are thus expected to be slightly higher than the value of a normal TFT. Figure 3(b) shows the transfer curve of these three TFTs with $V_{ds} = 10$ V, respectively. The on/off current ratio are about five orders of magnitude and the subthreshold swing is about 1.5 V/decade for these TFTs. These device parameters demonstrate that our TFTs have good quality even with SiO₂ as the gate insulator.

Then the stabilities of *a*-Si:H and *a*-Si:D TFTs were measured under five different bias stress conditions: (a) $V_{gs} = V_{ds} = 10$ V; (b) $V_{gs} = 10$ V, $V_{ds} = 20$ V; (c) $V_{gs} = V_{ds} = 20$ V; (d) $V_{gs} = 20$ V, $V_{ds} = 40$ V; and (e) gate electrode floating,

FIG. 3. (a) Relation between square root of I_d and gate bias (V_{gs}) and (b) transfer curves of as-deposited a -Si:H, PT a -Si:H, and PT a -Si:D TFTs with $V_{ds} = V_{gs}$.

$V_{ds} = 40$ V, respectively. The stress time varies from $t = 500$ to 10 000 s in seven steps. During the bias stress, the shifts of the threshold voltage (ΔV_T) and the subthreshold swing (ΔS) are extracted from the experimental data. They are divided into three categories, i.e., gate bias $V_{gs} = 20, 10$ and gate electrode floating, which shall be discussed in the following.

A. $V_{gs} = 20$ V and $V_{ds} = 20$ and 40 V

First, Figs. 4(a) and 4(b) replot the shifts of the threshold voltage and subthreshold swing of the as-deposited a -Si:H, PT a -Si:H, and PT a -Si:D TFTs, respectively, after $V_{gs} = V_{ds} = 20$ V stress for 500–10 000 s. After 10 000 s stress, the shifts of the threshold voltage of the as-deposited a -Si:H, PT a -Si:H, and PT a -Si:D TFTs are 6.94, 5.45, and 3.65 V, respectively. The voltage shift of a -Si:D TFT is the lowest. For the subthreshold swing, the shifts of the as-deposited a -Si:H, PT a -Si:H, and PT a -Si:D TFTs are 0.629, 1.10, and 0.512 V/decade, respectively. Again, the a -Si:D TFT has the lowest shift.

After the bias stress with $V_{gs} = 20$ V and $V_{ds} = 40$ V, the shifts of threshold voltage and subthreshold swing of the as-deposited a -Si:H, PT a -Si:H, and PT a -Si:D TFTs are shown in Figs. 5(a) and 5(b), respectively. The a -Si:D TFT also exhibits the lowest shifts both in threshold voltage and subthreshold swing. The values of the shifts after 10 000 s stress are listed in Table I, which shows that the shifts of both threshold voltage (ΔV_T) and subthreshold swing (ΔS) are reduced for the PT a -Si:H (ΔV_T from 5.45 to 4.68 V, ΔS from 1.1 to 0.823 V/decade) and the a -Si:D TFTs (ΔV_T from 3.65 to 3.22 V, ΔS from 0.513 to 0.43 V/decade) as the drain voltage (V_{ds}) increases from 20 to 40 V. But, on the con-

FIG. 4. (a) Threshold voltage and (b) subthreshold swing shifts of the as-deposited a -Si:H (■), PT a -Si:H (●), and a -Si:D (○) TFTs. The stress condition is $V_{gs} = 20$ V, $V_{ds} = 20$ V and the stress time varies from $t = 500$ to 10 000 s.

trary, both shifts (ΔV_T and ΔS) of the as-deposited a -Si:H TFT increase as the drain voltage increases (ΔV_T from 6.94 to 7.1 V, ΔS from 0.63 to 0.75 V/decade). This behavior will be discussed later.

B. $V_{gs} = 10$ V, $V_{ds} = 10$ and 20 V

Figures 6 and 7 show the shifts of the threshold voltage and the subthreshold swing, respectively, of the as-deposited a -Si:H, the PT a -Si:H, and the PT a -Si:D TFTs after 500–10 000 s stress. The stress conditions are $V_{gs} = 10$ V, $V_{ds} = 10$, and 20 V for Figs. 6 and 7, respectively. First, it is observed that the shift of the threshold voltage and the subthreshold swing are much smaller than in the previous case. Second, the a -Si:D TFT once again exhibits the lowest shifts of the threshold voltage and the subthreshold swing after 10 000 s stress. The values of the shifts after 10 000 s stress are summarized in Table I. From this table, we found that the shifts of both threshold voltage and subthreshold swing decrease for the PT a -Si:H (ΔV_T from 2.24 to 1.7 V, ΔS from 0.196 to 0.18 V/decade) and the a -Si:D TFTs (ΔV_T from 1.05 to 0.52 V, ΔS from 0.065 to 0 V/decade) as the drain voltage (V_{ds}) increases from 10 to 20 V. and again the as-deposited TFT exhibits the opposite (ΔV_T from 1.54 to 1.68 V, ΔS from 0.137 to 0.207 V/decade). These trends are similar to those described in Sec. III A and will be discussed later.

FIG. 5. (a) Threshold voltage and (b) subthreshold swing shifts of the as-deposited a-Si:H (■), PT a-Si:H (●), and a-Si:D (○) TFTs. The stress condition is $V_{gs} = 20$ V, $V_{ds} = 40$ V and the stress time varies from $t = 500$ to 10 000 s.

FIG. 6. (a) Threshold voltage and (b) subthreshold swing shifts of the as-deposited a-Si:H (■), PT a-Si:H (●), and a-Si:D (○) TFTs. The stress condition is $V_{gs} = 10$ V, $V_{ds} = 10$ V and the stress time varies from $t = 500$ to 10 000 s.

C. Gate electrode floating and $V_{ds} = 40$ V

Figures 8 and 8(b) show the shifts of the threshold voltage and the subthreshold swing, respectively, of the as-deposited a-Si:H, the PT a-Si:H, and the PT a-Si:D TFTs

after 500 to 10 000 s stress. The stress conditions are as follows: The gate electrode is floating and the $V_{ds} = 40$ V. The shifts of the threshold voltage of the as-deposited a-Si:H, the PT a-Si:H, and PT a-Si:D TFTs are 2.37, 2.40, and

TABLE I. The threshold voltage and subthreshold swing shifts of the as-deposited a-Si:H, PT a-Si:H, and PT a-Si:D TFTs after 10 000 s stress. The stress conditions are listed inside the table.

Stress conditions	As-deposited a-Si:H TFT		PT a-Si:H TFT		PT a-Si:D TFT	
	ΔV_T (V)	ΔS (V/decade)	ΔV_T (V)	ΔS (V/decade)	ΔV_T (V)	ΔS (V/decade)
$V_{gs} = 10$ V $V_{ds} = 10$ V	1.54	0.137	2.24	0.196	1.05	0.065
$V_{gs} = 10$ V $V_{ds} = 20$ V	1.68	0.207	1.7	0.18	0.52	~0
$V_{gs} = 20$ V $V_{ds} = 0$ V	9.22	0.325	...	...	5.87	0.3
$V_{gs} = 20$ V $V_{ds} = 20$ V	6.94	0.63	5.45	1.1	3.65	0.513
$V_{gs} = 20$ V $V_{ds} = 40$ V	7.1	0.75	4.68	0.823	3.22	0.43
$V_{gs} = -20$ V $V_{ds} = 0$ V	-4.03	0.1	...	...	-0.85	.05
Gate floating $V_{ds} = 40$ V	2.37	0.125	2.4	0.30	0.86	0.058

FIG. 7. (a) Threshold voltage and (b) subthreshold swing shifts of the as-deposited *a*-Si:H (■), PT *a*-Si:H (●), and *a*-Si:D (○) TFTs. The stress condition is $V_{gs} = 10$ V, $V_{ds} = 20$ V and the stress time varies from $t = 500$ to 10 000 s.

0.86 V, respectively. The shift of the *a*-Si:D TFT is still the lowest. For the subthreshold swing, the shifts are 0.125, 0.30, and 0.058 V/decade for the as-deposited *a*-Si:H, the PT *a*-Si:H, and the PT *a*-Si:D TFTs, respectively. The *a*-Si:D TFT shows the lowest shift again.

IV. DISCUSSION

In the *a*-Si:H(D) TFT, the shifts of the threshold voltage are due to the charges trapped inside the gate insulator and the interface states created by increasing the metastable states in the *a*-Si:H(D) layer.¹⁷ Experimental results show that the *a*-Si:D TFT has the lowest threshold voltage shift under five different stress conditions. Since the gate insulator (LPD-SiO₂) of these three TFTs are the same, their fabrication procedures are also the same. The improved stability of the *a*-Si:D TFT comes, therefore, from the lower metastable states created in the *a*-Si:D active layer. After the same stress time (10 000 s), the *a*-Si:D TFT also shows the smallest shift in subthreshold swing among three different samples. The shift of subthreshold swing is related to the density of defect states at the insulator/*a*-Si:H(D) interface by bias stress.^{18,19} Therefore, the experimental data indicates that the *a*-Si:D film is the most stable one under bias stress just like the case under light exposure.

In previous reports concerning the bias stress test,^{17,19} the drain bias V_{ds} is usually very small ($V_{ds} = 0.1$ V) or equals zero. In such stress conditions, the drain current (I_{ds})

FIG. 8. (a) Threshold voltage and (b) subthreshold swing shifts of the as-deposited *a*-Si:H (■), PT *a*-Si:H (●), and *a*-Si:D (○) TFTs. The gate electrode is floating, $V_{ds} = 40$ V and the stress time varies from $t = 500$ to 10 000 s.

is small and the effect due to carriers flowing in the channel region is also small. For example, the I_{ds} is at the system noise level ($\sim$ pA) when the as-deposited *a*-Si:H and the PT *a*-Si:H TFTs are in $V_{gs} = 20$ V and $V_{ds} = 0$ V stress conditions. But when $V_{gs} = 20$ V and $V_{ds} = 20$ or 40 V, the drain current I_{ds} is larger than 100 nA. Therefore, the effect of current flowing in the channel region should be considered. As the carriers flow in the *a*-Si:H(D) channel of the TFT, they can be injected into the gate insulator and trapped there by the defect states. The carriers can be also trapped by the pre-exist defect states near the *a*-Si:H(D)/SiO₂ interface and then the energy is released nonradiatively and converts to local vibration. As we proposed before,¹⁴ as the vibrational energy accumulates to a high level in a local region, the weak Si-Si bonds nearby can be broken up by this energy and more defect states are created. When more carriers flow in the channel region, the energy release through defect sites gets faster and more defects are created. The bias stresses at the drain or source terminals are different because of the large existing V_{ds} . In the stress conditions of $V_{gs} = 20$ V and $V_{ds} = 0$ V, the gate biases across drain or source terminals are equal to 20 V. But at the same gate bias stress condition, $V_{gs} = V_{ds} = 20$ V, the gate bias at the source terminal is still equal to 20 V, while the gate bias at the drain terminal is equal to 0 V. Then less charges are injected from the channel region near the drain terminal into the gate insulator and trapped there. Therefore, the total trapped charges in the in-

FIG. 9. (a) Threshold voltage and (b) subthreshold swing shifts of the as-deposited *a*-Si:H (■) and *a*-Si:D (○) TFTs. The stress condition is $V_{gs} = 20$ V, and $V_{ds} = 0$ V. The stress time varies from $t = 500$ to 10 000 s.

ulator becomes less and the ΔV_T becomes smaller.

In Table I, it is observed that the shifts of the threshold voltage ΔV_T and the subthreshold swing ΔS exhibit two opposite trends as V_{ds} increases from 20 to 40 V. The threshold voltage shifts ΔV_T drop about 0.77 and 0.43 V for the PT *a*-Si:H and *a*-Si:D TFTs, respectively, approximately 16.5% and 13.4% of the original values. The subthreshold swing shifts ΔS also drop about 0.27 and 0.084 V/decade, approximately 24.3% and 16.3% of the original values, for the PT *a*-Si:H and the *a*-Si:D TFT, respectively. For the as-deposited TFT, however, the threshold voltage shift increases about 0.16 V (2.3%) and the subthreshold swing shift increases approximately 0.12 V/decade (19%). In the PT *a*-Si:H and *a*-Si:D TFT, the changes of ΔV_T and ΔS are both evident (13% to 25%) while the as-deposited TFT exhibits a small change of ΔV_T (2.3%) but a larger change of ΔS (19%). We will propose a mechanism to explain these differences. As the V_{ds} increases from 20 to 40 V (V_{gs} is fixed at 20 V), the bias distribution across the oxide changes from $V_{gs} = 20$, $V_{gd} = 0$ V to $V_{gs} = 20$, $V_{gd} = -20$ V, where the V_{gd} represents the gate-drain bias. The gate-drain bias decreases from 0 to -20 V, but the channel bias increases from 20 to 40 V. In order to distinguish how these bias changes affect the stress results, both the source and drain electrodes are connected to the ground ($V_{ds} = 0$ V), and the gate bias is chosen either 20 or -20 V. After 10 000 s stress, the results are shown in Figs. 9 and 10 and Table I. They demonstrate that the threshold voltage increases after positive gate bias

FIG. 10. (a) Threshold voltage and (b) subthreshold swing shifts of the as-deposited *a*-Si:H (■) and *a*-Si:D (○) TFTs. The stress condition is $V_{gs} = -20$ V, $V_{ds} = 0$ V. The stress time varies from $t = 500$ to 10 000 s.

and decreases after negative gate bias. The subthreshold swing, however, increases no matter how the gate bias changes.

Now the results of stress measurement from $V_{ds} = 0$, 20 to 40 V with $V_{gs} = 20$ V can be explained. At $V_{ds} = 0$ V, the degradation due to the channel current is zero. The ΔV_T and ΔS are 9.22 V and 0.325 V/decade for the as-deposited *a*-Si:H TFT, 5.89 V and 0.299 V/decade for the PT *a*-Si:D TFT, respectively. The shift of ΔV_T is high, but the shift of ΔS is low. It means that the dominating mechanism of the degradation is the injection of electrons into the SiO_2 layer and being trapped there. Small amount of defects are also created by electron injection. The injected electrons near the interface form the interface states, which in turn degrade the subthreshold swing. As the V_{ds} increases from 0 to 20 V, the gate-drain bias is reduced from 20 to 0 V and the injection of electron from drain into the SiO_2 is minimized. The degradation becomes less and the ΔV_T decreases. But at the same time, the V_{ds} increases from 0 to 20 V and the drain current increases rapidly from 0 to above 100 nA. The effect of channel current becomes evident. It tends to increase both the ΔV_T and ΔS . Over all, the net ΔV_T decreases about 25%–35% and the ΔS increases about 77%–93% for both the as-deposited *a*-Si:H and the PT *a*-Si:D TFTs. In order to understand how the change of the charges trapped in insulator and that of the defect state density at the SiO_2/Si interface affects, the charge concentrations of both are calculated. From the literature,²⁰ the threshold voltage shift ΔV_T is in

FIG. 11. Densities of the trapped charges and the defect states in the as-deposited *a*-Si:H (●) and PT *a*-Si:D TFTs (○). The V_{gs} is 20 V and the V_{ds} varies from 0, 20 to 40 V and the stress time is 10 000 s.

proportion to the density of trapped charge in the insulator which is given by

$$N_T = \frac{\Delta V_T C_i}{q}, \quad (1)$$

where C_i is the gate insulator capacitance per unit area, q is the electron charge and N_T is the density of trapped charge ($1/\text{cm}^2$) in the insulator. For the defect state density at the SiO_2/Si interface, assuming a constant defect density distribution of N_0 , the relation between N_0 and subthreshold swings is¹⁹

$$S = \ln(10) \frac{kT}{q} \left(1 + \frac{q}{C_i} \sqrt{N_0 \epsilon_s} \right), \quad (2)$$

where k is the Boltzmann constant, T is the temperature and ϵ_s is the dielectric constant of *a*-Si:H(D). From the change of subthreshold swing, the defect density is calculated. And the concentrations of trapped charge and defect states are shown in Fig. 11. As V_{ds} increases from 0 to 20 V, the concentrations of the trapped charges are reduced but those of the interface states are increased in both the as-deposited *a*-Si:H and the PT *a*-Si:D TFTs.

As V_{ds} further increases to 40 V, the voltage across oxide at drain terminal changes from 0 to -20 V. The gate bias stress near drain terminal becomes negative, which results in less total negative trapped charges in oxide and the ΔV_T decreases. Therefore, the effective gate bias stress is reduced. On the other hand, the drain current only increases slightly as the V_{ds} is raised from 20 to 40 V which is different from the case when V_{ds} increases from 0 to 20 V, and the degradation due to channel current changes a little. When the gate electrode is floating and V_{ds} is set to 40 V, the gate is charged up 3–5 V and the drain current is only 0.1–5 nA. At this low-induced gate bias, the V_{gs} and V_{gd} are about 5 and -35 V, respectively. The net effective gate bias is approximate zero

at the source end or negative at drain end. Therefore, the ΔV_T becomes negative, similar to the results of Fig. 10. But in this case, the channel current exists and ΔV_T and ΔS due to the flow of the current are positive. Combining the above two opposite effects, ΔV_T and ΔS as listed in Table I turn out to be small, i.e., 0.86 V and 0.06 V/decade for the PT *a*-Si:D TFT, 2.4 V and 0.3 V/decade for the as-deposited *a*-Si:H TFT. In stress conditions under floating gate, we found that the shifts of the threshold voltage and the subthreshold swing are mainly due to the channel current rather than the gate bias. The degradation of the as-deposited *a*-Si:H TFT is larger than that of the PT *a*-Si:D, but its flow of drain current is smaller. This indicates that the *a*-Si:H channel is less stable than the *a*-Si:D channel. Probably, the LPD- SiO_2 quality is also better when deposited on the PT *a*-Si:D channel which has a denser structure.

As the V_{ds} increases from 20 to 40 V, the channel current I_{ds} increases about 10% but ΔV_T and ΔS due to ΔI_{ds} increase very slightly. At the same times, the gate effective bias is reduced and ΔV_T and ΔS decrease. Taking these two factors together, both ΔV_T and ΔS are reduced by 13% and 16%. In the as-deposited *a*-Si:H TFT, both the LPD- SiO_2 and the *a*-Si:H channel have poorer qualities. As the V_{ds} increases from 20 to 40 V, the gate effective bias is reduced and ΔV_T and ΔS decrease. At the same time, the I_{ds} increases about 10% as shown in Fig. 2(a). Because the quality of the *a*-Si:H TFT is poorer, the degradation due to ΔI_{ds} may be much larger and the increases of ΔV_T and ΔS be more than the decreases due to the small effective gate bias. The net degradation results in an increase of ΔV_T and ΔS about 2.3% and 19%, respectively. The results shown in Sec. III B are similar to those shown in Sec. III A. The same reasoning can be applied to explain the results.

V. CONCLUSIONS

A good quality *a*-Si:D TFT fabricated by plasma treatment method is demonstrated. The threshold voltage is 3.8 V, the field effect mobility at the saturation region is $0.16 \text{ cm}^2/\text{Vs}$, the on/off current ratio is about five orders of magnitude and the subthreshold swing is 1.5 V/decade. From measurement of different stress conditions, it is found that the PT *a*-Si:D TFT is much more stable compared to the as-deposited and PT *a*-Si:H TFTs. The stability of amorphous silicon TFT can indeed be improved by using deuterium atoms in place of hydrogen ones. This is consistent with the conclusions of the light-induced degradation in our previous article.¹⁴ Finally, as the V_{ds} increases from 0 to 20 V, the effective gate bias across oxide near the drain terminal is reduced and the threshold voltage shift is reduced but the subthreshold swing shift is increased. It means that the subthreshold swing is changed by the creation of the interface states which depend on the magnitude of the drain current. As the V_{ds} increases from 20 to 40 V, the effective gate bias reduces further but ΔV_T and ΔS due to ΔI_{ds} increases very slightly in the PT *a*-Si:H and the *a*-Si:D TFTs. The net effect is that ΔV_T and ΔS are decreased by 13% and 16%, respectively. The as-deposited *a*-Si:H TFT has the poorest qualities of the LPD- SiO_2 and the *a*-Si:H channel. As the V_{ds} in-

creases from 20 to 40 V, the degradation due to ΔI_{ds} is much larger and the increases of ΔV_T and ΔS are bigger than the decreases due to changes of effective gate bias. The net degradation results in an increase of ΔV_T and ΔS about 2.3% and 19%, respectively.

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