Enhanced thermally induced stress effect on an ultrathin gate oxide

Jiann-Liang Su, Chao-Chi Hong, and Jenn-Gwo Hwu^{a)}

Room 446, Department of Electrical Engineering/Graduate Institute of Electronics Engineering,
National Taiwan University, Taipei, Taiwan 106, Republic of China

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The effects of thermal stress on the electrical characteristics of metal–oxide–semiconductor diodes with oxides in an ultrathin regime were studied. By centering a quartz ring as a heat sink beneath the silicon wafer, the introduced temperature gradient results in a corresponding hat-like shape thickness distribution for an oxide grown on the wafer with a rapid thermal processing system. The enhanced exterior tensile and compressive thermal stresses due to introduced temperature gradient make the oxides exhibit less and more substrate injection saturation current J_{sat} , respectively, in comparison to control oxides. Their flatband voltage V_{FB} data also clearly show the dependency of effective charge number density N_{eff} on exterior thermal stress. A stress distribution model is proposed to explain the observation. Co-60 irradiation was also performed on the stressed samples to observe this stress extent by examining the variation of electrical characteristics. It was found that an oxide grown on a wafer in exterior compression exhibited better radiation hardness than one in tension. © 2002 American Institute of Physics. [DOI: 10.1063/1.1452763]

I. INTRODUCTION

Rapid thermal processing (RTP) is known to be very useful for its ability to heat and cool silicon wafers quickly within relatively low thermal budgets. However, temperature nonuniformity in the wafer is a critical issue for RTP because it induces problems associated with thermoplastic stress, such as wafer warpage and slip dislocation.¹ Recent work has shown that the methodologies of complementary metal–oxide–semiconductor (CMOS) device isolation, such as shallow trench isolation or the local oxidation of silicon technique, are useful in defining silicon on insulator transistors. In this kind of process, the stress that the device undergoes during forming the isolation region is of interest. The increased strain in the silicon oxide is attributed to the volume expansion of grown silicon oxide beneath the aluminum gate electrode. As devices are scaled down, an oxide thickness under 20 Å is essential for state-of-the-art CMOS technology, and the thermal stress effect on the ultrathin gate oxide is more important than before. Thus, it is important to determine the intrinsic physical stress inside the film. The reported main methods for detecting process-induced intrinsic stress are x-ray diffraction and Raman microscopy.^{2,3} Although much work has been done to study the thermal expansion stress in the oxide layer, little is known about the oxidation-induced stress effect on the silicon substrate during RTP.⁴ Moreover, process-induced stress could be caused by the generation of silicon oxide from the consumption of silicon atoms.^{5,6} It is believed that the oxidation-induced stress resulting from the differential growing volume of silicon oxides due to temperature nonuniformity will become more important for a high temperature RTP system compared to the typical mechanical stress resulting from the difference of thermal expansion coefficients.

In this work, we design a special wafer susceptor to grow oxides under thermal stress, and both exterior tensile and compressive stresses are simultaneously introduced to enhance the effect of thermal stress. The electrical properties of both silicon oxide and substrate were observed to be affected by the above stresses. It is noted that there are many approaches to studying the changes of the properties for metal–oxide–semiconductors (MOS) structures due to irradiation.^{7–9} It is known that interface trap generation is a consequence of the propagation of the radiation-induced bonding defects under the bond strain gradient. Furthermore, the oxidation process accounts for the magnitude of such a gradient, which is related to the observed dependencies of the radiation sensitivity.¹⁰ Thus, radiation seems to be an effective way to determine the extent of stress within the MOS structure. The stressed samples in this work were also subjected to receive Co-60 irradiation, and an interesting observation of the radiation hardness behavior for an exteriorly compressed sample is shown. A possible reason for the radiation hardness behavior of stressed samples is given.

II. EXPERIMENTS

The devices used in this work are MOS capacitors with aluminum gate electrodes fabricated on 3 in., (100), *p*-type substrates with a resistivity of 1–5 Ω cm. The MOS capacitor size is 150 by 150 μm². In this work, a special wafer susceptor, as shown in Fig. 1(a), was designed to grow silicon oxide by centering a 2 in. quartz ring beneath the wafer in the RTP system. The heat is sunk through the 2 in. quartz ring which acts as a heat conduction medium. By this approach, the temperature gradient introduces different oxide growth rate and generates a corresponding hat-like oxide thickness profile. The measured maximum and minimum oxide thicknesses are 25–12 Å, respectively. This process results in a thinner grown oxide at a contact superficial area and generates different thermal-induced stresses within the

^{a)} Author to whom correspondence should be addressed; electronic mail: hwu@cc.ee.ntu.edu.tw

FIG. 1. (a) Oxide thickness profile of a 3 in. wafer oxidized in RTP with a 2 in. quartz ring centered beneath it. (b) J - V characteristics of oxides at three different points grown with the special wafer susceptor.

wafer. It is noted that no postoxidation annealing was carried out to preserve the stress related information within samples.

In this work, a laser ellipsometer was used to measure the thickness of silicon oxide with a refractive index of 1.46. For the electrical characterizations of RTP oxides, the current-voltage (I - V) curves were measured by using a picoamp meter and voltage-current measurement unit. The high-frequency capacitance-voltage (HFCV) measurements were performed with a 1 MHz capacitance meter. A picoamp meter was also used for the time-zero-dielectric breakdown (TZDB) measurement. Following the oxidation and initial electrical measurement, all samples were exposed to the Co-60 γ rays with a total dose of 1 Mrad (SiO_2). All the samples had been floating in a wafer box for at least 48 h before the postirradiation measurements.

The flatband voltages V_{FB} of MOS capacitors can be calculated from the HFCV curves. Substrate injection saturation current density J_{sat} was measured under the positive gate voltage V_G . For convenience, we choose the J_{sat} at $V_G = 7$ V for comparison among samples. TZDB was measured by the I - V characteristic, starting from gate voltage $V_G = 0$ V with a ramp rate of -0.1 V/s. The breakdown current was set to be 5×10^{-5} A. A gate current that had a sharp increase and exceeded the above current level was identified as breakdown and the breakdown voltage V_{BD} was obtained.

FIG. 2. Oxide thickness, substrate injection saturation current density J_{sat} at $V_G = 7$ V, and flatband voltage V_{FB} distributions of MOS capacitors located at an investigated path as shown in Fig. 1.

III. RESULTS AND DISCUSSION

A. Thermal-induced compressive and tensile stresses

In Fig. 1(a) we described the special susceptor used to grow oxide and obtained the hat shaped oxide thickness profile. However, there are distinct current density-voltage (J - V) behaviors between different points located at different stressed areas. Figure 1(b) shows three J - V curves of points A, B, and C, as indicated in Fig. 1(a). Points A and C are of the same thinner thickness, and exhibit higher gate injection current density J_G under negative V_G but lower J_{sat} under positive V_G than point B, which has a thicker oxide. It is reasonable that a thinner oxide should appear a larger J_G . However for J_{sat} behavior, it is noteworthy that current saturation occurs without breakdown for ultrathin oxides (< 24 Å) and that a thinner oxide has a lower J_{sat} .

Now we examine the thermal-stressed samples as shown in Fig. 1(a). By investigating along a wafer diameter indicated in Fig. 1(a), we can see from Fig. 2 that both J_{sat} and V_{FB} values follow the thickness profile. However the lowering of J_{sat} for the thin gate oxide regions is not only due to the thickness factor. Some stress exists in these stressed samples. More so essential experiments were performed in this work to prove this hypothesis.

For comparison with the stressed samples, we also grew control samples, i.e., without a quartz ring, with various oxide thicknesses for reference. Their J - V curves are shown in Fig. 3. Clearly, J_{sat} increases with oxide thickness. It is known that the J_{sat} in a thin MOS device is dependent on several parameters.¹¹ Furthermore, it is probable that a thicker oxide will consume a larger volume of silicon, which may contribute to the larger interface trap and bulk trap densities. These larger trap densities are responsible for the increased J_{sat} behavior as observed above. Another possible reason for the saturation behavior is that when SiO_x is formed on the silicon substrate, the lattice type and spacing of silicon are redistributed and hence induce change in the silicon band gap E_g . The J_{sat} of an MOS structure is controlled by the generation of minority carriers in the depletion region and by the surface generation along the Si/SiO₂ inter-

FIG. 3. J - V curves of control samples with various oxide thicknesses.

face rather than in the silicon oxide layer. It has been reported that the generation current components are exponentially dependent on thermal stress, primarily through the change of intrinsic carrier concentration n_i .¹² A change of silicon E_g will change the n_i and therefore the J_{sat} level.

A comparison of J_{sat} behaviors between stressed and control samples are shown in Fig. 4, which indicates a significant result. In the regions of oxide thickness under 18 Å, the average J_{sat} of the stressed samples is smaller than the control samples with the same oxide thickness. But in the region of oxide thickness above 18 Å, the opposite is observed. According to the compressive stress-induced band gap narrowing model as proposed by Smeys *et al.*,¹² the J_{sat} is mainly related to the generation current in the depletion region which is exponentially dependent on silicon E_g . The silicon substrate is inherently tensile stressed by the oxide layer due to volume expansion. Thus, if there is an exterior tensile stress on silicon substrate, i.e., the net tensile stress that silicon sustains increases, then the silicon E_g will be enlarged. This reduces the n_i value and therefore the J_{sat} . On the contrary, an exterior compressive stress on the silicon substrate reduces the inherent and hence the net tensile stress

FIG. 4. Substrate injection saturation density J_{sat} at $V_G = 7$ V vs oxide thickness of stressed and control samples. FIG. 5. Gate injection current density J_G at $V_G = -3$ V vs oxide thickness of stressed and control samples.

sustained by the silicon substrate, as well as its E_g , and therefore increases the n_i value and the J_{sat} . Beyond this we can suppose that in the stressed sample the substrate regions of oxide thickness under 18 Å sustain exterior tensile stress, while those above 18 Å sustain exterior compressive stress. The detailed stress distribution model will be described later. Clearly the J_{sat} behavior differs between stressed and control samples.

Figure 5 shows the comparison of J_G between stressed and control samples. It is noticed that the J_G under negative V_G for these two sets of samples do not have a significant difference. This observation is consistent with the previous report that the stress-induced effect on the silicon oxide is not as serious as on the silicon substrate.¹³ For positive V_G , the J_{sat} changes severely because substrate injection is related not only to the silicon oxide but also to the physics of the Si/SiO₂ interface, such as the n_i value and silicon substrate stress, etc.

Additionally, from the viewpoint of oxide quality, we also measured the V_{FB} and calculated effective charge density N_{eff} for stressed MOS capacitors using the HFCV method, as shown in Figs. 6(a) and 6(b), respectively. The absolute values for V_{FB} of control samples increase as oxide thickness decreases. By comparing with the ideal value of V_{FB} , i.e., -0.9 V, the positive N_{eff} in oxide increases as oxide thickness decreases in control samples. It was suggested that the thinner the oxide, the more the portion that the transition layer from Si to SiO₂ occupies, thus resulting in larger N_{eff} . To our surprise, the V_{FB} for the stressed sample decreases rapidly as thickness decreases, which is quite different from that of control oxides. At the same time, the amounts of N_{eff} for stressed samples in thick regions are larger than those for control ones, while those in thin regions are smaller. Generally, it is known that a large additional stress will increase silicon lattice distortion and induce more charge in the oxide layer near the silicon substrate.¹⁴ But the extent of damage depends on whether the stress is compressive or tensile. It is also important to note that a normal oxidation process will introduce intrinsic tensile stress in a silicon substrate and compressive stress in silicon oxide, due

FIG. 6. Comparisons of: (a) the flatband voltage V_{FB} and (b) the effective charge number density N_{eff} vs oxide thickness of control and stressed samples.

to the volume expansion. Figures 6(a) and 6(b) indicate that the increase of N_{eff} for stressed samples in the thicker oxide regions might be due to the exteriorly enhanced lattice mismatch between SiO_2 and Si since the substrate has exterior compressive stress. The increased N_{eff} produces a larger value for V_{FB} than normal control oxide. On the contrary, a decrease of N_{eff} in thinner oxides for stressed samples implies that there is a reduction of lattice mismatch between SiO_2 and Si since the substrate now has exterior tensile stress. The decrease of N_{eff} produces a lower V_{FB} value than the normal control sample. TZDB voltages for the stressed and control samples are shown in Fig. 7, which also shows that the stressed samples on thinner oxide regions have lower breakdown voltages because of smaller negative V_{FB} values. Similarly, the stressed samples on thicker oxide regions have higher breakdown voltages than control samples because of their larger negative V_{FB} values.

Because of the temperature gradient, the oxide growth rates of the regions touching the quartz ring are slower than the remaining ones. Since heat is sunk through the quartz interface, the temperature gradient and different growth rate generate a hat-like oxide thickness profile above the silicon wafer. Since the silicon oxide is composed of oxygen and silicon elements, the thicker oxide regions consume more silicon atoms from the silicon substrate than do thinner ones.

FIG. 7. Gate injection TZDB voltage V_{BD} vs oxide thickness of control and stressed samples.

It is reasonable to speculate that the oxide thickness profile is convex and hence the underneath silicon substrate is concave-like in the thicker oxide region. We propose a model as shown in Fig. 8 to illustrate stress distribution between silicon oxide and silicon substrate for this special oxidation process and use this model as an approach to explain the experimental observation.

As shown in Fig. 8, in this model the different growth rates induce compressive and tensile oxidation-induced exterior stresses on the Si/SiO₂ interface. Thicker gate oxide regions show a higher exterior compressive stress on the silicon substrate because the concave interface implies that more elastic deformation is being imposed upon the underlying silicon substrate. Hence the silicon E_g narrows, and its n_i value increases. Thus the thicker oxide regions exhibit larger J_{sat} than conventional control samples of the same oxide thickness, as shown in Fig. 4. The reduction of J_{sat} in thinner oxide regions can also be explained by this model, and the J_{sat} behavior in Fig. 4 supports this model. Furthermore, the N_{eff} and the V_{FB} data in Figs. 6(a) and 6(b), and also the TZDB plot of Fig. 7 are all consistent with the

FIG. 8. The thermal-induced stress hypothetical model. The growth rate is slower at the contact superficial area, thus inducing less silicon to be consumed. The untouched area has a fast oxide growth rate thus bringing an exterior compressive stress to the corresponding center portion of the silicon substrate.

FIG. 9. Substrate injection saturation current density J_{sat} at $V_G = 7$ V vs oxide thickness of the stressed samples before and after radiation. The inset shows the positive J - V behaviors of the stressed sample with an oxide thickness of 16 Å before and after radiation.

model, as discussed earlier. The thermally induced stress seems truly important to the Si/SiO₂ interface property and contributes considerable influence to the electrical property of ultrathin oxides.

According to the calculations in previous papers, it has been shown that for typical stress values in integrated circuit processing, a change in the band gap of approximately 0.1 meV/MPa is achievable under external stress.¹⁵ Comparing our experimental observation in Fig. 4, we extracted the maximum value of the J_{sat} difference of stressed and control samples, and found that there was approximately a 90 meV reduction in the magnitude of silicon E_g . Hence we may expect that there is about 900 MPa of stress in the most heavily stressed region, a value that is comparable with those discussed in previous articles.^{12,15} The proposed model helps to find a general estimation of stress from the J_{sat} magnitude. It is probable that this model is useful in oxide engineering and that one can better understand the background of the silicon stress.

B. Co-60 irradiation effect under physical stress

Stressed samples in this work were irradiated by a Co-60 irradiator with a total dose of 1 Mrad at room temperature. No bias was applied to the sample during the radiation period. Figure 9 shows the J_{sat} behaviors of the stressed samples before and after radiation. From the inset of Fig. 9, it can be seen that for 16 Å, the J_{sat} increases by more than 3 orders of magnitude for the stressed sample due to radiation. This is because of the increased amount of bulk trap inside the stressed silicon substrate after radiation. In addition, the radiation effects on the thermal-stressed wafer are more severe in thinner oxide regions. On the other hand, when oxide thickness of the stressed samples increases, the J_{sat} increment due to irradiation decreases. This result is consistent with the previous research results of Shaw *et al.*¹⁶ Increased exterior compressive stress in the silicon substrate will reduce the total net (tensile) stress, which results in less radiation damage in the device. The exterior compressive stress in the

FIG. 10. Gate injection current density J_G at $V_G = -3$ V vs oxide thickness of the stressed samples before and after radiation. The inset shows the negative J - V behavior of the stressed sample with an oxide thickness of 16 Å before and after radiation.

silicon substrate under a thicker oxide region enhanced the lattice mismatch, which resulted in a large initial fixed oxide charge density Q_f , but released the strained bondings. A smaller amount of strained bonds should exhibit better radiation hardness according to the bond strain gradient model.¹⁷⁻¹⁹ Nevertheless, increase of exterior compressive stress or decrease of total tensile stress in a silicon substrate is a possible way to approach the radiation hardness.

Figure 10 shows the J_G at negative V_G of -3 V versus oxide thickness for stressed samples both before and after radiation. It is observed that all the J_G are obviously reduced after radiation for the stressed samples. Figure 11 shows the V_{FB} versus oxide thickness for stressed samples before and after radiation. Similarly, a thicker oxide exhibits better radiation hardness in J_G and V_{FB} shifts for the same reason as above.

IV. CONCLUSION

In this article, it is observed that the substrate injection saturation current density J_{sat} is strongly related to the com-

FIG. 11. The flatband voltages V_{FB} vs oxide thickness for the stressed samples before and after radiation.

pressive or tensile stress in the silicon substrate, which is exteriorly induced by a small modification of the wafer susceptor in the oxidation process. The examination of J_{sat} proves to be a useful tool to study the Si/SiO₂ interface property. By investigating the variation of electrical characteristics, we can determine how both the oxide thickness and physical stress in the silicon substrate affect the J_{sat} . A cross-section model considering the oxidation-induced stress is proposed to explain the J_{sat} mechanism and other electrical characteristics. A silicon band gap varying model is also adopted to explain the stress effect on J_{sat} behavior. It is concluded that exterior tensile (compressive) stress reduces (increases) the J_{sat} . Also, the V_{FB} , N_{eff} , and TZDB data show that exterior compressive stress on the substrate enlarges its lattice mismatch, and therefore introduces more N_{eff} at the Si/SiO₂ interface. This assumption is also clarified further by Co-60 irradiation from the viewpoint of stress-related radiation damage. The thermal-induced stress is of importance to the reliability of ultrathin gate oxides.

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- ¹K. C. Lee, H. Y. Chang, H. Chang, J. G. Hwu, and T. S. Wung, IEEE Trans. Semicond. Manuf. **12**, 340 (1999).
- ²Y. Guo, D. Mitchell, V. Sarihan, T. Y. T. Lee, and D. Zheng, IEEE Trans. Compon. Packag. Manuf. Technol. **23**, 388 (2000).
- ³K. F. Dombrowski *et al.*, Tech. Dig. - Int. Electron Devices Meet. **1999**, 357.
- ⁴A. Hamada, T. Fursawa, N. Saito, and E. Takeda, IEEE Trans. Electron Devices **38**, 895 (1991).
- ⁵B. S. H. Royce, IEEE Trans. Compon., Hybrids, Manuf. Technol. **11**, 454 (1988).
- ⁶B. Mohadjeri, M. R. Baklanov, E. Kondoh, and K. Maex, J. Appl. Phys. **83**, 3614 (1998).
- ⁷C. Codrescu, E. Iliescu, A. Badoiu, and M. Drafan, *Semiconductor Conference, CAS '99 Proceedings*, 1999, p. 239.
- ⁸W. Chen and T. P. Ma, J. Appl. Phys. **70**, 860 (1991).
- ⁹L. Vishnubhotla and T. P. Ma, J. Appl. Phys. **71**, 1058 (1992).
- ¹⁰V. Zekeriya and T.-P. Ma, J. Appl. Phys. **56**, 1017 (1984).
- ¹¹E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 1982).
- ¹²P. Smeys, P. B. Griffin, Z. U. Rek, I. D. Wolf, and K. C. Saraswat, IEEE Trans. Electron Devices **46**, 1245 (1999).
- ¹³J. W. Sleight, C. Lin, and G. J. Grula, IEEE Electron Device Lett. **20**, 248 (1999).
- ¹⁴C. Monserie, C. Papadas, G. Ghibaudo, C. Gounelle, P. Mortini, and G. Pananakakis, *31st Annual Proceedings of the International Reliability Physics Symposium*, 1993, p. 280.
- ¹⁵P. Smeys, P. B. Griffin, Z. U. Rek, I. D. Wolf, and K. C. Saraswat, Tech. Dig. Int. Electron Devices Meet. **1996**, 709.
- ¹⁶D. C. Shaw, L. Lowry, K. P. MacWilliams, and C. E. Barnes, IEEE Trans. Nucl. Sci. **39**, 2146 (1992).
- ¹⁷W. Chen and T.-P. Ma, J. Appl. Phys. **70**, 860 (1991).
- ¹⁸L. Vishnubhotla and T. P. Ma, J. Appl. Phys. **71**, 1058 (1992).
- ¹⁹V. Zekeriya and T.-P. Ma, J. Appl. Phys. **56**, 1017 (1984).