Degradation in metal-oxide-semiconductor structure with ultrathin gate oxide due to external compressive stress

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The effect of external stress on metal-oxide-semiconductor (MOS) structure with ultrathin gate oxide (~ 1.5 nm) was studied. J - V characteristics of fresh and stressed samples revealed that the tensile stress had little effect on J - V curves, whereas the compressive stress obviously increased the leakage current by about several hundred in percentages with respect to the fresh sample, in both positive and negative gate biases. This increase in leakage current was suggested to be attributed to the increase of interface states and silicon bulk traps under external compressive stress in the MOS device with an inherent tensile stressed silicon. In addition, we also found that once the device was damaged by the previously applied compressive stress, the second applied compressive stress of the same magnitude would not create more damage unless the device was breakdown. © 2001 American Institute of Physics. [DOI: 10.1063/1.1420491]

Metal-oxide-semiconductor (MOS) is the most important building structure in the ultra-large-scaled-integrated (ULSI) circuits. Since the integrated-circuit (IC) concept was originally described by Kilby in 1959, this technology has been greatly improved in 40 years and the packaging density of IC devices has increased for more than six orders of magnitude. As the device channel length scaled down to the deep subquartermicroregion, an effective gate oxide thickness below 3 nm is required,¹ and the leakage current of gate oxide becomes a major problem because too high gate leakage current will cause the device to operate improperly. Thus, many theories have been proposed to identify the current transport physics.²⁻⁵ In addition, various methods had been investigated to reduce the leakage current, such as H_2 baking,⁶ using oxynitride gate dielectrics,⁷ etc.

Mechanical stress-related problems have also become a key issue for the semiconductor process. It was noted that during oxide growth the tensile stress would enhance oxidation rate.⁸ The capacitance of a dielectric film changed when external stress was applied during measurement.⁹ Devices adjacent to film step or interconnection edges exhibited high stress and degradation of leakage current occurred.¹⁰ Internal stress in bulk silicon also has been shown to affect device performance.¹¹ The stress induced in local-oxidation-of-silicon (LOCOS) used for device isolation creates more silicon bulk traps and new leakage current components,^{12,13} even though the luminescence characteristics of compound semiconductors are affected by mechanical stress.¹⁴ However, the effect of mechanical stress on chips which have MOS structure on them has not yet been studied. Thus, in this work, external tensile and compressive stresses were applied to chips with MOS capacitors on them. After the release of stress, J - V curves under negative and positive biases were used to clarify the change in oxide and silicon due

to the external stress. Some very noteworthy experimental results were observed.

p -type 3-in.-(100) silicon wafers were oxidized in a rapid thermal processor (RTP) at 850 °C after standard RCA cleaning. The average oxide thickness was about 1.5 nm, as determined by the ellipsometer. After Al film evaporation, MOS capacitors of $150\text{ }\mu\text{m} \times 150\text{ }\mu\text{m}$ were formed using conventional photolithography. The wafer then was cut along the diameter to get bar-like chips 3 in. in length and about 0.28 in. in width, as shown in Fig. 1(a). Then postmetallization annealing (PMA) was performed in nitrogen at 375 °C for 10 mins in a furnace. The J - V curves of fresh samples were measured in ten MOS devices around the center of chip with HP 4140B. Then external tensile and compressive stresses were applied to bar-like chips, as shown in Fig. 1(b). The positions of chips and the length of sticks were designed

FIG. 1. Schematic diagrams of (a) the bar-like chip and (b) experimental setup for applying the tensile and compressive stresses to chips.

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FIG. 2. Representative J - V curves of reference, tensile stressed, and compressive stressed samples.

to make the tensile and compressive stressed samples have about the same curvature. The stress condition was held for about 1 day. After the release of stress, J - V curves were measured again for the same MOS devices on the stressed samples.

Figures 2(a)–2(c), show the representative J - V curves for reference, tensile stressed, and compressive stressed samples, respectively. In comparison with the J - V curve of reference sample, tensile stress did not have an obvious effect on the J - V curve of the device. By contrast, the leakage current densities in both negative and positive gate biases of the MOS device were significantly increased after it was compressively stressed. The behaviors of J - V curves are explained in more detail in this letter. The changes in gate current densities after stressing with respect to the fresh sample are illustrated in Fig. 3. The current density under -0.8 V gate bias denotes the oxide leakage current under direct tunneling region. The slight increases of leakage current in reference and tensile stressed samples would be caused by the stress-induced-leakage-current (SILC) effect since each device was measured twice. Compressive stress caused a clear increase in direct tunneling current. This increase in current under the direct tunneling region would be most likely due to the increase of interface states after compressive stressing, which could be seen directly from the simulation of interface states effect on the J - V curves.¹⁵ Several other studies also support this inference.^{16,17}

Under 6 V gate bias, the leakage current density of a tensile stressed sample exhibits the same behavior as that of the reference one. The measured value of current under posi-

FIG. 3. Change in percentages of gate current density under 6 and -0.8 V bias for reference, tensile stressed, and compressively stressed samples.

tive bias is very sensitive to room temperature, contact resistance, environmental noise coupling, etc. The actual reason for the slight difference of reference and tensile stressed samples between two measurements, as indicated in Figs. 2(a) and 2(b), is still unknown. However, the compressively stressed sample clearly appeared to have about one order of magnitude increase in the leakage current at 6 V gate bias.

It is known that the leakage current under positive bias involves three main components, i.e., depletion region generation current (J_{dg}), diffusion current (J_{diff}), and generation current of interface states (J_{sg}). They are expressed as:¹⁵

$$J_{dg} = \frac{qn_i w}{\tau_n} [\exp(-\varphi_s/2V_t) - 1], \quad (1)$$

$$J_{diff} \propto \frac{qL_n}{\tau_n} n_{p0} [\exp(-\beta\varphi_s) - 1], \quad (2)$$

and

$$J_{sg} = \frac{qD_{it}\nu_{th}\sigma_n n_i^2}{[p_l + p_s \exp(\beta V_g)]} \frac{\tau_s}{\tau_t + \tau_s} \left([\exp \beta(V_g - \varphi_s) - 1] - \frac{p_s}{n_l} \frac{\sigma_p}{\sigma_n} [1 - \exp(\beta V_g)] \right), \quad (3)$$

where n_i is the intrinsic carrier concentration, w the depletion width, τ_n the electron lifetime, V_t the thermal voltage, φ_s the difference between hole and electron quasi-Fermi levels and almost equal to V_g (gate voltage) for thin gate oxide, L_n electron diffusion length, $n_l(p_l)$ the electron (hole) concentration for the electron (hole) Fermi level at the trap energy level, D_{it} density of interface states, ν_{th} thermal velocity, $\beta = q/kT$, p_s the interface hole concentration, $\sigma_n(\sigma_p)$ the capture cross section for electron (hole), $\tau_t(\tau_s)$ the tunneling time constant to interface states (metal). It should be noticed that both J_{dg} and J_{diff} are related to τ_n , which is dependent on the silicon bulk trap density, while J_{sg} is dominated by D_{it} . Thus in Fig. 2(c), the rapid increase in current density under small positive bias of the compressively stressed sample would be due to the increase in density of interface states.¹⁵ If two devices were different from each other only in D_{it} , but not in τ_n , their leakage current curves under larger positive bias region would be parallel because their J_{dg} and J_{diff} were the same but this is not the case in the observation in Fig. 2(c). There, the current of device after compressive

FIG. 4. Change in percentages of gate current density for reference sample, samples treated by tensile and compressive stress applied in the sequences of CTCT and TCTC, as well as the sample after the release from compressive stress.

stress increased more rapidly than that of the fresh one as the bias was swept. This meant that not only J_{sg} increased, but that J_{dg} and J_{diff} also did. This shows that more silicon bulk traps are created after compressive stress was applied to chips.

It is known that the silicon wafer suffers from inherent tensile stress after oxidation due to volume expansion. After device fabrication, if a proper external tensile stress is applied to a chip, the bonding among atoms seems to be quite elastically recoverable, so little difference in device performance was observed after tensile stress. By contrast, if we bent the chip in a direction opposite to its initial curvature, e.g., a compressive stress was applied, much of the bonding would be broken, and thus more interface states and silicon bulk traps would be generated.

Furthermore, the tensile and compressive stresses were applied alternatively to a chip in different sequences and the $J-V$ curves of device after the release from stressing were measured over a period of time. In this experiment, we denoted T as tensile stress and C as the compressive stress. By comparing the CTCT, TCTC, and reference samples, it can be seen that once the compressive stress was applied to chips, and the change in leakage current would reach about 1000% with respect to that of the fresh sample, in other words, one order of magnitude higher. The data of the CTCT sample indicated that the second applied compressive stress had little effect on the measured leakage current. It was suggested that since the damage was caused after the previously applied compressive stress, the second applied compressive

stress in about the same magnitude would not create more damage. The increase of leakage current of the TCTC sample after the second applied compressive stress would be due to the breakdown of device oxide. From the inset in Fig. 4, it could also be seen that compressive stress would cause the device to be damaged, as mentioned above, and after the stress was released, the damage could not be healed by itself even after several days.

In conclusion, we point out that the MOS structure with an inherently tensile stressed silicon wafer could resist external tensile stress, but under compressive stress it was seriously degraded, by the appearance of increasing surface states and silicon bulk traps although in this letter, the external stress was intentionally applied, however, the mechanical stress could appear anywhere during processing such as wafer handling or the growth of an epilayer with the lattice constant different from that of silicon. This should be a considerable issue in the integration of the ULSI process.

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