Breakdown characteristics of ultrathin gate oxides (<4 nm) in metal–oxide–semiconductor structure subjected to substrate injection

Chia-Hong Huang and Jenn-Gwo Hwu^{a)}

Department of Electrical Engineering/Graduate Institute of Electronics Engineering, National Taiwan University, Room 446, Taipei, Taiwan, Republic of China

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Thin oxide property in a metal–oxide–semiconductor structure subjected to substrate injection from semiconductor into oxide is investigated by means of ramp-up and ramp-down current–voltage (I – V) measurements. Generally, gate injection causes catastrophic dielectric breakdown, and the damaged oxide suffers from permanent destruction which exhibits resistorlike behavior in the I – V curve. For substrate injection, however, there are three distinct modes existing in I – V characteristics. They are resistorlike, hysteresislike, and saturation, i.e., no breakdown. Their occurrence frequencies are dependent on the oxide thickness. For oxides thinner than 2.4 nm, in general, the gate current nearly saturates due to the limitation of minority carriers. For 3.9 nm oxide, the minority carrier generation rate increases due to trap generation near the Si surface. Thus the oxide sustains higher field and larger carrier injection causing destructive damage, i.e., resistorlike mode. For 3 nm oxide, sometimes a hysteresislike mode appears due to light damage in the oxide. The related characteristics of these three modes are studied and exhibit oxide thickness dependence. These phenomena are important to recent studies on devices with ultrathin gate oxides. © 2001 American Vacuum Society. [DOI: 10.1116/1.1403441]

I. INTRODUCTION

Oxide breakdown is still one of the important issues of concern in ultralarge scale integration technology. Especially, for sub-0.15 μm metal–oxide–semiconductor field-effect transistor technology, the gate oxide is required around 3 nm. In such thin oxides, oxide breakdown is significant and complicated. When scaling down silicon dioxide thickness, it is important to understand oxide breakdown properties under both bias polarities. In the existing literatures,^{1–4} oxide breakdown properties of charge-to-breakdown and time-to-breakdown have been investigated under gate and substrate electron injection and exhibit polarity dependence as oxide thickness scales down. Moreover, polarity dependence of the activation energy in charge-to-breakdown and time-to-breakdown has been also presented.⁵ It is reported that post-breakdown resistance of SiO_2 in metal–oxide–semiconductor (MOS) devices is related to polarity dependence and oxide field dependence of charge-to-breakdown.^{6,7}

The mechanism of dielectric breakdown about SiO_2 has been discussed the last few years, however, it is not yet completely understood. In this study it was found that due to the lack of minority carrier supply and high carrier tunneling rate there are three different modes existing in I – V behaviors under substrate injection. They are resistorlike mode, i.e., BD-R, hysteresislike mode, i.e., BD-H, and saturation without breakdown mode, i.e., NBD. Furthermore, the related characteristics of these three modes are as well examined by the dc resistance after breakdown, hysteresis loop voltage, and saturation current density. We also found that the occurrence frequencies of these modes are oxide thickness dependent

and are strongly related to the minority carrier generation rate near the Si surface and also the oxide characteristic. It is useful to understand the actual mechanism of dielectric breakdown under both polarity injections.

II. EXPERIMENT

The devices used in this work are MOS capacitors with an aluminum gate electrode fabricated on (100) oriented p -type substrate. The resistivity of Si substrate is 1–5 Ωcm . The gate oxides were grown at 800 °C in oxygen ambient by rapid thermal oxidation, and then followed by postoxidation annealing (POA) at 960 °C. The oxide thickness ranging from 1.5 to 3.9 nm was determined by ellipsometry. Current–voltage (I – V) measurements with a ramp rate of 0.05 V/s were carried out by using a HP 4140B pA meter/dc voltage source. Before measuring the I – V characteristics the gate was shorted to substrate for a few minutes to avoid transient effects.^{8,9} At least 40 devices were investigated for each sample.

III. RESULTS AND DISCUSSION

Figure 1 shows the typical current–voltage (I – V) characteristics of a MOS capacitor with 2 nm oxide thickness subjected to gate injection before and after breakdown. With a bias increasing a large amount of electrons with high energy supported by an Al gate electrode injects into the oxide, so that as soon as current suddenly increases, the oxide suffers from thermal damage and then reaches catastrophic breakdown with a maximum current density exceeding 10 A/cm^2 . As a result a conductive path exists between Al electrode and Si substrate. In general, this breakdown phenomenon is so-called complete breakdown or hard breakdown. Therefore MOS capacitors subjected to gate injection cannot

^{a)}Corresponding author; electronic mail: hwu@cc.ee.ntu.edu.tw

FIG. 1. Typical current-voltage (I - V) characteristics of a MOS capacitor with 2 nm oxide thickness subjected to gate injection before and after breakdown.

be recovered after breakdown. For substrate injection, however, the electrons in p -type silicon substrate are not so many as those under gate injection, so that the energy delivered to the oxide is not so heavy as above.

Due to the limitation of minority carrier supply, nevertheless, it is observed that there are three different modes in I - V characteristics under substrate injection in this work. Figure 2 shows current-voltage (I - V) characteristics of a MOS capacitor with 3.9 nm oxide thickness subjected to substrate injection before and after breakdown. Even though the applied voltage is gradually increasing after the occurrence of breakdown, the current increases but is obviously limited by carrier thermal generation.¹⁰ It is noted that this current limitation of about 10^{-2} A/cm² in Fig. 2 is not measurement protection limitation. Whether the bias is ramped up or down again after breakdown, I - V characteristics are almost the same and resistorlike. This phenomenon is called resistorlike after breakdown (BD-R) and is similar to Fig. 1. Note that we only consider the first breakdown event in this work.

Additionally, an interesting result is observed. Figure 3 shows four ramp-up and ramp-down I - V characteristics of a MOS capacitor with 3 nm oxide thickness subjected to substrate injection before and after breakdown. It is observed that all ramp-up I - V curves are similar in shape, that is, at a certain bias the gate current suddenly jumps. This observation may be related to the fact that the percolation threshold is not a single value for ultrathin oxides, but rather corre-

FIG. 2. Current-voltage (I - V) characteristics of a MOS capacitor with 3.9 nm oxide thickness subjected to substrate injection before and after breakdown. Resistorlike behavior is shown after oxide breakdown.

FIG. 3. Four ramp-up and ramp-down I - V characteristics of a MOS capacitor with 3 nm oxide thickness subjected to substrate injection before and after breakdown. Hysteresislike behavior is shown after oxide breakdown.

sponds to a distribution of percolation thresholds.¹¹ However, this I - V behavior does not appear in ramp-down I - V curves. Obviously, it is different from Fig. 2. Nevertheless, the difference between ramp-up and ramp-down I - V curves is gradually decreasing as test times after breakdown, and eventually ramp-up and ramp-down I - V curves are merged. In addition, after breakdown ramp-up I - V curves indicate minority carriers cluster trapping and detrapping behavior. Therefore the result in Fig. 3 is due to the light breakdown caused by the limitation of minority carrier supply and many traps generated in the oxide. It is called hysteresislike after breakdown (BD-H). Note that all I - V measurements are in the same capacitor whether for the ramp-up or for the ramp-down measurements.

As the oxide is subject to minority carrier injection, furthermore, oxide breakdown is rarely observed with oxide thickness less than a critical thickness. Figure 4 shows I - V characteristics of MOS capacitors with 1.5, 2, and 2.4 nm oxide thickness in the positive bias regime. It is found that no breakdown occurs and the gate current density is almost constant even if the bias is very large. It is because that the gate current is limited by the generation of minority carriers, and at a certain voltage carrier tunneling rate is larger than minority carrier generation rate. Therefore, the gate current does not rapidly increase with the bias so breakdown does not occur. Moreover, carrier tunneling rate increases with decreasing oxide thickness and increasing a bias. As a result, carrier tunneling rate increases more rapidly in a thinner ox-

FIG. 4. Current-voltage (I - V) characteristics of MOS capacitors with 1.5, 2, and 2.4 nm oxide thickness subjected to substrate injection. No oxide breakdown behavior is observed.

FIG. 5. dc resistance R_{dc} at 2 MV/cm after breakdown versus breakdown field E_{bd} for 3 and 3.9 nm oxide thickness under the BD-R mode.

ide than in a thicker one, so that the gate bias corresponding to the almost saturated current level is less in the thinner oxide than in the thicker one. From Fig. 4, clearly, the generation rate of minority carriers in ultrathin oxide devices is quite smaller than that in thicker oxide ones. This is because of lesser damage to the Si surface during rapid thermal processing in the ultrathin oxide regime. Therefore for thinner oxides the I - V behavior is limited by the minority carrier generation rate. It is called no breakdown (NBD).

On the other hand, in order to deeply understand a breakdown mechanism, we also investigate the related characteristics of three modes. Figure 5 shows the dc resistance R_{dc} at 2 MV/cm after breakdown versus breakdown field E_{bd} for 3 and 3.9 nm oxide thickness under BD-R. The dc resistance R_{dc} is defined by the ratio of the gate voltage to the gate current density at the applied field of 2 MV/cm after breakdown, and breakdown field E_{bd} is defined by the ratio of breakdown voltage to oxide thickness. It is indicated that there are two distinct correlations between the dc resistance and the breakdown field for 3 and 3.9 nm oxides, as shown in Fig. 5. For 3.9 nm oxide, the F-N tunneling component is dominant in conduction, so that thermal destruction caused by higher energy electron injection is serious whether the breakdown field is large or not. Therefore the dc resistances are small and nearly independent of breakdown field. For 3 nm oxide, however, the dc resistance is very sensitive to breakdown field. It is believed that for thinner oxides the direct tunneling component increases. A higher breakdown field corresponds to a larger released energy of the accelerated electrons to the oxide. Consequently, the larger oxide damage causes the decrease in the dc resistance. On the contrary, the lower breakdown field leads to less destruction, so that the dc resistance is higher. Therefore the R_{dc} is dependent on oxide thickness and/or breakdown field, that is, R_{dc} is determined by breakdown occurrence whether the oxide is stressed under F-N tunneling or under direct tunneling.

Figure 6 shows the hysteresis loop voltage ΔV_H versus oxide thickness under the BD-H mode. ΔV_H is defined by the difference between breakdown voltage in the second ramp-up I - V measurement and the gate voltage in the first ramp-down I - V one at the same corresponding gate current. The result indicates that ΔV_H increases with oxide thickness. ΔV_H is related to the number of traps in the oxide which is oxide thickness dependent, breakdown voltage/field, and

FIG. 6. Hysteresis loop voltage ΔV_H versus oxide thickness under the BD-H mode. ΔV_H is defined by the difference between breakdown voltage in the second ramp-up I - V measurement and gate voltage in the first ramp-down I - V measurement at the same corresponding gate current.

breakdown trigger. It needs further investigation.

From the above results, therefore, we propose a breakdown mechanism to explain the BD-H mode. While breakdown occurs and injected carriers are limited by the minority carrier generation, the lateral propagation of thermal damage is suppressed so that a weak or uncomplete conductive path is created between the Si substrate and Al gate electrode under substrate injection. As gate bias is swept down from a positive voltage, a larger amount of minority carriers is crowded in the Si substrate and passes the weak path. When the gate bias is swept up from zero voltage again, minority carriers are increasing with the gate bias but are still insufficient. The current is now larger than that in the fresh one due to the created path, but is smaller than the sweep down one due to the insufficient minority carrier. Eventually, a complete conductive path is reached to cause catastrophic breakdown, thereafter, the ramp-up and the ramp-down I - V curves are merged.

Figure 7 shows the saturation gate current density J_{sat} at $V_G = 5$ V versus oxide thickness for an oxide thinner than 2.4 nm under the NBD mode. In general, the saturation current is influenced by interface trap density and minority carrier lifetime.¹² It is found that the gate current density increases with oxide thickness. It is believed that a thicker oxide introduces larger surface and bulk traps, and therefore more minority carriers via surface and bulk traps are generated so as to lead to a higher saturation current density.¹²

FIG. 7. Gate current density J_{sat} at $V_G = 5$ V versus oxide thickness for oxides thinner than 2.4 nm under NBD mode.

FIG. 8. Occurrence frequencies histogram of NBD, BD-H, and BD-R modes for 3.9, 3, and 2 nm oxides.

Finally, Fig. 8 shows the occurrence frequencies histogram of NBD, BD-H, and BD-R modes for 3.9, 3, and 2 nm oxides. The result indicates that the occurrence frequency of BD-R decreases with decreasing oxide thickness, that the occurrence frequency of BD-H increases initially with decreasing oxide thickness and then decreases, and that the occurrence frequency of NBD increases with decreasing oxide thickness. Note that for 3.9 nm oxide NBD never appears and for 2 nm oxide BD-R does not occur.

From the above observation it is known that the breakdown characteristics of ultrathin oxides under substrate injection are quite different from that under gate injection. The I - V behavior under substrate injection is related to Si surface property as well as the oxide property. While that under gate injection is mainly related to oxide property only. It is of course meaningful to study device under substrate injection.

IV. CONCLUSION

Oxide breakdown properties of MOS capacitors subjected to substrate injection are studied and are found to be different from that subjected to gate injection. It is seen that there are three modes, i.e., BD-R, BD-H, and NBD, in I - V characteristics for oxides less than 4 nm. In general, the BD-R mode occurs in a thicker oxide due to the large supply of minority carriers and high built-up oxide field. The NBD mode is

generally observed in very thin oxide (<3 nm) which accounted for the limited minority carriers and leaky oxide. Besides, between the above two modes, the BD-H mode is observed due to light oxide damage caused by the limitation of minority carrier injection. The related characteristics of these three modes, such as R_{dc} , ΔV_H , and J_{sat} , are investigated and exhibit oxide thickness dependence. We find that there are two distinct relations from R_{dc} versus $\mathcal{E}_{bd}$. In thinner oxides (~ 3 nm), a high breakdown field corresponds to a low R_{dc} . For thicker oxides (~ 4 nm), however, R_{dc} is independent of $\mathcal{E}_{bd}$ and is small. ΔV_H is oxide thickness dependent and it needs further investigation. J_{sat} is larger for thicker oxides than for thinner ones. It is because the generation of minority carriers is different for various oxide properties. We also propose a breakdown mechanism to explain the BD-H mode. Moreover, the occurrence frequencies of three modes depend on oxide thickness and also on the Si surface property. Therefore the Si surface property is important to the above phenomena. These provide experimental foundations for further understanding of breakdown phenomena in ultrathin oxides.

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