Anomalous low-voltage tunneling current characteristics of ultrathin gate oxide (~ 2 nm) after high-field stress

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The effect of oxide barrier shape change caused by stress-induced interface trap charges on the low-voltage tunneling current (LVTC) characteristics of ultrathin gate oxide (~ 2 nm) is studied in this work. It was found that for an ultrathin gate oxide working in the direct tunneling regime, the LVTC behavior is strongly dependent on the barrier shape of the oxide. After high-field stress, anomalous LVTC phenomenon is observed. There is an invariant point existing in current–voltage curves. For a bias smaller than the value of the invariant point, the gate current decreases with stress time. However, for a bias larger than that, the gate current increases with stress time and then saturates. This phenomenon cannot be explained by conventional trap-assisted tunneling conduction, but by the change of tunneling probability due to barrier shape variation. An interface trap charge model is proposed to explain the observed invariant point mentioned above. From this, one can find the voltage corresponding to the midgap bias and, therefore, the initial effective oxide charge number density. © 2001 American Institute of Physics. [DOI: 10.1063/1.1364654]

I. INTRODUCTION

According to the scaling down rule of devices, the gate oxide thickness required for a metal–oxide–semiconductor field-effect transistor with a gate length of 50–70 nm is around 1.5–2 nm. In such an ultrathin gate oxide, direct tunneling (DT) current occurs and is dominant in the current–voltage (I – V) curve when biased typically less than 3 V. This gate leakage current increases power consumption and degrades device performance and circuit stability for ultra-large-scale integration circuits. Nevertheless, it is demanded that the power supply voltage for high-performance microprocessors will be reduced to 1.2 V or less within the next decade. From this point of view, it is required that the leakage current should not be too large. The reduction of leakage current can be resolved by a multiple dielectrics structure with a requirement of an ultrathin buffer interfacial oxide layer to sustain a good interface with the Si substrate.^{1,2} Therefore, it is essential to completely understand the low-voltage tunneling current (LVTC) behavior in the ultrathin gate oxide regime (~ 2 nm). There are many DT current models proposed in the literature.^{3–9} Ghetti *et al.* recently have shown that the low-voltage gate current in ultrathin oxide devices with highly doped substrates can largely exceed the ideal DT component.¹⁰ Additionally, the effects of tunneling probability, the number of tunneling carriers, and the type of tunneling carriers on DT current in gate oxides thinner than 5 nm have been studied.¹¹ On the other hand, the stress-induced leakage current (SILC) generally arises from trap-assisted tunneling via stress-induced traps including interface traps^{12,13} and oxide bulk traps^{14,15} and diminishes as the gate voltage is biased at the Fowler–Nordheim (FN) regime.¹⁶ There are many I – V models for SILC based

on trap-assisted tunneling.^{6,7,17–19} However, the decrease in SILC has been observed as the oxide thickness is less than 5 nm because of the competing effects of the tunneling probability and trap generation rate.^{18,20} Thus, the detailed characteristics of the LVTC are still open to discussion for ultrathin gate oxides (~ 2 nm).

In this work, the effect of oxide barrier change caused by stress-induced interface traps on the low-voltage tunneling current characteristics for ultrathin gate oxides is studied. Anomalous LVTC behavior is observed in the ultrathin gate oxide regime (~ 2 nm). We find that there is an invariant point in the current–voltage curves after high-field stressing. The LVTC corresponding to a bias smaller than the value of the invariant point decreases with stress time. When the bias is larger than that, the LVTC starts to increase with stress time and then saturates. This is unexplainable by the conventional trap-assisted tunneling current effect because it generally increases with oxide trap density.¹⁹ It is believed that the LVTC is strongly dependent on the barrier shape of the oxide, that is, tunneling probability, so that the charges generated in the oxide during the I – V measurement due to interface states being filled or empty should change the barrier shape and, therefore, the LVTC. As there exists the invariant point in the I – V curves, interface trap charge generation instead of trapped charges accounts for the LVTC behavior in this work. The observation occurs only in the oxide with thickness smaller than 3 nm.

II. EXPERIMENT

The devices used in this work are metal–oxide–semiconductor (MOS) capacitors with aluminum gate electrodes fabricated on $\langle 100 \rangle$ -oriented p -type (p -MOS) and n -type (n -MOS) substrates. The resistivities of the Si substrate are 1–5 and 0.55–1.1 Ω cm for p - and n types, respectively. The gate oxides were grown at 800 °C in oxygen am-

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FIG. 1. Experimental current–voltage (J – V) characteristics of MOS capacitors with 1.9–4.8 nm oxide thickness before and after stress.

bient by rapid thermal oxidation, and then followed by postoxidation annealing (POA) at 850, 900, and 960 °C, separately. An oxide thickness ranging from 1.8 to 4.8 nm was determined by ellipsometry. Constant field stress (–13 MV/cm) was applied to the gate oxide with the substrate being grounded. Additionally, negative voltage (–3 V) was applied to the n -MOS capacitors. The stress is interrupted periodically to measure the current–voltage characteristics of the degraded gate oxide with a ramp rate of 0.02 V/s. Before measuring the I – V characteristics, the gate was shorted to the substrate for a few minutes to avoid transient effects.^{14,19} I – V measurements were carried out using a HP 4140B pA meter/dc voltage source. Moreover, the capacitance–voltage (C – V) curve was measured by using a HP 4284 A precision LCR meter before and after stressing.

III. RESULTS AND DISCUSSION

Figure 1 shows the fresh and stressed current–voltage characteristics of the p -MOS capacitors with oxide thickness varying from 1.9 to 4.8 nm. Clearly, there are two distinct I – V characteristics for stressed curves with respect to the fresh one in Fig. 1. Furthermore, it is noted that to avoid the transient effect, the measurements in the same samples have been carried out using different sweeping rates, i.e., 0.1, 0.01, 0.02, and 0.0025 V/s, and no significant difference was observed between them and the result of using a sweeping rate of 0.02 V/s. Therefore, the data shown in the work were taken by using the sweeping rate of 0.02 V/s. For the gate oxide with thickness larger than 3.0 nm, a general stress-induced leakage current due to trap-assisted tunneling is observed. The gate current increases with stress time and diminishes as the gate voltage is biased at the FN regime. This result is similar to those reported in the literature.^{16,19,21} However, for oxides with a thickness less than 3.0 nm, the low-voltage tunneling current is not always monotonously increasing. The difference in the current–voltage curves between them is very obvious. There is an invariant point in the I – V curves with a corresponding voltage of $V_{G(\text{fix})}$ for oxides thickness less than 3 nm. The result is not similar with Ghetti's¹⁰ and Nicollian's.¹³ For bias smaller than $V_{G(\text{fix})}$, the gate current gradually decreases with stress time. But, for bias larger than $V_{G(\text{fix})}$, the gate current increases with stress

FIG. 2. Current density J_G and normalized change of current density $\Delta J/J_{\text{fresh}}$ vs V_G for a p -MOS capacitor after various stresses. The field independence of the crossover point $V_{G(\text{fix})}$ is observed.

time and then saturates. Interestingly, it is observed that the gate current is almost the same at $V_{G(\text{fix})}$ after stressing, so that it cannot be explained by the trap-assisted tunneling conduction mechanism. This phenomenon is reproducibly observed in samples with oxide thickness less than the 3.0 nm studied in this work.

Figure 2 presents the I – V characteristics of the field independence of $V_{G(\text{fix})}$ for the stress field applied continuously from –1 to –15 MV/cm. It is found that even if the stress is continuously varied, the gate current is almost at the same value at –0.78 V. The trend in the I – V characteristics is very similar to the result in Fig. 1 in which the oxide thickness is less than 3.0 nm. The result shows that the conduction mechanism is similar after different field stress. Figure 3 shows the fresh and stressed (–13 MV/cm) low-voltage tunneling current of a p -MOS capacitor with 1.8 nm gate oxide thickness in the negative and positive bias regimes. It is observed that under positive bias the gate current decreases after stressing, and as the bias is larger than 0.75 V, the fresh and stressed curves are merged and are gradually saturated due to the limitation of minority-carrier generation.²²

To understand this phenomenon, we also investigate the I – V characteristics of an n -MOS capacitor with 1.8 nm oxide thickness. Figure 4 shows the fresh and stressed (–3 V)

FIG. 3. Fresh and stressed (–13 MV/cm) low-voltage tunneling current of a p -MOS capacitor with 1.8 nm ultrathin gate oxide in the negative and positive bias regimes.

FIG. 4. Fresh and stressed (-3 V) low-voltage tunneling current of an n -MOS capacitor with 1.8 nm ultrathin gate oxide in the negative and positive bias regimes.

LVTC of an n -MOS capacitor under negative and positive bias conditions. From the left of Fig. 4, it is obviously observed that $V_{G(\text{fix})}$ still exists in the negative bias regime for n -MOS capacitors. For bias less than $V_{G(\text{fix})}$, the gate current decreases with stress time and then saturates. And as the bias is larger than $V_{G(\text{fix})}$, the gate current increases with stress time but does not saturate. It is noted that at negative bias, the semiconductor is in inversion for the n -type Si substrate, and the gate current gradually increases with the gate voltage, but the amount of increased current is small, and then almost saturated because of the limitation of minority-carrier generation.²² At the positive gate voltage, the stressed gate current is smaller than the fresh one, as shown in the right of Fig. 4.

In order to clarify the role of interface traps and oxide traps in I - V curves before and after stressing, capacitance-voltage measurement is carried out before and after stressing for the ultrathin gate oxide (~ 2 nm). Nevertheless, for the ultrathin gate oxide less than 3.0 nm, the interface trap density is not determined from the quasistatic capacitance-voltage measurement because of the large leakage current. Furthermore, the low-frequency C - V curve is similar to the general high-frequency C - V curve as the sample is in dark condition. Consequently, it is difficult to qualitatively analyze the fresh and stressed low-frequency C - V curves measured under the dark condition. So, all samples were illuminated by 0.035 mW/cm² during low-frequency C - V measurement. Figure 5 shows the result of the fresh and stressed C - V characteristics measured at the frequency of 20 Hz under 0.035 mW/cm² illumination. The C - V curves are not smooth because the direct tunneling current is large. With increasing stress time, the minimum of C - V curves moves upward. This is an indication of showing that the interface trap density (D_{it}) indeed increases after stressing.²³ The longer the stress time, the more D_{it} . But, as bias is from -0.6 to -0.2 V, the C - V curves move downward. The capacitance decreases with stress time. This is because in depletion and weak inversion regimes interface traps interact with electrons so that the number of minority carriers decreases. However, as required for charge neutrality, the width of the depletion increases so that the capacitance decreases. Moreover, the capacitance sharply drops because the

FIG. 5. Low-frequency (20 Hz) capacitance-voltage curves measured under 0.035 mW/cm² illumination for fresh and stressed (-13 MV/cm) capacitors.

electrons cannot be instantly generated by thermal generation when the bias is more positive. So, the drop behavior of the C - V curves in weak inversion is also related to the generation of interface traps. Additionally, it is also found that the C - V curves are not shifted. As a consequence, from Fig. 5 it is concluded that the interface trap density increases with stressing but the oxide trap charge changes very little after stressing. Therefore, it is supposed that the anode hole injection (AHI) (Ref. 24) is not serious in ultrathin gate oxides under high-field stress. This is consistent with the existing literature in which the generation rate of the oxide trap is low for ultrathin gate oxides.^{18,20}

In order to explain the above observation from Figs. 1-5, a model of interface trap generation is proposed. Figure 6 shows the schematic energy-band diagrams of a p -MOS capacitor for four distinct bias regimes, $V_{G(\text{mid})} < V_G < 0$, $V_G = V_{G(\text{mid})}$, $V_G < V_{G(\text{mid})} < 0$, and $V_G > 0$, from Figs. 6(a) to 6(d), respectively. It is supposed that $V_{G(\text{mid})}$ is the gate voltage applied to cause the silicon to be intrinsic at the Si/SiO₂ interface. That is to say, the Fermi energy level E_F is pinned at the midgap (E_i) at the Si/SiO₂ interface. Generally, it is

FIG. 6. Schematic energy-band diagrams of a p -MOS capacitor for four distinct voltage regimes: (a) $V_{G(\text{mid})} < V_G < 0$; (b) $V_G = V_{G(\text{mid})}$; (c) $V_G < V_{G(\text{mid})} < 0$; and (d) $V_G > 0$.

FIG. 7. Tunneling probability of a p -MOS capacitor with interface trap densities of $D_{it}=0$, 5×10^{11} , 10^{12} , and $2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ and a sheet of positive oxide trapped charge density of $2.4 \times 10^{-7} \text{ C/cm}^2$ located at a distance of 1 nm from the Si/SiO₂ interface.

believed that the interface traps are donor type below the midgap but acceptor type above the midgap. Since the excess stress-induced interface trap charge ΔQ_{it} is neutral in this situation, the barrier potential is unchanged ($\Delta \phi_B = 0$), and surface band bending is the same. Therefore, the tunneling current is invariant ($\Delta J_G = 0$), as shown in Fig. 6(b). Figure 6(a) shows that for bias $V_{G(\text{mid})} < V_G < 0$, that is, $E_F > E_i$ at the Si/SiO₂ interface, ΔQ_{it} is negative. The barrier potential is higher than normal ($\Delta \phi_B > 0$) and surface band bending decreases, so that the LVTC is reduced ($\Delta J_G < 0$), as shown in Fig. 6(a). However, for bias $V_G < V_{G(\text{mid})} < 0$, that is, $E_F < E_i$ at the Si/SiO₂ interface, ΔQ_{it} is positive. The barrier potential now becomes lower than normal ($\Delta \phi_B < 0$) and surface band bending increases so that the LVTC is increased ($\Delta J_G > 0$), as shown in Fig. 6(c). As the gate voltage is applied under positive bias, the semiconductor is in strong inversion, $E_F \approx E_C$ (conduction-band edge) at the Si/SiO₂ interface, the ΔQ_{it} is negative, as shown in Fig. 6(d). So, the tunneling current is decreased due to negative ΔQ_{it} under positive bias. It is noted that the p -MOS capacitor is proposed under the near-equilibrium condition. For an n -MOS capacitor, the energy-band diagram is similar at the negative and positive bias, as mentioned above for a p -MOS one. The difference between them is only the position of Fermi level E_F .

To demonstrate the observed phenomenon, the effect of the tunneling probability as influenced by the stress-induced interface trap charges on the I - V characteristics, the tunneling probabilities of a p -MOS capacitor with various interface trap densities under various biases are simulated. It is noted that a sheet of positive oxide trap charge density $2.4 \times 10^{-7} \text{ C/cm}^2$ located at a distance of 1 nm from the Si/SiO₂ interface is considered in the simulation. This simulation is based on the Wentzel-Kramers-Brillouin approximation.²⁵ It is noted that the image force effect is neglected and the effective mass is adjusted to yield the better fit in the direct tunneling regime in these simulations.⁸ The simulation results are shown in Fig. 7. It is found that an invariant cross point exists in the tunneling probability versus gate voltage curves. Consequently, the theoretical I - V characteristics of a p -MOS capacitor with various interface trap densities

FIG. 8. Theoretical current-voltage characteristics of a p -MOS capacitor with interface trap densities of $D_{it}=0$, 5×10^{11} , 10^{12} , and $2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$.

without oxide trap charge in the oxide are also simulated. The results are shown in Fig. 8. It is noted that the ideal theoretical value of $V_{G(\text{mid})}$ of the 1.9-nm-thick oxide is about -0.6 V for various interface trap densities, 0 , 5×10^{11} , 10^{12} , and $2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ in Fig. 8. It is observed that LVTC decreases with increasing interface trap density as the gate bias is less than -0.6 V and that LVTC increases with increasing interface trap density as the gate bias is larger than -0.6 V . The LVTC behavior, as shown in Fig. 8, is similar to the tunneling probability, as shown in Fig. 7. The difference between them is that the invariant point is more negative with positive fixed oxide charges than without. That is to say, the invariant point is related to the fixed oxide charge. Whenever the fixed oxide charge is unchanged during stressing, the invariant point will appear. $V_{G(\text{fix})}$ is dependent on the magnitude of the initial fixed oxide charge.

The simulation results are consistent with the experimental observation, as shown from Figs. 1 to 3. It is noted that the distribution of the stress-induced interface traps is assumed to be uniform and symmetric with respect to E_i after stress. Therefore, from Figs. 1 to 4, it is believed that the stress-induced traps are almost not oxide traps but interface traps. The interface trap density increases gradually with stressing time and will saturate. In reality, the stress-induced trap density is not uniform in distribution within the band gap.²⁶

As shown from Figs. 1 to 4, it is found that $V_{G(\text{fix})}$ is more negative than $V_{G(\text{mid})}$. It is reasonable to suppose that the difference between $V_{G(\text{fix})}$ and $V_{G(\text{mid})}$ is caused by the initial effective oxide charge number density N_{eff} . Their relationship can be expressed by

$$V_{G(\text{fix})} = V_{G(\text{mid})} - \frac{qN_{\text{eff}}}{C_{\text{ox}}}. \quad (1)$$

Figure 9 shows the calculated initial effective oxide charge number density extracted from Eq. (1) for the samples after different POA treatments. There are ten MOS capacitors in the measurement for each sample. The insets show the I - V curves of three samples from -0.5 to -1 V . As a result, $V_{G(\text{fix})}$ is obtained by the fresh I - V curve and three stressed I - V curves, as shown in the insets of Fig. 9. It is reasonable to observe that N_{eff} decreases with increasing POA tempera-

FIG. 9. Calculated initial effective oxide charge number density for three POA temperatures of 850, 900, and 960 °C. The insets are the J_G - V_G curves for the three conditions.

ture, as shown in Fig. 9. Table I illustrates the observed $V_{G(\text{fix})}$, the theoretical $V_{G(\text{mid})}$, and the calculated N_{eff} data for various samples. It is also found that N_{eff} is less for the n -MOS capacitor than for p -MOS one. Therefore, it is supposed that it is an alternative approach to find N_{eff} , provided that no oxide trapped charge is induced in LVTC after stress. From the above discussion, the initial N_{eff} can be calculated from the experimental $V_{G(\text{fix})}$ and the theoretical $V_{G(\text{mid})}$.

IV. CONCLUSION

The anomalous low-voltage tunneling current characteristics of ultrathin gate oxides (~ 2 nm) after high electrical stress have been investigated for n - and p -type substrates. LVTC behavior with an invariant point $V_{G(\text{fix})}$ in the I - V curves is observed before and after stress. The decrease in LVTC for $V_{G(\text{fix})} < V_G < 0$ and increase in LVTC for $V_G < V_{G(\text{fix})} < 0$ with stress time are clearly observed for ultrathin gate oxides. The field independence of $V_{G(\text{fix})}$ is found under stress with the field ranging from -1 to -15 MV/cm. These results are not explainable by trap-assisted tunneling conduction only. From the C - V measurements, it is shown that oxide trap charges do not increase with stress time but the interface trap density (D_{it}) does. Thus, stress-induced traps are interface traps for ultrathin gate oxides. Also, the theoretical tunneling probabilities and I - V characteristics are simulated with various D_{it} . There is also an invariant point $V_{G(\text{mid})}$ in the theoretical I - V curves. Therefore, we suggested that the conduction mechanism responsible for the above observation in ultrathin gate oxides is related to the tunneling probability affected by stress-induced interface trap charges. On the other hand, it is also observed that $V_{G(\text{fix})}$ is more negative than $V_{G(\text{mid})}$. It is believed that $V_{G(\text{fix})}$ is related to the fixed oxide charges. From the observed $V_{G(\text{fix})}$ and theoretical $V_{G(\text{mid})}$, one can find the initial effective oxide charge number density N_{eff} . Moreover, it is reasonable to observe that N_{eff} decreases with POA temperature. Therefore, the role of the interface trap is important to the analysis of LVTC behavior for ultrathin gate oxides.

TABLE I. Observed $V_{G(\text{fix})}$, theoretical $V_{G(\text{mid})}$, and calculated N_{eff} from LVTC for samples with various annealing temperatures and substrates.

Substrate type	p -Si		n -Si	
Annealing temperature	850 °C (1.9 nm)	900 °C (1.9 nm)	960 °C (2.0 nm)	960 °C (2.0 nm)
$V_{G(\text{fix})}$ (V) (observed)	-0.863	-0.792	-0.749	-0.69
$V_{G(\text{mid})}$ (V) (theoretical)	~ -0.6		-0.62	
$N_{\text{eff}} (5 \times 10^{12} \text{ cm}^{-2})$ (calculated)	2.99	2.2	1.6	0.79

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