Analysis of STI-induced mechanical stress-related Kink effect of 40 nm PD SOI NMOS devices biased in saturation region

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ABSTRACT

This paper reports the shallow trench isolation (STI)-induced mechanical stress-related Kink effect behaviour of the 40 nm PD SOI NMOS device. As verified by the experimentally measured data and the 2D simulation results, the Kink effect behaviour in the saturation region occurs at a higher V_D for the 40 nm PD device with a smaller S/D length (SA) of 0.17 μm as compared to the one with the SA of 1.7 μm due to the higher body-source bandgap narrowing (BGN) effect on the parasitic bipolar device (BJT) from the higher STI-induced mechanical stress, offset by the impact ionization (II) enhanced by the BGN in the high electric field region near the drain.

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1. Introduction

Mechanical stress induced by STI may affect the performance of CMOS devices [1,2]. Mechanical stress may affect work function, effective mass, carrier mobility, and junction leakage, etc. [3]. SOI is becoming another mainstream technology for CMOS VLSI in the nanometer regime [4]. For nanometer PD SOI CMOS devices, the source/drain region could be very small, hence the STI-induced mechanical stress cannot be overlooked. In the past, the effects of mechanical stress on the performance of SOI MOS devices with STI have been studied [1]. PD SOI NMOS devices have been reported for the notorious Kink effect behaviour [5]. Recently, the STI-induced mechanical stress effects on the Kink effect of the PD SOI CMOS devices have been reported [6–8]. In this paper, a detailed analysis of the STI-induced mechanical stress effects on the Kink effect behaviour of 40 nm PD SOI NMOS devices is presented. It will be shown that the bandgap narrowing (BGN) due to the STI-induced mechanical stress effects has a profound impact on the parasitic bipolar device (BJT) and the impact ionization (II), which influence the saturation region Kink effect behaviour of the PD SOI NMOS devices substantially. In the following sections, the device structure of the 40 nm PD SOI NMOS devices and the mechanical stress with the bandgap narrowing

are described first, followed by the Kink effect behaviour and discussion.

2. 40 nm PD SOI NMOS device

The cross sections of the 40 nm PD SOI NMOS test device fabricated in the industry are shown in Fig. 1. It has a 70 nm thin film doped with an acceptor impurity density of $3 \times 10^{18} \text{ cm}^{-3}$ above a buried oxide of 145 nm, under a gate oxide of 1.8 nm. A 65 nm lightly doped drain (LDD) region doped with an n-type density of 10^{19} cm^{-3} under a sidewall spacer has been used. A nickel polycide is formed on the top of the gate and a SiN capping layer is deposited over the device. Two cases of the test devices with the S/D length (SA) of 1.7 μm and 0.17 μm have been designed for the study. The width of the devices is 1 μm . The test devices have been designed in a way such that the structures are similar to each other. Experimental measurement of the test device and 2D device simulation considering mechanical stress effects have been used to carry out the study.

During the thermal anneal cycle of the manufacturing process for forming the STI structure, a mechanical stress occurs in the PD SOI NMOS device [1]. Based on the result from a process simulator [9] considering the hydrostatic pressure with the 2D device simulator [10], Fig. 2 shows the hydrostatic pressure and the associated BGN distribution at 3 nm below the gate oxide interface in the lateral direction of the 40 nm PD SOI NMOS device with the SA of 0.17 μm and 1.7 μm . As induced by STI, the mechanical stress in

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Fig. 1. Cross sections of the 40 nm PD SOI NMOS device under study.

Fig. 2. Mechanical stress and the corresponding bandgap narrowing (BGN) distribution at 3 nm below the gate oxide interface in the lateral direction of the 40 nm PD SOI NMOS device with the S/D length (SA) of 0.17 μm and 1.7 μm based on the 2D simulation.

terms of hydrostatic pressure is large in the SA near STI and decreases away from it. The corresponding BGN, which is correlated to the mechanical stress, has a dramatic impact on the saturation region Kink effect behaviour of the 40 nm PD NMOS device.

3. Saturation region Kink effect behaviour

Fig. 3 shows I_D versus V_D of the 40 nm PD NMOS device with SA of 1.7 μm and 0.17 μm , biased with its body floating, based on the

Fig. 3. Drain current versus drain voltage of the 40 nm PD SOI NMOS device with the SA of 1.7 μm and 0.17 μm , based on the experimentally measured data and 2D device simulation results using the mechanical stress and the corresponding BGN model with and without considering the BGN in the impact ionization (II) model.

experimentally measured data and 2D device simulation results using the mechanical stress model and the corresponding BGN model. In order to discriminate the BGN effect in the BJT from that in the II region, 2D device simulation results based on the II model considering BGN and without have been done. As shown in the figure, with a smaller SA of 0.17 μm , the Kink effect behaviour occurs at a larger V_D as compared to the case with the SA of 1.7 μm . Considering BGN in the II model, the Kink effect behaviour occurs at a smaller V_D . Without considering BGN in the II model while doing the 2D device simulation, the curves shift to the right. Please note that 2D simulation with and without considering the tunnelling leakage current has been done. Although the tunnelling leakage current has a substantial effect on the gate current, the drain current characteristics in the saturation region remain the same with and without considering the tunnelling leakage current. The difference between the simulation results and the experimental data is mainly due to the limitation of the mobility model used.

Fig. 4 shows the related output conductance versus V_D characteristics of the PD device with the SA of 0.17 μm and 1.7 μm , based on the experimentally measured data and the 2D simulation results using the mechanical stress model and the corresponding

Fig. 4. Output conductance versus drain voltage of the 40 nm PD SOI NMOS device biased at $V_G = 0.8 \text{ V}$, based on the experimentally measured data and 2D device simulation results using the mechanical stress and the corresponding BGN model, with and without considering the BGN in the II model.

BGN model with and without considering the BGN in the II model, biased at $V_G = 0.8$ V. With the smaller SA of $0.17 \mu\text{m}$, the Kink effect behaviour indeed occurs at a larger V_D due to the higher BGN effect from the larger mechanical stress. Without considering BGN in the II model, the curves shift to the right. Please note that the smaller output conductance for the case with the SA of $0.17 \mu\text{m}$ is due to the increased source/drain resistance.

4. Discussion

The Kink effect behaviour of the PD SOI NMOS device could be understood by considering the plots of the 2D hole and electron quasi-Fermi potential (Φ_p/Φ_n) contours in the PD SOI NMOS device with the SA of $0.17 \mu\text{m}$, biased at $V_G = 0.4$ V and $V_D = 0.8$ V, based on the 2D device simulation results using the mechanical stress and the corresponding BGN model as shown in Fig. 5. Also shown in the figures are the 2D hole and electron current vector distributions. From Fig. 5, the electron current is flowing mostly in the surface channel under the gate oxide while the hole current is originated from the high electric field region in the post-pinchoff region, where II occurs. The hole current flows to the region below the surface channel in the thin film, which accommodates the BJT.

Fig. 6 shows the current conduction mechanism of the PD SOI NMOS device under study, biased in the saturation region and including the Kink effect [11]. At the gate oxide/thin film interface, there is a channel current (I_{ch}) due to electron drift. In the high

electric field region near the drain, II takes place, resulting in electron and hole pair formation. The generated electrons and holes move in the opposite directions as a result of the electric field—the generated electrons move toward the drain contact and the generated holes move in the source direction. This results in the generated electron and hole currents (I_h) that are equal in magnitude (the II current). A portion of the II current (kI_h) is directed vertically toward the buried oxide owing to the vertical field. As a result, in the area above the buried oxide in the thin film, there is a hole (base current) which leads to activation of the parasitic BJT above the buried oxide. As the BJT is activated, these holes recombine with electrons in the base region. In the parasitic BJT region, a portion of the collector current ($k'I_c$), which is mainly composed of electrons, is toward the high electric field as a result of the vertical electric field. These electrons also give rise to II and consequently also generate electron and hole pairs as for the channel current described above. Considering the effects of the II and the parasitic BJT, the drain current is composed of the channel current (I_{ch}), the II current (I_h), and the collector current (I_c) of the parasitic BJT:

$$I_D = I_{ch} + I_h + I_c. \quad (1)$$

The source current of the device can be expressed as the sum of the channel current (I_{ch}), a portion of the II current $[(1-k)I_h]$, and the emitter current (I_e) of the BJT:

$$I_s = I_{ch} + (1-k)I_h + I_e. \quad (2)$$

The II current is a function of the current components, which include the channel current (I_{ch}) and a portion of the collector current ($k'I_c$) following through the high electric field region:

$$I_h = (M-1)(I_{ch} + k'I_c), \quad (3)$$

where M is the multiplication factor, which is a function of the BGN ionization coefficient in the nonlocal II model [10]. From Eqs. (1)–(3), the drain current of the PD SOI NMOS device biased in the saturation region with the Kink effect behaviour is closely related to the parasitic BJT and the II in the post-pinchoff region, which are dependent on the BGN.

Fig. 7 shows the body-source voltage— the V_{BE} of the BJT in the thin film, versus the drain voltage of the 40 nm PD SOI NMOS device, biased at $V_G = 0.8$ V and 0.4 V, based on 2D device simulation results using the mechanical stress and the corresponding BGN model with and without considering the BGN in the II model. Note that the V_{BE} of the BJT is extracted from the hole quasi-Fermi potential (Φ_p) at the centre of the lateral channel in the device from the simulation results. As shown in the figure, with a smaller SA of $0.17 \mu\text{m}$, the body-source voltage rises at a larger V_D , which indicates the later turn on the BJT device, which could be reasoned as follows. The current gain of the BJT is a function of the difference in the BGN between the base and the emitter [12]:

$$\beta \propto \exp(\Delta E_{gb} - \Delta E_{ge}/kT), \quad (4)$$

where ΔE_{gb} and ΔE_{ge} are the BGN in the base and emitter regions, respectively. K is Boltzmann constant. T is the temperature in Kelvin. Due to the higher mechanical stress from STI, the BGN in the emitter/source ΔE_{ge} is larger than that in the base/channel region ΔE_{gb} for the $0.17 \mu\text{m}$ case as shown in Table 1. Please note that $\Delta E_{gb} - \Delta E_{ge}$ is negative. Since $\Delta E_{gb} - \Delta E_{ge}$ (-15.3 meV) is more negative for the $0.17 \mu\text{m}$ case as compared to the $1.7 \mu\text{m}$ one (-10 meV), the parasitic BJT turns on later for the $0.17 \mu\text{m}$ case, which is reflected as a weaker BJT function at $V_D = 0.8$ V as shown in Fig. 7 and Table 2.

Please note that in Table 2, ΔV_{be} is defined as the difference in the base-emitter voltage between the 40 nm PD SOI NMOS devices with the SA of $0.17 \mu\text{m}$ and $1.7 \mu\text{m}$, which is extracted from the simulation results. At $V_D = 0.8$ V, without considering BGN in the

Fig. 5. Plots of the 2D hole and electron quasi-Fermi potential (Φ_p/Φ_n) contours in the PD SOI NMOS device with the SA of $0.17 \mu\text{m}$, biased at $V_G = 0.4$ V and $V_D = 0.8$ V, based on 2D device simulation results using the mechanical stress and the corresponding BGN model. Also shown in the figures are the 2D hole and electron current vector distributions.

Fig. 6. Current conduction mechanism of the PD SOI NMOS device under study, biased in the saturation region with the Kink effect behaviour.

Fig. 7. Base-emitter voltage versus drain voltage of the 40 nm PD SOI NMOS device biased at $V_G = 0.8$ V and 0.4 V, based on 2D device simulation results using the mechanical stress and the corresponding BGN model with and without considering the BGN in the II model.

Table 1

Effective bandgap narrowing (BGN) in the base and the emitter of the parasitic BJT in the 40 nm PD SOI NMOS device with the S/D length (SA) of 0.17 μ m and 1.7 μ m based on the 2D device simulation results using the mechanical stress and the corresponding BGN model

S/DL ΔE_g	ΔE_{gb}	ΔE_{ge}
0.17 μ m	34.7 meV	50 meV
1.7 μ m	4.5 meV	14.5 meV

Table 2

The difference in base-emitter voltage (ΔV_{be}) between the 40 nm PD SOI NMOS device with the SA of 0.17 μ m and 1.7 μ m, biased at $V_D = 0.8$ V and V_G of 0.8 V and 0.4 V, based on the 2D device simulation results using the mechanical stress and the corresponding BGN model, with and without considering the bandgap narrowing in the impact ionization (II) model

II Model V_G	With BGN	w/o BGN
0.8 V	57.8 mV	107.5 mV
0.4 V	1.4 mV	40.3 mV

II model, the difference in base-emitter voltage (ΔV_{be}) between the cases for the 40 nm PD SOI NMOS devices with the SA of 0.17 μ m and 1.7 μ m is 107 mV at $V_G = 0.8$ V and 40 mV at $V_G = 0.4$ V. The parasitic BJT is more difficult to turn on for the case with the SA of 0.17 μ m as compared to the case with the SA of 1.7 μ m due to the more negative value of $\Delta E_{gb} - \Delta E_{ge}$. Therefore, the function of the parasitic BJT in the thin film of the device with the shorter SA of 0.17 μ m becomes weaker due to the BGN effect.

In addition to the BJT effect, the Kink effect behaviour is also affected by the II in the high electric field region near the drain. BGN in the high electric field region may help the II [10]. As shown in Fig. 7 and Table 2, considering BGN in the II model, the difference in V_{BE} (ΔV_{be}) between the cases for the 40 nm PD SOI NMOS device with the SA of 0.17 μ m and the 1.7 μ m becomes smaller. At $V_D = 0.8$ V, ΔV_{be} shrinks from 107 mV to 57 mV at $V_G = 0.8$ V and from 43 mV to 1.4 mV at $V_G = 0.4$ V. Therefore, the Kink effect behaviour in the saturation region occurs at a higher V_D for the 40 nm PD device with a smaller SA of 0.17 μ m due to the higher body-source BGN effect on the parasitic BJT from the higher STI-induced mechanical stress, offset by the II enhanced by the BGN in the high electric field region near the drain.

5. Conclusion

In this paper, the STI-induced mechanical stress-related Kink effect behaviour of the 40 nm PD SOI NMOS device has been reported. As verified by the experimentally measured data and the 2D simulation results, the Kink effect behaviour in the saturation region occurs at a higher V_D for the 40 nm PD device with a smaller SA of 0.17 μ m as compared to the one with the SA of 1.7 μ m due to the higher body-source BGN effect on the BJT from the higher STI-induced mechanical stress, offset by the II enhanced by the BGN in the high electric field region near the drain.

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