Briefs

Modeling the Fringing Electric Field Effect on the Threshold Voltage of FD SOI nMOS Devices With the LDD/Sidewall Oxide Spacer Structure

S. C. Lin and J. B. Kuo

Abstract—This paper presents analysis of the fringing electric field effect on the threshold voltage of fully depleted (FD) silicon-on-insulator nMOS devices with the lightly doped drain (LDD)/sidewall oxide spacer structure based on a closed-form analytical model derived from the two-dimensional (2-D) Poisson's equation and using the conformal mapping technique. Based on the analytical model, as verified by the experimental data and the 2-D simulation results, with a lower n-LDD doping density, the fringing electric field effect in the sidewall oxide spacer lowers the short-channel effect.

Index Terms—Device model, fringing electric field, fully depleted, silicon-on-insulator (SOI), nMOS.

I. INTRODUCTION

Fully depleted (FD) silicon-on-insulator (SOI) CMOS devices provide advantages in reduced short-channel effects and smaller floating body effects [1], [2]. As for bulk counterparts, the LDD/sidewall oxide spacer structure has also been used in a short-channel FD SOI CMOS devices to reduce high electric field effects [3] [4]. Short-channel effects of the FD SOI CMOS devices have been reported [5], [6]. In fact, the fringing electric field in the sidewall oxide spacer is important since it may affect the performance of the FD SOI CMOS devices with the LDD/sidewall oxide spacer structure. Recently, fringing induced barrier lowering (FIBL) in a sub-100-nm nMOS device in terms of the gate dielectric constant has been reported [7]. In fact, the fringing electric field in the sidewall oxide spacer region may have a strong impact on the device performance. Due to the complexity from the LDD/sidewall oxide spacer structure, until now no analytical model for the fringing electric field related threshold voltage is available. In this paper, the analysis of the fringing electric field effect of FD SOI nMOS devices with the LDD/sidewall oxide spacer structure based on a closed-form analytical model derived from the two-dimensional (2-D) Poisson’s equation and using the conformal mapping technique is described. It will be shown that based on the analytical model, as verified by the experimental data and the 2-D simulation results, with a lower n-LDD doping density, the fringing electric field effect in the sidewall oxide spacer lowers the short-channel effect.

II. MODEL DERIVATION

In order to concentrate on the fringing electric field effect and to simplify the analysis, an FD SOI nMOS device with an LDD/sidewall oxide spacer structure has been studied [3]. Fig. 1 shows the 2-D electric field contours in a 0.25-μm FD SOI nMOS device with a 0.1-μm lightly doped drain (LDD)/sidewall oxide spacer structure and an n⁺ polysilicon gate of 2000 Å, biased at V_D = 0.1 V and the threshold voltage—V_GS = 0.193 V.

Fig. 1. Two-dimensional electric field contours in a 0.25-μm FD SOI nMOS device with a 0.1-μm lightly doped drain (LDD)/sidewall oxide spacer structure, having an n⁺ polysilicon gate of 2000 Å, a front gate oxide of 70 Å, a thin-film of 500 Å doped with a p-type doping density of 2 × 10¹⁷ cm⁻³, and a buried oxide of 4000 Å, biased at V_D = 0.1 V and the threshold voltage—V_GS = 0.193 V.

The fringing electric field in the sidewall oxide spacer region may have a strong impact on the device performance. Due to the complexity from the LDD/sidewall oxide spacer structure, until now no analytical model for the fringing electric field related threshold voltage is available. In this paper, the analysis of the fringing electric field effect of FD SOI nMOS devices with the LDD/sidewall oxide spacer structure based on a closed-form analytical model derived from the two-dimensional (2-D) Poisson’s equation and using the conformal mapping technique is described. It will be shown that based on the analytical model, as verified by the experimental data and the 2-D simulation results, with a lower n-LDD doping density, the fringing electric field effect in the sidewall oxide spacer lowers the short-channel effect.

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For the FD SOI nMOS device under study [Fig. 2(a)], the origin is at the source end of the channel under the front gate oxide. The x axis is in the substrate direction and the y axis is in the lateral channel direction toward the drain. A quasi-2-D approach as used in modeling the partially depleted SOI devices [10] has been adopted to solve the 2-D Poisson’s equation. In order to facilitate model derivation, the depletion region in the thin-film of the device is divided into three portions:

1) the n-LDD depletion region near the source (I);
2) the n-LDD depletion region near the drain (II);
3) the p-channel region under the gate (III).

In region (I), the n-LDD depletion region near the source, its width is determined by the doping density of the p-type channel region (N_A) and the n-LDD region (N_D) as

\[ L_s = \frac{2e_A}{q} \frac{N_A}{(N_A + N_D)} \frac{V_{bi}}{N_D} \]

where \( V_{bi} \) is the built-in voltage:

\[ V_{bi} = \frac{kT}{q} \ln \left( \frac{N_D N_A}{n_i^2} \right) \]

\( n_i \) is the intrinsic concentration, \( \varepsilon_A \) is silicon permittivity, and \( q \) is the electron charge. In region (II), the n-LDD depletion region near the drain, its width is decided by the drain voltage as

\[ L_d = \frac{2e_A}{q} \frac{N_A}{(N_A + N_D)} \left( \frac{V_{bi} + V_D}{N_D} \right) \]

Note that in \( L_s \) and \( L_d \), the 2-D effect has been neglected.

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In these three depleted regions in the thin-film, the electrostatic potential can be approximated using the polynomial as shown below [8]

$$\Psi_i(x, y) = a_{0i}(y) + a_{1i}(y)x + a_{2i}(y)x^2$$  \hspace{1cm} (1)

where $i$ is (1), (2), or (3), representing the three depleted regions, respectively. Equation (1) should satisfy the 2-D Poisson’s equation

$$\frac{\partial^2 \Psi_i(x, y)}{\partial x^2} + \frac{\partial^2 \Psi_i(x, y)}{\partial y^2} = -\frac{qN}{\epsilon_{ox}}$$  \hspace{1cm} (2)

where $N$ is equal to $N_D$ in the n-LDD region and $-N_A$ in the p-type channel region. The four boundary conditions for the 2-D Poisson’s equation are described as follows: 1) at the front gate oxide/thin-film interface ($x = 0$), the electrostatic potential is $\Psi_i(0, y) = \Psi_{atl}(y)$, where $\Psi_{atl}(y)$ is the surface electrostatic potential of the thin-film at location $y$. 2) At the buried oxide/thin-film interface ($x = t_{ox}$), where $t_{ox}$ is the thin-film thickness, the electrostatic potential is $\Psi_i(t_{ox}, y) = \Psi_{absl}(y)$, where $\Psi_{absl}(y)$ is the electrostatic potential on the top of the buried oxide. 3) At the front gate oxide/thin-film interface ($x = 0$), from Gauss Law, the displacement is continuous. Thus, one obtains

$$\left. \frac{\partial \Psi_i(x, y)}{\partial x} \right|_{x=0} = -\frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\Psi_{cit} - \Psi_{atl}(y)}{l(y)}$$

where $\epsilon_{ox}$ is oxide permittivity, $\Psi_{cit}$ is the electrostatic potential of the polysilicon gate $\Psi_{cit} = V_{Ga} - \phi_f + \phi_g = (kT/q)\ln(N_D/n_i)$ is the fermi potential of the n-type polysilicon gate, and $l(y)$ is the distance between the gate electrode and the thin-film/buried oxide interface. 4) Similarly, at the buried oxide/thin-film interface, from Gauss Law, one obtains

$$\left. \frac{\partial \Psi_i(x, y)}{\partial x} \right|_{x=t_{box}} = -\frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\Psi_{absl}(y) - \Psi_{cit}}{t_{box}}$$

where $t_{box}$ is the thickness of the buried oxide and $\Psi_{cit}$ is the electrostatic potential of the back gate ($\Psi_{cit} = V_{back} - \phi_{fbox}$), $V_{back}$ is the back gate bias, and $\phi_{fbox} = (kT/q)\ln(n_i/N_{mub})$ is the fermi potential of the p-type substrate.

A. Region (I)

In region (I)—in the n-LDD depletion region under the sidewall oxide spacer near the source, it is affected by the fringe electric field in the sidewall oxide spacer. A conformal mapping technique [8], [11] has been applied to simplify the analysis. In region (I), from (1) and the boundary conditions, the electrostatic potential at the thin-film/buried oxide interface and the coefficients in the electrostatic potential $\Psi_I(x, y)$ are

$$\Psi_{absl}(y) = \frac{\epsilon_{ox}}{2C_x + C_{box}} \left\{ -\frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\Psi_{cit} - \Psi_{atl}(y)}{l(y)} + \frac{2}{t_{si}} \Psi_{atl}(y) + \frac{C_{box}}{\epsilon_{ox}} \Psi_{cit} \right\}$$  \hspace{1cm} (3)

where

$$a_{01}(y) = \Psi_{atl}(y), \hspace{0.5cm} a_{11}(y) = -\frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\Psi_{cit} - \Psi_{atl}(y)}{l(y)}$$

$$a_{21}(y) = \frac{1}{t_{si}} \left\{ \Psi_{absl}(y) - \left[ 1 + \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{t_{si}}{l(y)} \right] \Psi_{atl}(y) \right\}$$

In order to simplify the effect of the nonfixed value of the distance $(l(y))$ between the gate electrode and the thin-film/buried oxide interface on the term $\Psi_{cit} - \Psi_{atl}(y)/l(y)$ in $a_{11}(y)$, in the n-LDD region under the sidewall oxide spacer, conformal mapping transformation technique [8], [11] has been used to transform the original $x X + y Y$ space in terms of the $X$ and $Y$ axes as shown in Fig. 3(b) into the $u U + v V$ space in terms of $U$ and $V$ axes based on the following transfer function: $y Y' = n x X' = K \sinh(u U + v V)$, where

$$n = \frac{L_{sid}}{t_{si} \sinh \left[ \frac{\cosh^{-1} \left( \frac{L_{sid} t_{si}}{t_{ox}} \right)}{t_{ox}} \right]}$$

$$K = \frac{-L_{sid}}{\sinh \left[ \frac{\cosh^{-1} \left( \frac{L_{sid} t_{si}}{t_{ox}} \right)}{t_{ox}} \right]}$$

and $L_{sid}$ is the width of the n-LDD region. Based on the above formula, ABCD in the $x X + y Y$ coordinates is transformed into $A'B'C'D'$ in the $u U + v V$ coordinates. Under this condition, the arc-shaped electric field contour in the sidewall oxide spacer in the $x X + y Y$ coordinates becomes straight-line-shaped in the $u U + v V$ coordinates. Based on this transformation, the distance between the gate electrode and the n-LDD/sidewall oxide spacer interface $(l(y))$, which is not a fixed value, has been transformed into $m \pi/2$, which is the distance between points $A'$ and $C'$ in the new coordinates, with the condition that $m$ must satisfy $\sin(m \pi/2) = 1$. Based on the conformal mapping formula, the term $-\Psi_{cit} - \Psi_{atl}(y)/l(y)$ has been simplified to $(\Psi_{cit} - \Psi_{v}(v))/m \pi/2$ in the new coordinates. Therefore, one also obtains: $y = K \sinh V$ at the thin-film/front gate oxide interface $(x = 0)$. With the transformation, one obtains

$$a_{01}(v) = \Psi_{v}(v)$$

$$a_{11}(v) = -\frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\Psi_{cit} - \Psi_{v}(v)}{m \pi/2}$$

$$a_{21}(v) = -\alpha \Psi_{v}(v) + \beta_0$$  \hspace{1cm} (4)

where

$$\alpha_0 = \frac{1}{t_{si}} \left\{ -\frac{C_s + C_{box}}{(2C_x + C_{box})C_s} \right\}$$

and

$$\beta_0 = \frac{1}{t_{si}} \left\{ \frac{C_s + C_{box}}{(2C_x + C_{box})C_s} \right\}$$

The 2-D Poisson’s equation of (2) can be further simplified using the following approach [12]—at any depth $(x)$ in the thin-film, the deriva-
tive of the electric field in the lateral channel direction is related to the derivative of the surface electric field as follows:

$$\frac{\partial^2 \Psi_s(x, y)}{\partial y^2} = \frac{1}{k_s} \frac{d^2 \Psi_s(x, y)}{dy^2}$$

(5)

where $k_s$ is a parameter less than 1 ($k_s < 1$). In region (I), from (5) with the conforming mapping technique, one obtains

$$\frac{\partial^2 \Psi_1(x, y)}{\partial y^2} = \frac{1}{k_s} \left[ \frac{d^2 \Psi_1(v)}{dv^2} - \frac{1}{K^2 \cosh^2 v} \left( \frac{d \Psi_1(v)}{dv} \right)^2 \right]$$

(6)

in the new coordinates. Therefore, a second-order differential equation in terms of the surface electrostatic potential in the new coordinates has been obtained

$$\frac{d^2 \Psi_1(v)}{dv^2} - \left( \frac{d \Psi_1(v)}{dv} \right)^2 + \left( \frac{B_0 \cosh^2 v}{K} \right) \Psi_1(v) = B_1 \cosh^2 v$$

$$B_0 = \frac{q N_D}{\epsilon_a} K^2$$

$$B_1 = - \left( \frac{q N_D}{\epsilon_a} + \beta_0 \right) k_s K^2.$$  

(7)

Solving (7), the surface electrostatic potential in the new coordinates is

$$\Psi_1(v) = g_1 e^{r \sinh v} + g_2 e^{-r \sinh v} + \frac{B_1}{B_0}$$

$$r = \sqrt{-B_0}.$$  

(8)

Using the conforming mapping transformation ($y = K \sinh v$), (8) becomes

$$\Psi_{a1}(y) = g_1 e^{r \sinh y} + g_2 e^{-r \sinh y} + \frac{B_1}{B_0}$$

(9)

in the original coordinates. Considering the boundary conditions: 1) at the left end of the n-LDD depletion region, the surface electrostatic potential is equal to $\Psi_{a1}(L) = \psi_{in}$, where $\psi_{in} = (kT/q) \ln(N_D/n_i)$ and $N_D$ is the doping density of the n-LDD region; 2) at the right end, the surface electrostatic potential is equal to $\Psi_{a1}(0) = \Psi_1$, then the surface electrostatic potential in region (I) becomes

$$\Psi_{a1}(y) = g_1 e^{r \sinh y} + g_2 e^{-r \sinh y} + \frac{B_1}{B_0}$$

(10)

where

$$g_1 = \frac{1}{2 \sinh \left( \frac{r L}{K} \right)} \left\{ \left( \frac{\psi_{in} - B_1}{B_0} \right) e^{r \sinh L} \right\}$$

and

$$g_2 = \frac{1}{2 \sinh \left( \frac{r L}{K} \right)} \left\{ \left( \frac{\psi_{in} - B_1}{B_0} \right) e^{-r \sinh L} \right\}.$$  

B. Region (II)

In region (II), its structure is identical to that in region (I). Therefore, the approach in obtaining the electrostatic potential ($\Psi_2(x, y)$) and the surface electrostatic potential ($\Psi_{a2}(y)$) is similar as for region (I) except the boundary conditions: 1) at the left end of the depleted n-LDD region, its surface electrostatic potential is $\Psi_{a2}(L) = \Psi_2$ and 2) at the right end, it is $\Psi_{a2}((L + L_d) = V_{DS} + \phi_{in}$. Consequently, the surface electrostatic potential in region (II) is

$$\Psi_{a2}(y) = g_3 e^{r \sinh y} + g_4 e^{-r \sinh y} + \frac{B_1}{B_0}$$

(11)

where

$$g_3 = \frac{1}{2 \sinh \left( \frac{r L_d}{K} \right)} \left\{ \left( \frac{V_{DS} + \phi_{in} - B_1}{B_0} \right) e^{r \sinh L_d} \right\}$$

and

$$g_4 = \frac{1}{2 \sinh \left( \frac{r L_d}{K} \right)} \left\{ \left( \frac{V_{DS} + \phi_{in} - B_1}{B_0} \right) e^{-r \sinh L_d} \right\}.$$  

C. Region (III)

In region (III), for the p-channel depletion region under the front gate oxide, the equations derived before are still applicable except that $t(y)$ should be replaced by the front gate oxide thickness $t_{ox}. From (1), the relationship between the front surface electrostatic potential $\Psi_{st}(y)$ and the back surface electrostatic potential $\Psi_{at}(y)$, and the coefficients $a_{03}(y), a_{13}(y)$, and $a_{23}(y)$ have been obtained:

$$\Psi_{st}(y) = \frac{2C_x + C_{ox}}{2C_x + C_{box}} \Psi_{at}(y) - \frac{C_{ox}}{2C_x + C_{box}} \Psi_{Gib} - \frac{C_{box}}{2C_x + C_{box}} \Psi_{Gib}$$

(12)

where

$$a_{03}(y) = \Psi_{at}(y)$$

$$a_{13}(y) = \frac{C_{ox}}{C_{box} + C_{ox}} \Psi_{at}(y) - \frac{C_{box}}{C_{box} + C_{ox}} \Psi_{Gib}$$

and

$$a_{23}(y) = \frac{1}{r^2} \left\{ \left( \frac{C_{box} + C_{ox}}{2C_x + C_{box} + C_{ox}} \right) \Psi_{at}(y) - \frac{C_{box}}{2C_x + C_{box}} \Psi_{Gib} \right\}.$$  

From (12), one obtains a second-order differential equation in terms of the surface electrostatic potential

$$\frac{d^2 \Psi_{at}(y)}{dy^2} = \frac{1}{r^2} \Psi_{at}(y) = G_1$$

(13)

where

$$G_1 = \frac{g N_D k_s}{\epsilon_a} - \frac{2k_2 C_{ox} C_x + C_{box} C_x}{r^2} \Psi_{at}$$

$$+ \frac{2k_2 C_{box} C_x}{r^2} \Psi_{Gib}$$

and

$$r = \frac{1}{2k_2} \left( \frac{C_{box} + C_{ox}}{2C_x + C_{box} + C_{ox}} \right) \Psi_{Gib} + G_{00} + G_{02} \Psi_{Gib} + G_{03} \Psi_{Gib}.$$  

The boundary conditions for the above equation are 1) at the left end, its surface electrostatic potential is $\Psi_{at}(0) = \Psi_1$, and 2) at the right end, it is $\Psi_{at}(L) = \Psi_2$. Solving the differential equation [(13)] with the boundary conditions, one obtains

$$\Psi_{at}(y) = g_5 e^{r \sinh y} + g_6 e^{-r \sinh y} - \frac{G_1}{r^2}$$

(14)

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where

\[ g_5 = \frac{1}{2 \sinh(r_1 L)} \left[ -\Psi_1 e^{-r_1 L} + \frac{G_1}{r_1} \left( 1 - e^{-r_1 L} \right) + \Psi_2 \right] \]

and

\[ g_6 = \frac{1}{2 \sinh(r_1 L)} \left[ \Psi_1 e^{r_1 L} - \frac{G_1}{r_1} \left( 1 - e^{r_1 L} \right) - \Psi_2 \right]. \]

At the boundary between regions (I) and (III), the electric field should be continuous

\[ \frac{d\Psi_{e2}(y)}{dy} \bigg|_{y=0} = \frac{d\Psi_{e3}(y)}{dy} \bigg|_{y=0}. \]

Similarly, at the boundary between regions II and III, the electric field should be continuous

\[ \frac{d\Psi_{e2}(y)}{dy} \bigg|_{y=L} = \frac{d\Psi_{e3}(y)}{dy} \bigg|_{y=L}. \]

Therefore, from the continuity of the electric field at the boundaries, the surface electrostatic potential at two ends of region (III) can be expressed

\[ \Psi_1 = H_0 + H_1 \Psi_{e1} + H_2 \Psi_{e2} \]

\[ \Psi_2 = H_3 + H_4 \Psi_{e1} + H_5 \Psi_{e2} \]

\[ \text{where} \]

\[ H_0 = \frac{1}{\Omega} \left[ r_1 \coth(r_1 L) + \frac{r_1}{K} \coth \left( \frac{r_1}{K} L_d \right) \right] V_{00} \]

\[ + \frac{V_{10}}{\sinh(r_1 L)} \]

\[ H_1 = \frac{1}{\Omega} \left[ r_1 \coth(r_1 L) + \frac{r_1}{K} \coth \left( \frac{r_1}{K} L_d \right) \right] V_{01} \]

\[ + \frac{V_{11}}{\sinh(r_1 L)} \]

\[ H_2 = \frac{1}{\Omega} \left[ r_1 \coth(r_1 L) + \frac{r_1}{K} \coth \left( \frac{r_1}{K} L_d \right) \right] V_{02} \]

\[ + \frac{V_{12}}{\sinh(r_1 L)} \]

\[ H_3 = \frac{1}{\Omega} \left[ r_1 \coth(r_1 L) + \frac{r_1}{K} \coth \left( \frac{r_1}{K} L_d \right) \right] V_{10} \]

\[ + \frac{V_{00}}{\sinh(r_1 L)} \]

\[ H_4 = \frac{1}{\Omega} \left[ r_1 \coth(r_1 L) + \frac{r_1}{K} \coth \left( \frac{r_1}{K} L_d \right) \right] V_{11} \]

\[ + \frac{V_{01}}{\sinh(r_1 L)} \]

\[ H_5 = \frac{1}{\Omega} \left[ r_1 \coth(r_1 L) + \frac{r_1}{K} \coth \left( \frac{r_1}{K} L_d \right) \right] V_{12} \]

\[ + \frac{V_{02}}{\sinh(r_1 L)} \]

\[ \Omega = \left[ r_1 \coth(r_1 L) + \frac{r_1}{K} \coth \left( \frac{r_1}{K} L_d \right) \right] \cdot \left[ r_1 \coth(r_1 L) + \frac{r_1}{K} \coth \left( \frac{r_1}{K} L_d \right) \right] \]

\[ - \left[ \frac{r_1}{\sinh(r_1 L)} \right]^2 \]

\[ V_{00} = \frac{1}{2 \sinh(r_1 L)} \left[ \frac{G_{00}}{r_1} + \frac{r_1}{\sinh \left( \frac{r_1}{K} L_d \right)} \cdot \left[ 1 - \cosh \left( \frac{r_1}{K} L_d \right) \right] \right] \cdot \left[ q N_D e_{so} + \phi_f + \frac{2 \alpha_0 e_{so}}{r_1} \right] \]

\[ V_{01} = \frac{1}{\sinh(r_1 L)} \left[ \frac{G_{01}}{r_1} + \frac{r_1}{\sinh \left( \frac{r_1}{K} L_d \right)} \cdot \left[ 1 - \cosh \left( \frac{r_1}{K} L_d \right) \right] \right] \cdot \left[ \frac{2 \alpha_0 e_{so}}{r_1^2} \right] \cdot \left[ \frac{C_s + C_{hox}}{2C_s + C_{hox}^2} \right] \]

\[ V_{02} = \frac{1}{\sinh(r_1 L)} \left[ \frac{G_{02}}{r_1} + \frac{r_1}{\sinh \left( \frac{r_1}{K} L_d \right)} \cdot \left[ 1 - \cosh \left( \frac{r_1}{K} L_d \right) \right] \right] \cdot \left[ \frac{2 \alpha_0 e_{so}}{r_1^2} \right] \cdot \left[ \frac{C_s + C_{hox}}{2C_s + C_{hox}^2} \right] \]

\[ V_{10} = \frac{1}{\sinh(r_1 L)} \left[ \frac{G_{00}}{r_1} + \frac{r_1}{\sinh \left( \frac{r_1}{K} L_d \right)} \cdot \left[ 1 - \cosh \left( \frac{r_1}{K} L_d \right) \right] \right] \cdot \left[ q N_D e_{so} \right] \cdot \left( \frac{2 \alpha_0 e_{so}}{r_1^2} \right) \]

\[ V_{11} = \frac{1}{\sinh(r_1 L)} \left[ \frac{G_{02}}{r_1} + \frac{r_1}{\sinh \left( \frac{r_1}{K} L_d \right)} \cdot \left[ 1 - \cosh \left( \frac{r_1}{K} L_d \right) \right] \right] \cdot \left[ \frac{2 \alpha_0 e_{so}}{r_1^2} \right] \cdot \left[ \frac{C_s + C_{hox}}{2C_s + C_{hox}^2} \right] \]

\[ V_{12} = \frac{1}{\sinh(r_1 L)} \left[ \frac{G_{01}}{r_1} + \frac{r_1}{\sinh \left( \frac{r_1}{K} L_d \right)} \cdot \left[ 1 - \cosh \left( \frac{r_1}{K} L_d \right) \right] \right] \cdot \left[ \frac{2 \alpha_0 e_{so}}{r_1^2} \right] \cdot \left[ \frac{C_s + C_{hox}}{2C_s + C_{hox}^2} \right] \]

\[ D. \text{ Threshold Voltage} \]

For an FD SOI nMOS device, its threshold voltage is defined as the gate voltage when the minimum surface electrostatic potential reaches \( \Psi_{e2,min} = \phi_{fn} \), where \( \phi_{fn} = (kT/q) \ln(m_0/N_A) \) and \( N_A \) is the doping density of the p-type thin-film. Therefore, the minimum surface electrostatic potential is \( \Psi_{e2,min} = 2\sqrt{E_{\text{sub}} - (G_1/r_1^2)} \), which is equal to \( \phi_{fn} \) at the threshold voltage. Consequently, the threshold voltage is

\[ V_{th} = -L_1 + \sqrt{L_1^2 - 4L_0 L_2} + \phi_{fn} \]
III. MODEL EVALUATION AND DISCUSSION

In order to assess the validity of the analytical model considering the fringing electric field effect from the sidewall oxide spacer, the analytical model results have been compared with the 2-D simulation results. Fig. 3 shows the surface electrostatic potential at the front gate oxide/thin-film interface in the lateral channel region of the FD SOI nMOS device with the parameters as described in the caption of Fig. 1, for the doping densities of $2 \times 10^{18}$ cm$^{-3}$ and $8 \times 10^{17}$ cm$^{-3}$ in the n-LDD region, with its gate biased at the threshold voltage and its drain at $V_{DS} = 0.1$ V, based on the model and 2-D simulation results.

![Surface Electrostatic Potential](image1)

**Fig. 3.** Surface electrostatic potential at the front gate oxide/thin-film interface in the lateral channel region of the FD SOI nMOS device with the parameters as described in the caption of Fig. 1, for the doping densities of $2 \times 10^{18}$ cm$^{-3}$ and $8 \times 10^{17}$ cm$^{-3}$ in the n-LDD region, with its gate biased at the threshold voltage and its drain at $V_{DS} = 0.1$ V, based on the model and 2-D simulation results.

For the doping densities of $2 \times 10^{18}$ cm$^{-3}$ and $8 \times 10^{17}$ cm$^{-3}$ in the n-LDD region, with its gate biased at the threshold voltage—$V_{TH} = 0.193$ V and $V_{TH} = 0.1$ V, based on the model and the 2-D simulation results. As shown in the figure, at a lower n-LDD doping density of $8 \times 10^{17}$ cm$^{-3}$, the depletion region of the n-LDD region ($L_d$) increases. Therefore, the voltage drop in the n-LDD depletion region becomes larger—the effective drain voltage decreases, which leads to a lower minimum surface electrostatic potential in the channel. For the model results considering the fringing electric field effect at the interface between the n-LDD depletion region and the sidewall oxide spacer, extra flux exists—effective charge increases in the n-LDD depletion region, which can be understood from Gauss law. As a result, the effective drain voltage in the channel region as compared to the case without considering the fringing electric field effect. Therefore, considering the fringing electric field effect, the minimum surface electrostatic potential in the channel is higher—a lower threshold voltage. The fringing electric field effect gets stronger for the case with a lower doping density in the n-LDD region.

![Threshold Voltage](image2)

**Fig. 4.** Threshold voltage versus channel length of the FD SOI nMOS device with various thin-film doping densities, gate oxide thicknesses and n-LDD doping densities, biased at $V_{TH} = 0.1$ V based on the experimental data (solid square), the 2-D simulation results (solid circle), and the model results considering the fringing electric field effect (solid line) and without (dashed line).

IV. CONCLUSION

In this paper, analysis of the fringing electric field effect on the threshold voltage of FD SOI nMOS devices with various thin-film doping densities, gate oxide thicknesses and n-LDD doping densities, biased at $V_{TH} = 0.1$ V based on the experimental data (solid square), the 2-D simulation results (solid circle), and the model results considering the fringing electric field effect (solid line) and without (dashed line).

**REFERENCES**


CMOS scaling requirements of small EOT and acceptable gate leakage current [1]. These materials include oxynitrides with high nitrogen content (3.9 < \kappa < 7.5), and metal oxides such as HfO2 (20 < \kappa < 30). Among other process and integration problems, mobility (performance) reduction is particularly challenging to using these materials for high performance CMOS applications [1]. In developing these dielectrics, it is common to compare their performance against baseline or benchmark dielectrics (pure or lightly nitrided thermal SiO2) that have effective mobility near the universal limit.

In many cases, the evaluation of the performance of alternative gate dielectrics is based on the maximum linear transconductance (g_{\text{max}}) and drive current (I_{\text{d}}) of long channel devices as an alternative to comparing effective mobility (\mu_{\text{eff}}) [2]–[5]. This is usually done for practical reasons where fast and statistically sound data can be measured using automatic wafer-level testers. In order to normalize for differences in oxide thickness, such an evaluation assumes the standard scaling relationships for g_{\text{max}} and I_{\text{d}} with T_{\text{ox}}inv, i.e.,

\[ g_{\text{max}} \propto T_{\text{ox}}^{-1} \]
\[ I_{\text{d}} \propto T_{\text{ox}}^{-1} \]

In this case, the performance of an alternative gate dielectric against a benchmark dielectric is evaluated by comparing g_{\text{max}} \propto T_{\text{ox}}inv and I_{\text{d}} \propto T_{\text{ox}}inv.

The validity of (1) is based on the simplifying assumptions of (3) and (4), and the validity of (2) is based on the simplifying assumption given by (4) and (5) [6]

\[ Q_i \mu_{\text{eff}} \ll \frac{\partial Q_i}{\partial V_g} \]
\[ \mu_{\text{eff}} \neq f(T_{\text{ox}}) \]
\[ \mu_{\text{eff}} \neq f\left(\frac{V_g - V_T}{I_{\text{d}} T_{\text{inv}}}\right) \]

The assumptions given by (3)–(5) may not hold for aggressively scaled oxides as evidenced by experimental data [2], [7]–[9]. The observed experimental dependence of \mu_{\text{eff}} on V_T (3) at low fields will result in a slight deviation from (1). The observed experimental dependence of \mu_{\text{eff}} on T_{\text{ox}}inv (4) has been related to a variety of scattering mechanisms. Scattering mechanisms that can be affected by process parameters include Columbic scattering due to fixed and interfacial oxide charges or ionized channel impurities (\mu_{\text{C}}), and interface roughness at the oxide/channel interface (\mu_{\text{R}}) [8]. Scattering mechanisms that are due to inevitable physical mechanisms include remote charge scattering (RCS) due to charge impurities in the gate material [10], [11]. The RCS mobility (\mu_{\text{RCS}}) has a strong dependence on physical oxide thickness, significantly degrading mobility for oxides less than 20 Å [10], [11]. The effect of remote charge scattering on the scaling of g_{\text{max}} with T_{\text{ox}}inv is demonstrated in the simulation results of Fig. 1, where inclusion of the RCS effect results in sub-ideal scaling of the form g_{\text{max}} \propto T_{\text{ox}}^{\alpha} with \alpha < 1. It can be seen that \alpha is dependent on the theoretical model used to estimate the RCS mobility component for given channel and polysilicon gate doping densities.

The universal experimental dependence of \mu_{\text{eff}} on electric field (\mathcal{E} = 1/\varepsilon Si Q_B + 1/nQ_i) \approx (V_g - V_T)/6GT_{\text{ox}} was shown to result in smaller \mu_{\text{eff}} (at constant V_g - V_T) for thinner T_{\text{ox}}inv [12], [13]. This dependence results in subideal scaling of I_{\text{d}} with T_{\text{ox}}inv (i.e., I_{\text{d}} \propto T_{\text{ox}}^{-1} with \beta = 0.8) [12], [13]. The value of \beta can be reduced further if process parameters were not optimized to maintain the same \mu_{\text{eff}} for thin and thick oxides.

Based on the above discussion, it is postulated that simple semi-empirical power laws may be used to describe the scaling of g_{\text{max}} and...