specifications for the return losses are 20 dB. For the above data, the insertion loss at infinite frequency is 22.76 dB, corresponding to $|K| = 0.0364174$ or $|K| = 27.4594006$ (1). According to (4), for $N=4$ there are 60 different networks. Fig. 1 shows three possible implementations for three different positions of the K inverter and the same order in the extraction of the poles corresponding to transmission zeros at w_1, w_2, w_3 and w_4 . All the circuitual values are collected in Table 1. The theoretical response of the lowpass prototype is the same for the three implementations and is shown in Fig. 2. For instance, in the implementation A, after extracting the three first poles ($\phi_1, b_1, \phi_2, b_2, \phi_3, b_3$) a phase shifter (ϕ_5) at infinite frequency is extracted. Then, the network is turned, the fourth pole is extracted (ϕ_4, b_4), and the other phase shifter at infinite (ϕ_6) is obtained. Finally, the unit inverter and the K inverter extractions are accomplished. The cascading of the unit inverter and the phase shifter ϕ_6 is equivalent to a phase shifter of value ($\phi_6 \pm \pi/2$) and the phase shifters ϕ_1 and ϕ_4 can be ignored since they are located at input and output, respectively.

Table 1: Circuit element values for three implementations A, B, C

Implementation A	Implementation B	Implementation C
$\phi_1 = -22.396656^\circ$	$\phi_1 = -22.396656^\circ$	$\phi_1 = -22.396656^\circ$
$b_1 (w_1) = 7.418234$	$b_1 (w_1) = 7.418234$	$b_1 (w_1) = 7.418234$
$\phi_2 = 19.763480^\circ$	$\phi_2 = 19.763480^\circ$	$\phi_2 = 19.763480^\circ$
$b_2 (w_2) = 58.955954$	$b_2 (w_2) = 58.955954$	$b_2 (w_2) = 58.955954$
$\phi_3 = 2.281133^\circ$	$\phi_3 = -34.824057^\circ$	$\phi_3 = 2.281133^\circ$
$b_3 (w_3) = 336.725069$	$b_3 (w_3) = 2.813465$	$b_3 (w_3) = 336.725069$
$\phi_4 = -50.564385^\circ$	$\phi_4 = 25.688594^\circ$	$\phi_4 = 0.2895468^\circ$
$b_4 (w_4) = 1.142814$	$b_4 (w_4) = 8.361019$	$b_4 (w_4) = 514.012924$
$\phi_5 = -89.647957^\circ$	$\phi_5 = -87.366823^\circ$	$\phi_5 = -89.937504^\circ$
$\phi_6 = 50.564385^\circ$	$\phi_6 = 9.135462^\circ$	$\phi_6 = 0^\circ$
$K = -3.641740088 \times 10^{-2}$	$K = -3.641740088 \times 10^{-2}$	$K = -3.641740088 \times 10^{-2}$

In all cases, ϕ_5 and ϕ_6 are phase shifters extracted at $s = j\infty$

Fig. 1 Three different lowpass networks of fourth order filter

a K inverter between third and fourth poles
b K inverter between second and third poles
c K inverter between fourth pole and output

Fig. 2 Theoretical response of lowpass prototype for three implementations

Conclusion: A systematic procedure for the synthesis of N -order filters with N transmission zeros at finite real frequencies by means of the extracted-pole technique has been presented. A procedure to ensure the behaviour of this kind of filters for infinite frequency has been presented. To validate it, three different implementations of a fourth order filter with four transmission zeros have been calculated.

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Ultra-low-voltage SOI CMOS inverting driver circuit using effective charge pump based on bootstrap technique

J.H.T. Chen and J.B. Kuo

A novel SOI CMOS inverting driver circuit is reported using a concise charge pump based on bootstrap technique (CPBT) for ultra-low-voltage (ULV) VLSI applications. The ULV driver with CPBT composed of a bootstrap capacitor, a pre-charge device and a driver device, provides a four times speed improvement as compared to a counterpart circuit using the direct bootstrap technique at an output load of 100 fF operating at 0.5 V.

Introduction: SOI CMOS circuits are receiving much attention owing to their potentials for low-voltage VLSI applications [1]. Several low-voltage driver circuits based on the dynamic threshold MOS (DTMOS) technique [2] and the bootstrap technique have been reported [3, 4–6]. Although they are aimed for sub-1 V operation, they may not be effective for use in a driver circuit using a power supply voltage as low as 0.5 V, comparable or smaller than the magnitude of the threshold voltage of the devices [2, 4–6]. In this Letter, a novel SOI CMOS inverting driver circuit using a concise charge pump based on CPBT for ultra-low-voltage (ULV) VLSI applications is described. It will be shown that, compared with a counterpart circuit using the direct bootstrap technique, this ULV driver with charge pump based on bootstrap technique (CPBT) provides a four times speed improvement.

ULV SOI driver with CPBT: Fig. 1 shows the ULV SOI CMOS inverting driver circuit using a charge pump based on the bootstrap technique (CPBT). As shown in the Figure, in addition to the conventional devices P1 and N1, the ULV driver circuit is composed of two CPBT circuits for magnifying the input signals to overcome the shortage of the gate voltage over-drive problems for ULV operation such as 0.5 V, which is comparable to or smaller than the magnitude of the threshold voltage of the devices used. The top CPBT circuit, which enhances the pull-down of the output, is made of the bootstrap capacitor C_{B1} , pre-charge device P3, and driver device N2 with its

body controlled by the internal node V_B . The bottom CPBT circuit, which enhances the pull-up of the output, is made of the bootstrap capacitor C_{B2} , pre-discharge device N3 and driver device P2 with its body controlled by the internal node V_A . Using the two CPBT circuits at top and bottom, the problem associated with the shortage of gate voltage over-drive has been resolved.

Fig. 1 ULV SOI CMOS inverting driver circuit using CPBT

Fig. 2 Waveforms during pull-up and pull-down transients of ULV SOI CMOS inverting driver circuit with CPBT operating at V_{dd} of 0.5 V

Performance and discussion: To assess the performance of this ULV circuit with CPBT, a test circuit using 0.5 V power supply voltage with a capacitive load of 0.1 pF at the output node, based on a 0.18 µm SOI CMOS technology has been designed. The channel length of all devices in the circuit is 0.18 µm. The channel width of each NMOS/PMOS device is listed in Fig. 1. Fig. 2 shows the waveforms during pull-up and pull-down transients of the ULV SOI CMOS inverting driver circuit with CPBT operating at V_{dd} of 0.5 V. Fig. 3. shows the equivalent circuits of the ULV CMOS inverting driver circuit with CPBT operating at V_{dd} of 0.5 V at the time (i) prior to the pull-up transient and (ii) after the input ramp-down period. As shown in Fig. 3a, prior to the pull-up transient at t_1 , V_{IN} is high (0.5 V), P3 is off and the pre-discharge device N3 in the bottom CPBT circuit turns on. Thus, the internal V_B , which is at the right side of the bootstrap capacitor C_{B2} , is set to 0 V. Therefore the bootstrap capacitor C_{B2} is charged with its left side set to 0.5 V. Under this situation, the driver device P2 turns off since the magnitude of its threshold voltage is increased to 0.75 V due to pull-high of its body. At this time, the output node is set to 0 V via devices N1 and N2. As shown in Fig. 3b, after the input ramp-down period, V_{IN} is 0 V, N3 turns off. Owing to the charge stored in the bootstrap capacitor C_{B2} , the internal node becomes negative. Thus the driving capability of device P2 is enhanced and the output node is quickly pulled up to 0.5 V. At the same time, the internal node V_A is pulled high via device P3 such that the bootstrap capacitor C_{B1} is charged for the next operation. Note although V_A is high, device N2 is off due to the increased threshold voltage since its body is pulled to below 0 V. The

pull-down transient has a complementary configuration. Fig. 4 shows the propagation delay time against power supply voltage of the ULV CMOS inverting driver circuit with CPBT. Also shown in the Figure are the results for the counterparts using conventional CMOS devices and the direct bootstrap technique [3]. As shown in the Figure, the CPBT approach is most effective at ultra-low voltages. At the power supply voltage of 0.5 V, the CPBT approach provides a four times speed improvement as compared to a counterpart circuit using the direct bootstrap technique with an output load of 100 fF. As shown in the Figure, the CPBT can work at the power supply voltage as low as 0.3 V, which is below the magnitude of the threshold voltage of the CMOS devices (0.5 V) while other approaches stop working at 0.4 V.

Fig. 3 Equivalent circuits of ULV SOI CMOS inverting driver circuit with CPBT operating at V_{dd} of 0.5 V

a Time prior to pull-up transient
b Time after input ramp-down period

Fig. 4 Propagation delay time against power supply voltage of ULV SOI CMOS inverting driver circuit with CPBT

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Versatile high voltage level shift and driver for MEMS applications

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A high voltage (>50 V) driver with a simple interface to 5 V or 3.3 V conventional CMOS is described. Unlike previous such circuits, the static current is zero for full CMOS compatibility. The circuit has been realised on a multi-sourced high voltage CMOS process.

Most IC processes operate on 5 V, 3.3 V or less. However, there are increasing numbers of applications, primarily in the MEMS field, where transducers must be driven at 20 to 50 V. Some silicon foundries recognise this, and offer process variants for 50 V or more, typically by extending gate, source and drain regions to accommodate the higher voltages, and by selective gate oxide thicknesses.

A key element in the development of MEMS driver circuits is the level shift. This must operate on CMOS input voltage levels, 0–5 V or 0–3.3 V, and must drive the output transistors so that the full supply voltage swing, which may be 50 V, is available at the circuit output port. It must perform this function in a speed-power efficient way, and most desirably, it should have CMOS-like current characteristics, i.e. it is acceptable to take greater current at higher clock speeds, but when the clock is very slow, or consists of infrequent pulses, the circuit should take current only on voltage transitions. It should also operate without modifications from a wide range of high voltage supply voltages.

A cross-coupled latch driver structure has been used for this function [1]. However, it takes a standing current which, for fast operation, should be relatively high; typical values are 0.5 mA per output. In many circuits this is impractical.

A simpler circuit has been used which avoids the standing current problem, while offering higher speed for a given current and smaller chip area. It will operate up to a supply voltage just below the gate-source breakdown voltage of the critical devices, which are usually the PMOS output transistors in an N-well process. Provided that this voltage is not exceeded, the operation is entirely CMOS-like, i.e. the current is exactly proportional to frequency over at least 5 decades, and is practically zero when not clocked. Although high voltage devices are not fast, the circuit can clock at 2 MHz with a heavy capacitive load (30 pF) and shows no instability.

The circuit operation is shown in Fig. 1. M1–M4 provide two conventional inverters at 5 V, using 0.8 μm channel devices from the target process, austriamicrosystems CXZ. M5 and M6 feed the level shift, which is performed by M9 and M10, acting as cross-coupled latches with the P-channel output transistors M11 and M12. M7 and M8 provide the N-channel output drivers. The circuit function as shown has two complementary outputs, a typical requirement for MEMS switch drivers, where one unit is switched on while the other turns off. Output devices M7/M11 and M8/M12 have been optimised for driving capacitive loads, and so are larger than minimum size, respectively M7 and M8 are $40 \times 3 \mu\text{m}$ and M11/M12 are $40 \times 5 \mu\text{m}$. A single driver would still need an inverted drive for the level shift, but would omit half of the transistors in the level shift and output stages.

Fig. 1 Double output driver circuit diagram

The drains of transistors M5–M8 can see the full supply voltage, so the overall requirement was satisfied by a thin gate oxide, high voltage drain NMOS device, which can operate with >50 V supply. This device has a low enough threshold voltage that it can be driven by 5 V or even 3.3 V inputs. The PMOS output drivers require a high gate-source breakdown, so a thicker gate oxide device was used. Drain-source breakdown for this device was >50 V, with gate oxide breakdown of 40 V minimum.

The high voltage supply current, feeding in this case four dual complementary output stages, was plotted against the supply voltage, for a range of clock frequencies. This is shown in Fig. 2. As in conventional CMOS, the supply current rose linearly with frequency and with supply voltage up to 40 V. At 50 V supply, the current was still frequency related, but was noticeably greater than at the lower voltages. On a sample of devices, at 55 V a catastrophic breakdown occurred, which was not reversible. While this result is process dependent, the increasing availability of such processes indicates that the voltage limitation may be lifted to 90 V or more in the immediate future.

Fig. 2 Current against clock frequency for four dual drivers

Average risetime over a small number of samples was 123 ns, $\sigma = 2.5$ ns, and falltime 155 ns, $\sigma = 3.8$ ns. The current for four complementary outputs was 3.9 mA, i.e. just under 0.5 mA per output. The current increased to 4.7 mA with the connection of the 20 pF scope probe. Faster rise/fall times were observed using a 2 pF FET probe, but this was limited to 20 V swing. The lower capacitance load results are more indicative of real MEMS microsystems operation.