0.83, 1.575 and 1.7 GHz, respectively, and the 3 dB beamwidths in the E-plane patterns are 75.5°, 60.5°, 50° and in the H-plane patterns 66.5°, 46.5° and 44.5° at 0.83, 1.575 and 1.7 GHz, respectively.

Fig. 1 TSMPA
a Exploded view of TSMPA
b Equivalent circuit of rectangular patch fed by slot in ground plane

Fig. 2 Measured and simulated results of TSMPA

Fig. 3 Measured E-plane radiation pattern of TSMPA

Conclusions: The TSMPA is presented for use in multiband systems. It consists of three microstrip patches. The first patch is excited by the aperture coupled feeding method to produce wide-band characteristics, the second patch is coupled with the first and the third patches using a slot-line on the middle patch. The centre patch is designed to be resonant at lower frequencies, while the first and third patches resonate at the upper frequencies of interest. Using knowledge of the conventional optimisation method for an input impedance, the TSMPA has been optimised for wide-band performance, and the foam dielectric substrate is inserted into each patch to use the commercially available substrate RT/Duroid 5800. The size of the TSMPA is $150 \times 150 \times 34$ mm and the measured bandwidths, with return losses less than -10 dB, are 0.785–0.855 GHz and 1.535–1.715 GHz. The measured radiation patterns have approximately the same radiation characteristics at cellular, GPS and PCS frequencies and the measured 3 dB beamwidths in the E-plane patterns are 75.5°, 60.5°, 50° and in the H-plane patterns 66.5°, 46.5° and 44.5° at 0.83, 1.575 and 1.7 GHz, respectively. The measured results prove that the TSMPA, which was designed and fabricated, can be used in a multiband system.

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Han-Cheol Ryu (Electronics and Telecommunications Research Institute, Taejeon, Korea)

Hee-Ran Ahn, Sang-Hwa Lee and Wee Sang Park (Dept. of E&E Engineering, POSTECH (Pohang University of Science and Technology), Pohang, Korea)

E-mail: wsp@postech.ac.kr

References

- MURAKAMI, Y., CHUJO, W., and FUJISE, M.: 'Mutual coupling between two ports of dual slot coupled circular patch antennas'. IEEE AP-S Int. Sym. Digest, 1993, pp. 1469–1472
- TARGONSKI, S.D., WATERHOUSE, R.B., and POZAR, D.M.: 'Design of wide-band aperture-stacked patch microstrip antennas', *IEEE Trans. Antennas. Propag.*, 1998, **46**, (9), pp. 1245–1251
- CHO, Y.K., SON, G.H., CHAE, G.S., YUN, L.H., and HONG, J.: 'Improved analysis method for broadband rectangular microstrip antenna geometry using E-plane gap coupling', *Electron. Lett.*, 1993, **29**, pp. 1907–1909
- POZAR, D.M., and DUFFY, S.M.: 'A dual band circularly polarized aperture-coupled stacked microstrip antenna for global positioning satellite', *IEEE Trans. Antennas. Propag.*, 1997, **45**, (11), pp. 1618–1625
- GARGO, R., BHARTIA, P., BAHL, I., and ITTIPOON, A.: 'Microstrip antenna design handbook' (Artechhouse, London, Boston, 2001), pp. 539–536

0.8 V CMOS adiabatic differential switch logic circuit using bootstrap technique for low-voltage low-power VLSI

Y. Zhang, H.H. Chen and J.B. Kuo

A novel 0.8 V CMOS adiabatic differential switch logic (ADSL) circuit using the bootstrap technique for low-voltage low-power VLSI is reported. Using capacitance coupling effects from the bootstrap transistors with the related isolating transistors, this 0.8 V ADSL circuit has a 52% smaller propagation delay time, consuming 26% less power as compared to the energy efficient logic circuit.

Introduction: Low voltage and low power are the current trends in CMOS VLSI circuits [1]. CMOS adiabatic logic circuits are effective in achieving these goals in low power consumption [1]. A 1.5 V energy efficient logic (EEL) circuit based on CMOS adiabatic differential switch logic (DSL) circuits has been reported [2]. Designing CMOS adiabatic circuits using down-scaled CMOS devices with a sub-1 V power supply voltage is challenging since the magnitude of the threshold voltage of the CMOS devices cannot be scaled down

accordingly with the power supply voltage. Recently, bootstrap techniques have been used to enhance the speed performance of a CMOS driver circuit with a large capacitive load using a low power supply voltage [3, 4]. In this Letter, a 0.8 V CMOS adiabatic differential switch logic (ADSL) circuit using cross-coupled bootstrap transistors and related isolating transistors is described.

Fig. 1 0.8 V CMOS ADSL circuit

0.8 V CMOS ADSL circuit: Fig. 1 shows the 0.8 V CMOS ADSL circuit using the bootstrap technique. As shown in the Figure, four cascading ADSL cells are controlled by four four-phase clocks. For two adjacent ADSL cells, their related clocks are different by one sequential phase. The ADSL cell is derived from a DSL circuit with the cross-coupled bootstrap transistors MN3 and MN4 and two NMOS devices MN5 and MN6 for providing isolation from the input devices. In addition, two PMOS devices MP1 and MP2 are with their body tied to source, instead of being connected to V_{dd} as in the EEL circuit [2]. The four phases of each clock are (1) wait, (2) precharge, (3) evaluate and (4) recover. During the wait phase, all devices are off and the output nodes OUT and OUT' are 0 V. In the precharge phase, the power clock (PC) gradually increases from 0 V to 0.8 V. If the input IN is high and the input IN' is low, the NMOS device MN7 is on and the NMOS device MN8 is off. When the NMOS devices MN3–MN6 are on, the output node OUT is discharged to ground and OUT' is rising since the PMOS device MP1 is off and the PMOS device MP2 is on. When the power clock enters the evaluate phase (PC is high), both OUT and OUT' maintain their states. When PC decreases from 0.8 V to 0 V, it enters the recover phase, which is for energy recycling. During the recover phase, when PC is greater than 0.4 V, the PMOS device MP2 maintains on and the charge previously stored in the output node OUT' flows upward to PC and OUT' decreases. When PC is smaller than 0.4 V, the PMOS device MP2, and the NMOS devices MN4, and MN6 turn off and the NMOS device MN2 turns on instead. Therefore, the upward flow of the charge continues—the output node OUT' continues to decrease. The inclusion of the NMOS devices MN5 and

MN6 is used to provide isolation of the output nodes from the input devices during the recovery phase. Owing to the capacitance coupling effects of the gate-drain capacitance (C_{gd}) of the bootstrap transistor MN4, the internal node BP2 may become smaller than 0 V. As a result, upward flow of the charge stored at the output node OUT' is enhanced. In addition, during the next precharge phase, the negative potential of the internal node BP2 may help the output node OUT' be pulled up faster. Furthermore, the energy consumption of the ADSL cell is smaller as compared to the EEL circuit [2] since the body of the PMOS devices MP1 and MP2 is connected to the source, which is the power clock (PC) instead of V_{dd} .

Fig. 2 Transient waveforms of 0.8 V CMOS ADSL circuit

Fig. 3 Consumed energy of 0.8 V CMOS ADSL circuit

Performance and discussion: To assess the performance of the ADSL circuit using bootstrap technique, a test circuit based on a 0.18 μm CMOS technology has been designed. The channel length of all devices in the circuit is 0.18 μm . The channel width of the NMOS/PMOS devices is 0.5 $\mu\text{m}/1 \mu\text{m}$. A capacitive load of 10 fF is placed at the output node. Fig. 2 shows the transient waveforms of the 0.8 V CMOS ADSL circuit based on SPICE simulation results. As shown in the Figure, when IN is 0.8 V and IN' is 0 V, during the recover phase (PC1 switching from 0.8 V to 0 V), the internal node BP2 may be below 0 V due to the capacitance coupling effect from the gate-drain capacitance C_{gd} of the bootstrap transistor MN4. When IN is 0 V and IN' is 0.8 V, a complementary result can be seen—the internal node BP1 may be below 0 V due to the effect from the bootstrap transistor MN3. Using the bootstrap transistors in the ADSL circuit, during the precharge and the recover phases, the output node settles to the final state faster. Define the propagation delay time as the time from the 0.72 V (90%) of PC1 to 0.72 V (90%) of OUT' in the precharge phase. Using the bootstrap transistors, the propagation delay time of the ADSL circuit is always smaller as compared to the EEL circuit [2]. At 0.8 V, the propagation delay time of the ADSL circuit is 52% shorter. Therefore, the bootstrap technique is effective in enhancing the speed performance of the ADSL circuits. Fig. 3 shows the consumed energy of the 0.8 V CMOS ADSL circuit using the bootstrap technique. As shown in the Figure, within a time window of

100 ns, the ADSL circuit consumes 31 fJ, which is 26% smaller than that for the EEL (42 fJ). The smaller consumed energy of the ADSL circuit is due to the body-source connected configuration of the PMOS devices MP1 and MP2, instead of the body- V_{dd} connected one as in the EEL circuit. In addition, owing to the isolation of the output nodes from the input devices provided by the NMOS devices MN5 and MN6, recycling of the charge stored at the output nodes has been carried out more efficiently.

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Y. Zhang, H.H. Chen and J.B. Kuo (Dept. of Electrical & Computer Engineering, Univ. of Waterloo, Waterloo, Ontario N2L 3G1, Canada)

H.H. Chen: Also with NTUET, Taipei 10617, Taiwan

J.B. Kuo: On leave from NTUET, Taipei 10617, Taiwan

E-mail: jbkuo@uwaterloo.ca

References

- 1 KUO, J.B., and LOU, J.H.: 'Low-voltage CMOS VLSI circuits' (Wiley, New York, 1999)
- 2 YEH, C.C., LOU, J.H., and KUO, J.B.: '1.5 V CMOS fully-swinging energy efficient logic (EEL) circuit suitable for low-voltage and low-power VLSI application', *Electron. Lett.*, 1997, **33**, (16), pp. 1375–1376
- 3 LAW, C.F., YEO, K.S., and SAMIR, R.S.: 'Sub-1 V bootstrapped CMOS driver for giga-scale-integration era', *Electron. Lett.*, 1999, **35**, (5), pp. 392–393
- 4 YEO, K.S., MA, J.G., and DO, M.A.: 'Ultra-low-voltage bootstrapped CMOS driver for high performance applications', *Electron. Lett.*, 2000, **36**, (8), pp. 706–707

BCI test conforming with statistical estimates of random-field radiation

S. Pignari and G. Spadacini

Bulk current injection (BCI) and field-to-wire coupling of radiated electromagnetic interference (EMI) are compared. An EMI description in terms of random plane waves is used to state the equivalence. Analytical, frequency piecewise-linear BCI feeding conditions are derived such that interference induced in the equipment under test conforms to statistical estimates of radiation-induced effects.

Introduction: Bulk current injection (BCI) is often used for susceptibility assessment of electronic equipment to external electromagnetic interference (EMI). According to this technique, interference is generated with a radio-frequency (RF) signal source and injected in the equipment under test (EUT) via a probe, clamped on the wiring harness connecting the EUT to auxiliary equipment (AE). Contrary to conventional susceptibility-tests in which EMI is radiated on the structure under analysis, BCI involves lower-cost instrumentation and simpler test procedures. However, in general injection and radiation produce different effects [1], and equivalence is theoretically achieved only with two injection probes and for unpractical feeding conditions [2, 3].

In this Letter, the statistical nature of EMI is recognised and used to state the equivalence between injection and radiation. EMI is described in terms of plane waves with random parameters [4], and simple/practical feeding conditions for the injection probe are derived, conforming to specific statistical estimates of interference induced in the EUT by radiation. It is shown that an RF voltage source with frequency piecewise-linear (PWL) profile is to be used in the BCI test, and closed-form expressions for mean value and dispersion of the EMI level induced in the EUT are derived.

Deterministic equivalence: The BCI test setup is modelled as shown in Fig. 1. Namely, EUT and AE are represented by lumped impedances (Z_{EUT} , Z_{AE}), the wiring harness is described by a single-conductor transmission line running above an infinite ground plane (ℓ , h , and Z_C being wire length, height, and characteristic impedance, respectively). For the sake of brevity, the more general

case of multiwire harness and matrix terminal impedances is not considered in this Letter. As in [1], the injection probe is modelled by a lumped voltage source V_P , placed at $z = p\ell$, $p \in [0, 1]$. The voltage V_P is related to RF voltage source V_S by $V_P = F(j\omega)V_S$, where

$$F(j\omega) = \frac{j\omega M_P}{(Z_S + j\omega L_P)} \quad (1)$$

In (1), $Z_S = 50 \Omega$ is the internal impedance of the RF voltage source, and L_P , M_P are the self- and mutual-inductance of the injection probe, respectively [5].

Fig. 1 Circuit model of BCI setup

For radiation concerns, EMI is modelled as a linearly polarised plane-wave electric field with strength E_0 , polarisation angle η , and incidence angles ϑ , ψ (see Fig. 1 of [2]).

The currents I_{EUT}^{BCI} and I_{EUT}^{rad} induced in the EUT by injection and radiation, respectively, are evaluated via the previously-described models. If equivalence is stated by imposing the same EUT current magnitude, i.e. $|I_{EUT}^{BCI}| = |I_{EUT}^{rad}|$, the following condition for the magnitude of voltage V_P is obtained:

$$|V_P| = E_0 h \left| H \left(\frac{\ell}{\lambda}; \vartheta, \psi, \eta, p, k_{AE} \right) \right| \quad (2)$$

Where

$$H = \frac{a_1 + a_2 e^{-j2\pi(1+m)\ell/\lambda} + a_3 e^{j2\pi(1-m)\ell/\lambda}}{(1 - k_{AE})e^{-j2\pi p\ell/\lambda} + (1 + k_{AE})e^{j2\pi p\ell/\lambda}} \quad (3)$$

$$\begin{aligned} a_1 &= 4[(m + k_{AE})q - s] \\ a_{2,3} &= 2(k_{AE} \mp 1)[\mp s - (1 \mp m)q] \\ m &= \sin \vartheta \cos \psi, \quad s = \sin \vartheta \cos \eta \\ q &= \frac{\cos \vartheta (\cos \vartheta \cos \psi \cos \eta + \sin \psi \sin \eta)}{(1 - m^2)} \end{aligned}$$

In (3), λ is the wavelength and $k_{AE} = Z_{AE}/Z_C$. Transfer ratio H depends on EUT-to-AE wiring electrical length ℓ/λ , external wave parameters ϑ , ψ , η , probe location p , and normalised AE impedance k_{AE} . Note that, since H does not depend on the EUT impedance Z_{EUT} , (2) and (3) prove that voltage V_P required for equivalence is not influenced by the EUT characteristics.

For low frequencies (i.e., for $\ell/\lambda \ll 1$), the following first-order expansion of the transfer ratio in (3) holds:

$$H_{LF} \cong j4\pi \frac{\ell}{\lambda} [\cos \eta (k_{AE} \sin \vartheta - \cos \psi) - \cos \vartheta \sin \psi \sin \eta] \quad (4)$$

Eqn. (4) indicates that for low frequencies $|H|$ increases linearly with +20 dB/dec slope, and equivalence between injection and radiation is achieved for a specific wave (ϑ , ψ , η), regardless of the position of the probe p . Nevertheless, numerical evaluation of (3) shows a complicated frequency shape of H in the standing-wave region of the EUT-to-AE interconnection and, in general, a strong variability with the wave parameters ϑ , ψ , η . This proves that an equivalence procedure founded on a deterministic basis is inherently poor. Such a limitation is overcome in the following Section, where the random nature of EMI is recognised and the probe-induced voltage $V_P(j\omega)$ is consequently determined in agreement with the statistics of the current level induced in the EUT by radiation.

Statistical equivalence: Since the angular wave parameters are usually unknown and uncontrolled, in the following these quantities are treated as random variables (RVs) with uniform probability