Plots of C_{ox} , C_m , and L versus resistance can be seen in Fig. 5. Also shown in Fig. 5, are the initial values, based of the typical technology parameters of Table I, used in the optimization routine derived from (3), (5) and (6) respectively. From this figure, it is seen that, as the resistance increases, so do the elements L and C_m , while C_{ox} decreases, in a linear fashion. Fig. 6 shows that the substrate resistance R_{Si} decreases, while the substrate capacitance C_{Si} increases as the resistance is increased by increasing the number of line lengths, N .

V. CONCLUSIONS

A scalable, physically based, lumped element model was presented that accurately models thin film meander-line resistors at microwave frequencies fabricated in a silicon technology process. The scalable model presented has been verified for various structure sizes. The simulated results are in good agreement with the measured results. This scalable model, with its model parameters, can be easily implemented as a subcircuit in SPICE, making this a good physical model for the RF circuit designer.

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REFERENCES

- [1] N. M. Nguyen and R. G. Meyer, "Si IC-compatible inductors and LC passive filters," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1028–1031, Aug. 1990.
- [2] R. A. Pucel, *Notes for Lectures Presented in Course on Microwave Circuit Design II—Nonlinear Circuits*. Berkeley, CA: Univ. California Press, 1984.
- [3] *NT25 Electrical Specifications and Layout Design Rules, Version ISO1.5*, Canadian Microelectronics Corp., Kingston, ON, Canada, 1999.
- [4] M. A. Margarit, J. L. Tham, R. G. Meyer, and M. J. Deen, "A low-noise low power VCO with automatic amplitude control for wireless applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 761–771, June 1999.
- [5] K. B. Ashby, I. A. Koullias, W. C. Finley, J. J. Basteck, and S. Moinian, "High Q inductors for wireless applications in a complementary silicon bipolar process," *IEEE J. Solid-State Circuits*, vol. 31, pp. 4–9, Jan. 1996.
- [6] J. N. Burghartz, M. Souyer, and K. A. Jenkins, "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 100–104, Jan. 1996.
- [7] H. Ronkainen, H. Kattelus, E. Tarvainen, T. Rihisaari, M. Andersson, and P. Kuivalainen, "IC compatible planar inductors on silicon," *Proc. Inst. Elect. Eng., Circuits Devices Syst.*, vol. 144, no. 1, pp. 1–7, Feb. 1997.
- [8] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of microstriplines on Si–SiO₂ system," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, pp. 869–881, Nov. 1971.
- [9] T. F. Coleman and Y. Li, "An interior, trust region approach for nonlinear minimization subject to bounds," *SIAM J. Optim.*, vol. 6, pp. 418–445, 1996.
- [10] C. H. Chen and M. J. Deen, "A general noise and S -parameter de-embedding procedure for on-wafer high-frequency noise measurements of MOSFET's," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1004–1005, May 2001.
- [11] D. K. Cheng, *Field and Wave Electromagnetics*. Reading, MA: Addison-Wesley, 1992, pp. 215–216.

Compact Threshold-Voltage Model for Short-Channel Partially-Depleted (PD) SOI Dynamic-Threshold MOS (DTMOS) Devices

James B. Kuo, Kuo-Hua Yuan, and Shih-Chia Lin

Abstract—This paper presents a closed-form threshold-voltage model for short-channel partially-depleted (PD) SOI dynamic-threshold MOS (DTMOS) devices based on a quasi-two-dimensional (2-D) approach. As verified by experimental data and 2-D simulation results, this compact model provides an accurate prediction of the threshold-voltage behavior of the short-channel PD SOI DTMOS devices. Based on the analytical model, as verified by the 2-D simulation results, PD SOI DTMOS devices have less short-channel effects including DIBL-induced short-channel effects as compared to the devices without the DTMOS configuration.

Index Terms—DIBL, DTMOS, PDSOI, quasi-2-D approach, short-channel effect.

I. INTRODUCTION

Partially-depleted (PD) SOI dynamic-threshold MOS (DTMOS) devices have been receiving a lot of attention owing to their potential for low-voltage VLSI circuit applications. Dynamic-threshold technique was first reported to improve the performance of PD SOI CMOS devices [1]. In the dynamic threshold MOS (DTMOS) technique, the body terminal is connected to the gate terminal making the threshold voltage as function of the gate voltage. PD SOI DTMOS devices can provide a larger drain current owing to a reduced threshold voltage at a gate voltage as compared to the device without the dynamic-threshold technique. Owing to their advantages, PD SOI DTMOS devices are especially suitable for realizing low-voltage (0.6 V or smaller) VLSI circuits. Recently, low-power VLSI circuits using PD SOI DTMOS devices have been reported [2]–[6]. However, no compact analytical threshold-voltage models exist for short-channel PD SOI DTMOS devices. In order to facilitate circuit simulation and to gain insights into device operation, in this paper, a closed-form threshold-voltage model for short-channel PD SOI DTMOS devices based on a quasi-2-D approach is described. In the following sections, the analytical model is derived first, followed by model verification and discussion.

II. MODEL DERIVATION

In a PD SOI DTMOS device biased under standard operating conditions, the silicon thin-film is partially depleted. Fig. 1 shows the cross section of the PD SOI DTMOS device. As shown in the figure, V_{sub} is the back gate voltage, which can be grounded or any supply voltage depending on the operating conditions of the DTMOS device. In order to facilitate model derivation, excluding the bottom neutral region, the silicon thin-film is divided into three regions—(I) the left fully-depleted region near the source ($0 < y < l_1$), (II) the top fully-depleted region near the surface ($l_1 < y < l_2$), and (III) the right fully-depleted region near the drain ($l_2 < y < L$). Assuming

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an abrupt pn junction approximation, the edges of the Region (I) and Region (III) are

$$l_1 = \sqrt{\frac{2\epsilon_s \left(\frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \right)}{q} \left(\frac{N_A + N_D}{N_A N_D} \right)}$$

and

$$l_2 = L - \sqrt{\frac{2\epsilon_s \left(\frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} + V_{DS} \right)}{q} \left(\frac{N_A + N_D}{N_A N_D} \right)}$$

where ϵ_s is silicon permittivity, q is electron charge, N_A is the doping density of the silicon thin-film, k is Boltzmann constant, T is temperature in Kelvin, n_i is the intrinsic concentration, and N_D is the n-type doping density of the source/drain region. Note that the source terminal is assumed to be grounded. The influence of V_{BS} on l_1 and l_2 is assumed to be negligible to simplify the analysis.

A. Region (I)— $0 < y < l_1$

Region (I) is the left fully-depleted region near the source ($0 < y < l_1$). In Region (I), 2-D Poisson's equation is:

$$\frac{\partial^2 \Psi_1(x, y)}{\partial x^2} + \frac{\partial^2 \Psi_1(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_s}. \quad (1)$$

The electrostatic potential in Region (I) can be approximated by the following equation [7]:

$$\Psi_1(x, y) = a_{01}(y) + a_{11}(y)x + a_{21}(y)x^2. \quad (2)$$

Three boundary conditions for 2-D Poisson's equation in Region (I) are: i) at the top surface, the surface electrostatic potential is $\Psi_1(0, y) = \Psi_{s1}(y)$, ii) at the top surface, its vertical electric field is

$$\left. \frac{\partial \Psi_1(x, y)}{\partial x} \right|_{x=0} = \frac{\epsilon_{ox}}{\epsilon_s} \frac{\Psi_{s1}(y) - \Psi_G}{t_{ox}}$$

where ϵ_{ox} is oxide permittivity, t_{ox} is gate oxide thickness, and Ψ_G is the gate electrostatic potential, iii) at the bottom of the thin-film, its vertical electric field is

$$\left. \frac{\partial \Psi_1(x, y)}{\partial x} \right|_{x=t_{si}} = \frac{\epsilon_{ox}}{\epsilon_s} \frac{\Psi_{sub} - \Psi_1(t_{si}, y)}{t_b}$$

where t_b is the thickness of the buried oxide, Ψ_{sub} is the electrostatic potential of the n-type substrate below the buried oxide, and t_{si} is the thickness of the thin-film. Solving 2-D Poisson's equation (1) with three boundary conditions and using (2), one obtains a second-order differential equation in terms of the surface electrostatic potential in Region (I): (See Appendix)

$$\alpha_1 \cdot \frac{d^2 \Psi_{s1}(y)}{dy^2} + \beta_1 \cdot \Psi_{s1}(y) = \gamma_1 \quad (3)$$

where

$$\alpha_1 = 1 + \frac{\epsilon_{ox} x}{\epsilon_s t_{ox}} - \frac{\left[1 + \frac{t_b}{t_{ox}} + \frac{\epsilon_{ox} t_{si}}{\epsilon_s t_{ox}} \right] x^2}{t_{si}^2 + 2t_{si} \frac{\epsilon_{si} t_b}{\epsilon_{ox}}}$$

$$\beta_1 = \frac{-2 \left[1 + \frac{t_b}{t_{ox}} + \frac{\epsilon_{ox} t_{si}}{\epsilon_s t_{ox}} \right]}{t_{si}^2 + 2t_{si} \frac{\epsilon_{si} t_b}{\epsilon_{ox}}}$$

Fig. 1. Cross section of the PD SOI dynamic-threshold MOS (DTMOS) device under study.

$$\gamma_1 = \frac{qN_A}{\epsilon_s} - \frac{2\Psi_{sub}}{t_{si}^2 + 2t_{si} \frac{\epsilon_{si} t_b}{\epsilon_{ox}}} - \frac{2\Psi_G \left[\frac{t_b}{t_{ox}} + \frac{\epsilon_{ox} t_{si}}{\epsilon_s t_{ox}} \right]}{t_{si}^2 + 2t_{si} \frac{\epsilon_{si} t_b}{\epsilon_{ox}}}.$$

Solving (3) with the boundary conditions that i) at the source/Region (I) interface, the surface electrostatic potential is $\Psi_{s1}(0) = \Phi_{bi}$, where $\Phi_{bi} = (kT/q) \ln(N_D/n_i)$, ii) at the Region (I)/Region (II) interface, the surface electrostatic potential is $\Psi_{s1}(l_1) = \Psi_{l1}$, where Ψ_{l1} is the surface electrostatic potential at $y = l_1$, one obtains the surface potential in Region (I) as shown in (4) at the bottom of the next page.

B. Region (II)— $l_1 < y < l_2$

In Region (II), 2-D Poisson's equation is

$$\frac{\partial^2 \Psi_2(x, y)}{\partial x^2} + \frac{\partial^2 \Psi_2(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_s}. \quad (5)$$

While deriving the threshold voltage model, among three regions, Region (II) is the most important. In order to increase the precision of the model and based on MEDICI 2-D simulation results, instead of the second-order approximation as shown in (2), a third-order expression has been adopted for approximating the electrostatic potential in Region (II):

$$\Psi_2(x, y) = a_{02}(y) + a_{12}(y)x + a_{22}(y)x^2 + a_{32}(y)x^3. \quad (6)$$

The four boundary conditions for solving (5) are i) at the top surface, the surface electrostatic potential is $\Psi_2(0, y) = \Psi_{s2}(y)$, ii) at the top surface, the vertical electric field is

$$\left. \frac{\partial \Psi_2(x, y)}{\partial x} \right|_{x=0} = \frac{\epsilon_{ox}}{\epsilon_s} \frac{\Psi_{s2}(y) - \Psi_G}{t_{ox}},$$

iii) at the Region (II)/neutral region interface, its electrostatic potential is $\Psi_2(w_d, y) = \Psi_B$, iv) at the Region (II)/neutral region interface, its vertical electric field is

$$\left. \frac{\partial \Psi_2(x, y)}{\partial x} \right|_{x=w_d} = 0$$

where w_d is the depth of the depletion region in Region (II) given by

$$w_d = \sqrt{\frac{2\epsilon_s(\Psi_{s2} + \phi_f - V_B)}{qN_A}}$$

Ψ_B is the body electrostatic potential $\phi_f = (kT/q)\ln(N_A/n_i)$ is the Fermi voltage of the p-type thin-film, and V_B is the body bias. Using the above boundary conditions and (5) and (6), one obtains a second-order differential equation in terms of the surface electrostatic potential in Region (II):

$$\alpha_2 \cdot \frac{d^2 \Psi_{s2}(y)}{dy^2} + \beta_2 \cdot \Psi_{s2}(y) = \gamma_2, \quad (7)$$

$$\alpha_2 = 1 - \frac{3x^2}{w_d^2} + \frac{2x^3}{w_d^3} + \frac{\epsilon_{ox}x}{\epsilon_s t_{ox}} - \frac{2\epsilon_{ox}x^2}{\epsilon_s t_{ox}w_d} + \frac{\epsilon_{ox}x^3}{\epsilon_s t_{ox}w_d^2}$$

$$\beta_2 = \frac{12x}{w_d^3} - \frac{6}{w_d^2} + \frac{6\epsilon_{ox}x}{\epsilon_s t_{ox}w_d^2} - \frac{4\epsilon_{ox}}{\epsilon_s t_{ox}w_d}$$

$$\gamma_2 = \frac{qN_A}{\epsilon_s} + \left[\frac{12x}{w_d^3} - \frac{6}{w_d^2} \right] \Psi_B + \left[\frac{6\epsilon_{ox}x}{\epsilon_s t_{ox}w_d^2} - \frac{4\epsilon_{ox}}{\epsilon_s t_{ox}w_d} \right] \Psi_G.$$

Solving (7) with two boundary conditions: i) at the Region (I)/Region (II) interface, its surface electrostatic potential is $\Psi_{s2}(l_1) = \Psi_{l1}$, ii) at

the Region (II)/Region (III) interface, its surface electrostatic potential is $\Psi_{s2}(l_2) = \Psi_{l2}$, where Ψ_{l2} is the surface electrostatic potential at $y = l_2$, one obtains (8), as shown at the bottom of the page.

C. Region (III)— $l_2 < y < L$

Similar to Region (I), Region (III) is the right fully-depleted region near the drain ($l_2 < y < L$) except that the boundary conditions are different—i) at the Region (II)/Region (III) interface, its surface potential is $\Psi_{s3}(l_2) = \Psi_{l2}$, ii) at the drain end, its potential is $\Psi_{s3}(L) = \Phi_{bi} + V_{DS}$. In Region (III), its surface electrostatic potential can be obtained using a similar method as for Region (I), as shown in (9) at the bottom of the next page, where $\alpha_3 = \alpha_1$, $\beta_3 = \beta_1$, and $\gamma_3 = \gamma_1$.

In order to have a consistency in the electrostatic potential in Regions (I)–(III), and since the electrostatic potential and the lateral electric field should be continuous at the Region (I)/(II) and (II)/(III) interfaces ($y = l_1, y = l_2$): $\Psi_{s1}(l_1) = \Psi_{s2}(l_1) = \Psi_{l1}$, $\Psi_{s2}(l_2) = \Psi_{s3}(l_2) = \Psi_{l2}$:

$$\left. \frac{d\Psi_{s1}(y)}{dy} \right|_{y=l_1} = \left. \frac{d\Psi_{s2}(y)}{dy} \right|_{y=l_1}$$

$$\left. \frac{d\Psi_{s2}(y)}{dy} \right|_{y=l_2} = \left. \frac{d\Psi_{s3}(y)}{dy} \right|_{y=l_2}.$$

From (4), (8), and (9), one obtains

$$\Psi_{l1} = \frac{(N_1 - J_1)(K_1 + I_2) - M_1 \cdot (J_2 + N_1)}{(I_1 - K_1)(K_1 + I_2) + M_1^2}, \quad (10)$$

$$\Psi_{l2} = \frac{(N_2 - J_2)(K_1 - I_1) + K_2 \cdot (J_1 - N_1)}{(I_1 - K_1)(K_1 + I_2) + M_1^2} \quad (11)$$

$$\Psi_{s1}(y) = A_1 \cdot \exp\left(\sqrt{\frac{-\beta_1}{\alpha_1}} y\right) + B_1 \cdot \exp\left(-\sqrt{\frac{-\beta_1}{\alpha_1}} y\right) + \frac{\gamma_1}{\beta_1}$$

$$A_1 = \frac{-\left(\Phi_{bi} - \frac{\gamma_1}{\beta_1}\right) + \left(\Psi_{l1} - \frac{\gamma_1}{\beta_1}\right) \exp\left(\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right)}{\exp\left(2\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right) - 1}$$

$$B_1 = \frac{\left(\Phi_{bi} - \frac{\gamma_1}{\beta_1}\right) \exp\left(2\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right) - \left(\Psi_{l1} - \frac{\gamma_1}{\beta_1}\right) \exp\left(\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right)}{\exp\left(2\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right) - 1} \quad (4)$$

$$\Psi_{s2}(y) = A_2 \cdot \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} y\right) + B_2 \cdot \exp\left(-\sqrt{\frac{-\beta_2}{\alpha_2}} y\right) + \frac{\gamma_2}{\beta_2}$$

$$A_2 = \frac{\left(\Psi_{l2} - \frac{\gamma_2}{\beta_2}\right) \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \left(\Psi_{l1} - \frac{\gamma_2}{\beta_2}\right) \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)}{\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)}$$

$$B_2 = \frac{-\left(\Psi_{l2} - \frac{\gamma_2}{\beta_2}\right) \exp\left[\sqrt{\frac{-\beta_2}{\alpha_2}} (l_2 + 2l_1)\right] + \left(\Psi_{l1} - \frac{\gamma_2}{\beta_2}\right) \exp\left[\sqrt{\frac{-\beta_2}{\alpha_2}} (2l_2 + l_1)\right]}{\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)} \quad (8)$$

where (see the equation at the bottom of the page). From (8), where the minimum surface electrostatic potential occurs at $y = S_2 = (1/2)\sqrt{(-\alpha_2/\beta_2)}\ln(B_2/A_2)$ with its value equal to

$$\begin{aligned}\Psi_{s2}(y = S_2) &= \Psi_{s2\min} \\ &= A_2 \cdot \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} S_2\right) \\ &\quad + B_2 \cdot \exp\left(-\sqrt{\frac{-\beta_2}{\alpha_2}} S_2\right) + \frac{\gamma_2}{\beta_2}\end{aligned}\quad (12)$$

$$\begin{aligned}A_2 &= C_2 + D_2 \cdot \gamma_2 \\ B_2 &= E_2 + F_2 \cdot \gamma_2 \\ C_2 &= \frac{\Psi_{l2} \cdot \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \Psi_{l1} \cdot \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)}{\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)}\end{aligned}$$

$$\begin{aligned}\Psi_{s3}(y) &= A_3 \cdot \exp\left(\sqrt{\frac{-\beta_3}{\alpha_3}} y\right) + B_3 \cdot \exp\left(-\sqrt{\frac{-\beta_3}{\alpha_3}} y\right) + \frac{\gamma_3}{\beta_3} \\ A_3 &= \frac{\left(\Phi_{bi} + V_{DS} - \frac{\gamma_3}{\beta_3}\right) \exp\left(\sqrt{\frac{-\beta_3}{\alpha_3}} L\right) - \left(\Psi_{l2} - \frac{\gamma_3}{\beta_3}\right) \exp\left(\sqrt{\frac{-\beta_3}{\alpha_3}} l_2\right)}{\exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} L\right) - \exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} l_2\right)} \\ B_3 &= \frac{-\left(\Phi_{bi} + V_{DS} - \frac{\gamma_3}{\beta_3}\right) \exp\left[\sqrt{\frac{-\beta_3}{\alpha_3}} (L + 2l_2)\right] + \left(\Psi_{l2} - \frac{\gamma_3}{\beta_3}\right) \exp\left[\sqrt{\frac{-\beta_3}{\alpha_3}} (2L + l_2)\right]}{\exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} L\right) - \exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} l_2\right)}\end{aligned}\quad (9)$$

$$\begin{aligned}I_1 &= \frac{\sqrt{\frac{-\beta_1}{\alpha_1}} \left[\exp\left(2\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right) + 1 \right]}{\exp\left(2\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right) - 1} \\ J_1 &= \frac{-\sqrt{\frac{-\beta_1}{\alpha_1}} \left[2 \left(\Phi_{bi} - \frac{\gamma_1}{\beta_1} \right) \exp\left(\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right) + \frac{\gamma_1}{\beta_1} \left(\exp\left(2\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right) + 1 \right) \right]}{\exp\left(2\sqrt{\frac{-\beta_1}{\alpha_1}} l_1\right) - 1} \\ K_1 &= \frac{-\sqrt{\frac{-\beta_2}{\alpha_2}} \left[\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) + \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right) \right]}{\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)} \\ M_1 &= \frac{2\sqrt{\frac{-\beta_2}{\alpha_2}} \exp\left[\sqrt{\frac{-\beta_2}{\alpha_2}} (l_1 + l_2)\right]}{\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)} \\ N_1 &= \frac{\frac{\gamma_2}{\beta_2} \sqrt{\frac{-\beta_2}{\alpha_2}} \left[\exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right) \right]^2}{\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)} \\ I_2 &= \frac{-\sqrt{\frac{-\beta_3}{\alpha_3}} \left[\exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} L\right) + \exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} l_2\right) \right]}{\exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} L\right) - \exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} l_2\right)} \\ J_2 &= \frac{\sqrt{\frac{-\beta_3}{\alpha_3}} \left[2 \left(\Phi_{bi} + V_{DS} - \frac{\gamma_3}{\beta_3} \right) \exp\left(\sqrt{\frac{-\beta_3}{\alpha_3}} (L + l_2)\right) + \frac{\gamma_3}{\beta_3} \left(\exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} L\right) + \exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} l_2\right) \right) \right]}{\exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} L\right) - \exp\left(2\sqrt{\frac{-\beta_3}{\alpha_3}} l_2\right)}\end{aligned}$$

TABLE I
KEY PARAMETERS OF THE n-CHANNEL PARTIALLY-DEPLETED (PD) SOI
DYNAMIC-THRESHOLD MOS (DTMOS) DEVICE [3] UNDER STUDY

channel length (L)	0.2 μm
channel width (W)	1.0 μm
gate oxide thickness (t_{ox})	64 $\text{\AA}$
buried oxide thickness (t_b)	4000 $\text{\AA}$
thin-film thickness (t_{si})	1500 $\text{\AA}$
thin-film doping density (N_A)	$3.0 \times 10^{17} \text{cm}^{-3}$
source/drain doping density (N_D)	$5.0 \times 10^{19} \text{cm}^{-3}$
flat-band voltage (V_{FB})	0.56V
temperature in Kelvin (T)	300K

$$D_2 = \frac{-\frac{1}{\beta_2} \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) + \frac{1}{\beta_2} \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)}{\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)}$$

$$E_2 = \frac{-\Psi_{l2} \cdot \exp\left[\sqrt{\frac{-\beta_2}{\alpha_2}} (l_2 + 2l_1)\right] + \Psi_{l1} \cdot \exp\left[\sqrt{\frac{-\beta_2}{\alpha_2}} (2l_2 + l_1)\right]}{\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)}$$

$$F_2 = \frac{\frac{1}{\beta_2} \exp\left[\sqrt{\frac{-\beta_2}{\alpha_2}} (l_2 + 2l_1)\right] - \frac{1}{\beta_2} \exp\left[\sqrt{\frac{-\beta_2}{\alpha_2}} (2l_2 + l_1)\right]}{\exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_2\right) - \exp\left(2\sqrt{\frac{-\beta_2}{\alpha_2}} l_1\right)}$$

Threshold voltage of the PD SOI DTMOS device is defined as the gate voltage when its minimum surface electrostatic potential is equal to the thin-film Fermi voltage ϕ_f . Therefore, from (12), threshold voltage is

$$V_{th} = -V_{fb} + \left(\frac{G_2}{H_2} - \frac{qN_A}{\epsilon_s}\right) \frac{-\epsilon_s t_{ox} w_d}{\epsilon_{ox}} \quad (13)$$

where

$$G_2 = \phi_f - C_2 \cdot \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} S_2\right) - E_2 \cdot \exp\left(-\sqrt{\frac{-\beta_2}{\alpha_2}} S_2\right)$$

and

$$H_2 = \frac{1}{\beta_2} + D_2 \cdot \exp\left(\sqrt{\frac{-\beta_2}{\alpha_2}} S_2\right) + F_2 \cdot \exp\left(-\sqrt{\frac{-\beta_2}{\alpha_2}} S_2\right)$$

in which, in order to consider the influence of the lateral and the vertical electric fields, α_2 and β_2 are approximated as the value at $x = w_d/2$. As shown in (13), the threshold voltage of the PD SOI DTMOS device is a function of its gate voltage—dynamic threshold.

III. MODEL VERIFICATION

In order to verify the validity of the compact threshold-voltage model for short-channel PD SOI DTMOS device, the analytical model results have been compared with the experimental data [3] and MEDICI 2-D simulation results. The key parameters of the n-channel PD SOI DTMOS devices under study are given in Table I.

Based on the analytical model, experimental data and MEDICI 2-D simulation results, Fig. 2 shows the threshold voltage vs. body voltage of the n-channel PD SOI DTMOS device for different channel lengths. As shown in the figure, when V_{BS} increases, its threshold voltage decreases. In contrast, for non-DTMOS devices, the threshold voltage is independent of the body voltage. Due to short-channel effects, when

Fig. 2. Threshold voltage versus body voltage of the n-channel partially-depleted (PD) SOI dynamic-threshold MOS (DTMOS) device based on the analytical model and the 2-D simulation results.

Fig. 3. Threshold voltage versus channel length of the n-channel partially-depleted (PD) SOI dynamic-threshold MOS (DTMOS) device based on the analytical model and the 2-D simulation results.

channel length is scaled down, the threshold voltage of the DTMOS device becomes smaller. When the body voltage becomes larger, its short-channel effects become less noticeable. As shown in the figure, the analytical model results correlate well with the experimental data [3] and MEDICI 2-D simulation results.

Fig. 3 shows the threshold voltage versus channel length of the n-channel PD SOI DTMOS device. As shown in the figure, with a more heavily doped thin-film and a thinner gate oxide, its short-channel effects are less noticeable. Also shown in the figure, at a larger V_{DS} , the short-channel effects due to drain-induced-barrier lowering (DIBL) are more noticeable. Furthermore, at a high V_{BS} , its short-channel effects are smaller, which is identical to the results as shown in Fig. 2. Compared to the case without the DTMOS configuration ($V_{BS} = 0$ V), the DTMOS one ($V_{BS} = 0.6$ V) shows less DIBL-induced short-channel effects. As shown in the figure, as verified by the MEDICI 2-D simulation results, the analytical model predicts well of the DIBL-induced short-channel effects.

Fig. 4. Location in the lateral channel with the minimum surface electrostatic potential versus drain voltage of the n-channel partially-depleted (PD) SOI DTMOS device based on the analytical model.

IV. DISCUSSION

The threshold-voltage model [(13)] for short-channel DTMOS devices is derived from the quasi-2-D approach as described before. Considering a long channel case ($L \rightarrow \infty$), from (10)–(12): $C_2 = D_2 = E_2 = F_2 = 0$. Therefore, $G_2 \simeq \phi_f$, $H_2 \simeq 1/\beta_2$, where $\beta_2 = -\epsilon_{ox}/\epsilon_s t_{ox} w_d$. From (13), the threshold voltage formula is simplified to

$$V_{th} = -V_{fb} + \left(\frac{G_2}{H_2} - \frac{qN_A}{\epsilon_s} \right) \frac{-\epsilon_s t_{ox} w_d}{\epsilon_{ox}} = -V_{fb} + \phi_f + \frac{qN_A w_d}{C_{ox}} \quad (14)$$

which is the conventional 1D threshold voltage formula.

The threshold voltage formula [(13)] also includes the drain-induced-barrier-lowering (DIBL) effects. As described in the last section, compared to the device without the DTMOS structure ($V_{BS} = 0$ V), the DTMOS device ($V_{BS} \neq 0$ V) has less DIBL-induced short-channel effects, which can be reasoned as follows. Owing to the body-tied-to-gate structure, the gate control capability over the channel region is enhanced as compared to the case without the DTMOS configuration. As a result, the drain induced electric field over the lateral channel region has been offset by the increased surface potential caused by V_{BS} —the DTMOS configuration. Consequently, for the DTMOS cases, when V_{BS} is increased, DIBL is noticeably reduced. Based on the analytical model, Fig. 4 shows the location in the lateral channel with the minimum surface electrostatic potential versus drain voltage of the n-channel PD SOI DTMOS device. As shown in the figure, at a higher V_{DS} , the location with the minimum surface electrostatic potential moves closer to the source end. Compared to the case without the DTMOS configuration ($V_{BS} = 0$ V), with the DTMOS configuration ($V_{BS} > 0$ V) the location with the minimum electrostatic potential moves away from the source end—less DIBL, which confirms the results in Fig. 3.

V. CONCLUSION

In this paper, a closed-form threshold-voltage model for short-channel partially-depleted (PD) SOI dynamic-threshold MOS (DTMOS) devices based on a quasi-2-D approach has been presented. As verified by experimental data and 2-D simulation results, this compact model provides an accurate prediction of the threshold-voltage behavior of the short-channel PD SOI DTMOS devices. Based on the analytical model, as verified by the 2-D simulation results, PD

SOI DTMOS devices have less short-channel effects including DIBL-induced short-channel effects.

APPENDIX DERIVATION OF (3)

In the Appendix, derivation of (3) is described.

From (2), with the first boundary condition i) $\Psi_1(0, y) = \Psi_{s1}(y)$, one obtains

$$a_{01}(y) = \Psi_{s1}(y). \quad (A1)$$

From the derivative of (2):

$$\frac{\partial \Psi_1(x, y)}{\partial x} = a_{11}(y) + 2a_{21}(y)x \quad (A2)$$

with the second boundary condition

$$\text{ii) } \left. \frac{\partial \Psi_1(x, y)}{\partial x} \right|_{x=0} = \frac{\epsilon_{ox}}{\epsilon_s} \frac{\Psi_{s1}(y) - \Psi_G}{t_{ox}}$$

one obtains

$$a_{11}(y) = \frac{\epsilon_{ox}}{\epsilon_s} \frac{\Psi_{s1}(y) - \Psi_G}{t_{ox}}. \quad (A3)$$

From (2), at $x = t_{si}$, one obtains

$$\Psi_1(t_{si}, y) = a_{01}(y) + a_{11}(y)t_{si} + a_{21}(y)t_{si}^2. \quad (A4)$$

From (A4) with the third boundary condition

$$\text{iii) } \left. \frac{\partial \Psi_1(x, y)}{\partial x} \right|_{x=t_{si}} = \frac{\epsilon_{ox}}{\epsilon_s} \frac{\Psi_{sub} - \Psi_1(t_{si}, y)}{t_b}$$

the third boundary condition becomes

$$\left. \frac{\partial \Psi_1(x, y)}{\partial x} \right|_{x=t_{si}} = \frac{\epsilon_{ox}}{\epsilon_s t_b} [\Psi_{sub} - a_{01}(y) - a_{11}(y)t_{si} - a_{21}(y)t_{si}^2]. \quad (A5)$$

From (A1)–(A3), and (A5), one obtains

$$a_{21}(y) = -\frac{1 + \frac{t_b}{t_{ox}} + \frac{\epsilon_{ox} t_{si}}{\epsilon_s t_{ox}}}{t_{si}^2 + 2 \frac{\epsilon_s t_b}{\epsilon_{ox}} t_{si}} \Psi_{s1}(y) + \frac{\Psi_{sub} + \left(\frac{t_b}{t_{ox}} + \frac{\epsilon_{ox} t_{si}}{\epsilon_s t_{ox}} \right) \Psi_G}{t_{si}^2 + 2 \frac{\epsilon_s t_b}{\epsilon_{ox}} t_{si}}. \quad (A6)$$

Using (A1), (A3), and (A6) in (2), and then taking second-order derivatives of (2) with respect to x and y , one obtains

$$\frac{\partial^2 \Psi_1(x, y)}{\partial x^2} = 2 \left[-\frac{1 + \frac{t_b}{t_{ox}} + \frac{\epsilon_{ox} t_{si}}{\epsilon_s t_{ox}}}{t_{si}^2 + 2 \frac{\epsilon_s t_b}{\epsilon_{ox}} t_{si}} \Psi_{s1}(y) + \frac{\Psi_{sub} + \left(\frac{t_b}{t_{ox}} + \frac{\epsilon_{ox} t_{si}}{\epsilon_s t_{ox}} \right) \Psi_G}{t_{si}^2 + 2 \frac{\epsilon_s t_b}{\epsilon_{ox}} t_{si}} \right] \quad (A7)$$

$$\frac{\partial^2 \Psi_1(x, y)}{\partial y^2} = \left[1 + \frac{\epsilon_{ox} x}{\epsilon_s t_{ox}} - \frac{\left(1 + \frac{t_b}{t_{ox}} + \frac{\epsilon_{ox} t_{si}}{\epsilon_s t_{ox}} \right) x^2}{t_{si}^2 + 2 \frac{\epsilon_s t_b}{\epsilon_{ox}} t_{si}} \right] \frac{d^2 \Psi_{s1}(y)}{dy^2}. \quad (A8)$$

From (A7), (A8), and (1), one obtains (3).

REFERENCES

- [1] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, "A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation," in *IEDM Tech. Dig.*, 1994, pp. 809–812.
- [2] F. Assaderaghi and S. Parke, "A dynamic threshold voltage MOSFET (DTMOS) for very low voltage operation," *IEEE Electron Device Lett.*, vol. 15, pp. 510–512, Dec. 1994.
- [3] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage VLSI," *IEEE Trans. Electron Devices*, vol. 44, pp. 414–422, Mar. 1997.
- [4] I. Y. Chung, Y. J. Park, and H. S. Min, "A new SOI inverter using dynamic threshold for low-power applications," *IEEE Electron Device Lett.*, vol. 18, pp. 248–250, June 1997.
- [5] W. Jin and C. H. Chan, "On the power dissipation in dynamic threshold SOI CMOS inverter," *IEEE Trans. Electron Devices*, vol. 45, pp. 1717–1724, Aug. 1998.
- [6] T. W. Houston, "A novel dynamic threshold voltage circuit configuration," in *IEEE SOI Conf. Dig.*, Oct. 1997, pp. 154–155.
- [7] K. K. Young, "Short-channel effect in fully depleted SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 36, pp. 399–402, Feb. 1989.

MOSFET Subthreshold Compact Modeling With Effective Gate Overdrive

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Abstract—In this brief, previously-proposed one-region MOSFET drain current (I_{ds}) model is improved in the subthreshold modeling. The compact model is derived based on first-principle drift–diffusion formulation with the correct drift and diffusion currents in strong inversion and subthreshold, respectively. The new model has only one fitting parameter for subthreshold slope and can ensure excellent continuity with smooth transition from subthreshold to strong-inversion regimes, including the moderate-inversion region of growing importance for low-voltage and low-power circuits.

Index Terms—Drift–diffusion, effective gate overdrive, MOSFET, subthreshold.

I. INTRODUCTION

The current trend of ULSI technology is toward low-power and low-voltage applications, where accurate transistor modeling near the threshold condition is becoming more and more important. This is the regime in which a MOSFET changes its region of operations from strong to weak inversion and from linear to saturation when the gate voltage (V_{gs}) reduces at a fixed drain voltage (V_{ds}). The fundamental physics of MOSFETs is based on charge inversion by the vertical field (V_{gs}) in the channel and carrier transport by the parallel field (V_{ds}) along the channel. The difficulty in modeling near threshold voltage (V_t) lies in the presence of both inversion and depletion charges as well as both drift and diffusion currents.

As witnessed by the industry-standard Berkeley Short-channel Integrated-gate FET Model (BSIM) [1]–[3], conventional piecewise models have evolved to continuous single-region models that have

smooth transition characteristics in the moderate-inversion regime. Use of smoothing functions [3] for the effective saturation voltage (V_{deff}) to join linear and saturation currents and the introduction of the offset voltage (V_{off}) [4] in the effective gate overdrive (V_{geff}) to join drift and diffusion currents have resulted in unified I_{ds} expressions for all regions that have continuous partial derivatives, which is essential for circuit simulation.

In this paper, we present enhanced formulations of a one-region I_{ds} model for deep-submicron MOSFETs, with emphasis on subthreshold modeling. The model covers full range of gate lengths down to the V_t roll-off regime at low and high drain biases with one set of fitting parameters extracted with one iteration. Only one fitting parameter (V_{off}) is used to characterize the subthreshold current, in which length- and bias-dependent subthreshold slope has been physically modeled. Our previously formulated I_{ds} model [5] has been improved in the subthreshold regime with continuous inversion and depletion charges, effective mobility and effective field, series resistance, and effective gate overdrive. Currently, our model does not include narrow-width effect.

II. MODEL FORMULATION

A major contribution to single-region MOSFET current modeling is attributed to the introduction of the effective gate overdrive [4]

$$V_{geff} = \frac{2nv_{th} \ln \left(1 + e^{(V_{gs}-V_t)/(2nv_{th})} \right)}{1 + 2n(C_{ox}/C_d)e^{-(V_{gs}-V_t-2V_{off})/(2nv_{th})}} \quad (1)$$

in which an offset voltage V_{off} to characterize the leakage current at zero gate bias is used as a fitting parameter. The smoothing function (1) makes it possible that the unified inversion charge

$$Q_{inv} = C_{ox} V_{geff} \quad (2a)$$

approach the correct asymptotes in strong inversion

$$Q_{inv} = C_{ox}(V_{gs} - V_t) \quad (2b)$$

when $V_{gs} > V_t$, and in the subthreshold regime

$$Q_{inv} = C_d v_{th} e^{(V_{gs}-V_t-V_{off})/(nv_{th})} \quad (2c)$$

when $V_{gs} - V_t < 2V_{off}$ [6], [7] thus, the factor 1 in the denominator of (1) can be ignored and $\ln(1 + e^x)$ in the numerator approaches e^x . In (1) and (2c), $v_{th} = kT/q$ is the thermal voltage. $C_{ox} = \epsilon_{ox}/t_{ox}$ is the gate oxide capacitance per unit area.

$$n = 1 + C_d/C_{ox} \quad (2d)$$

is the subthreshold slope factor. And

$$C_d = \frac{\gamma C_{ox}}{2\sqrt{0.75\phi_s - V_{bs}}} \quad (2e)$$

is the depletion capacitance, which is modified for the factor $0.75\phi_s$ based on the assumption that at subthreshold, the surface potential ($\phi_s = 2\phi_F - \Delta\phi_s$, [5]) is the average of weak (ϕ_F) and strong ($2\phi_F$) inversion condition [7]. The length-dependent subthreshold slope, given by (2d) and (2e), is implicitly embedded in the barrier-lowering term, $\Delta\phi_s$ [5].

For $V_t + V_{off} < V_{gs} < V_t$ (V_{off} is normally negative), the MOSFET is in moderate inversion, which is modeled by the smoothing function (1). The parameter V_{off} must be extracted from the measured terminal $I_{ds} - V_{gs}$ data, in which a finite V_{ds} must be applied. However, both

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