A Novel Low-Voltage Content-Addressable-Memory (CAM) Cell with a Fast Tag-Compare Capability Using Partially Depleted (PD) SOI CMOS Dynamic-Threshold (DTMOS) Techniques

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Abstract—This paper reports a novel low-voltage content-addressable-memory (CAM) cell with a fast tag-compare capability using partially depleted (PD) SOI CMOS dynamic-threshold (DTMOS) techniques. With two auxiliary pass transistors to dynamically control the bodies of transistors in the tag-compare portion of CAM cell, this SOI CAM cell has a fast tag-compare capability at a low supply voltage of 0.7 V as verified by the results from the two-dimensional semiconductor device simulation program MEDICI.

Index Terms—CMOS, content-addressable memory (CAM), dynamic threshold (DTMOS), low voltage, partially depleted (PD) silicon-on-insulator (SOI), tag cell, VLSI.

I. INTRODUCTION

CONTENT-addressable memory (CAM) has been broadly used in many VLSI system applications such as imaging processing, network communication, and parallel data processing to facilitate operations of fast comparison and validation of patterns [1]. As shown in Fig. 1, a conventional 10T CAM cell [2] is composed of two portions: the SRAM portion (transistors M1-M6) and the tag-compare portion (transistors M7-M10) for performing the XOR operation of the data stored in the SRAM cell with the input data at the digit lines. If a logic-1 is stored at the internal storage node n1, which is different from the logic state of the data on the digit line (DL), then the match line (ML) is pulled down to ground, indicating a miss. Along with the increased complexity of the related VLSI systems, the tag-compare operation of a related large-size CAM circuit has become a bottleneck for high-speed applications. This is especially serious for operations using a low supply voltage. Recently, CMOS dynamic threshold (DTMOS) techniques have been reported for their advantages in low-voltage SOI CMOS VLSI circuits [3]–[5]. In this paper, a low-voltage CAM cell structure with a fast tag-compare capability using partially depleted (PD) SOI CMOS DTMOS techniques is described. In the following sections, the new SOI CAM circuit and its operation are described first, followed by performance evaluation and conclusion.

Fig. 1. Conventional content-addressable-memory (CAM) cell.

II. LOW-VOLTAGE SOI CAM CELL

Fig. 2 shows the new low-voltage CAM cell with a fast tag-compare capability using PD SOI DTMOS techniques. As shown in the figure, there are twelve transistors in the new CAM cell. In addition to the ten transistors for the SRAM cell and the tag-compare portion as in the conventional CAM cell (Fig. 1), two auxiliary transistors M11 and M12, which are controlled by the internal storage nodes of the SRAM cell, for controlling the bodies of transistors M7-M10 have been added to the tag-compare portion. Digit lines DL and DLB are connected to the drain of transistors M12 and M11. In addition, digit lines DL and DLB also control the turn-on of transistors M8 and M10. Using this arrangement, either transistor M11 or M12 turns on depending on the data stored in the SRAM cell. If the internal storage node n1 in the memory cell is high, both transistors M7 and M11 turn on and both transistors M9 and M12 are off. Prior to the tag-compare operation, both digit lines DL and DLB are low and the match line ML is precharged to high. Since transistor M11 is on, the bodies of transistors M7 and M8 are tied to low via transistor M11. During the tag-compare operation, if logic-0 exists on the digit line DL (a logic 1 exists on the complementary digit line DLB), transistor M8 turns on. Due to the logic 1 status on

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Fig. 2. New low-voltage CAM cell with a fast tag-compare capability using PD SOI DTMOS techniques.

the complementary digit line DLB, the threshold voltages of both transistors M7 and M8 are lowered since the bodies of transistors M7 and M8 are high. As a result, the conductance of transistors M7 and M8 will be increased, and the match line ML will be discharged (indicating a miss) faster than in the conventional case. When the tag-compare procedure is over, the complementary digit line DLB is restored back low. Therefore, transistor M7 remains on and M8 turns off with their threshold voltages restored to their zero-biased values since their bodies are tied to zero by transistor M11. This implies that the leakage current in transistor M8 stays low as in the case with the DTMOS techniques.

Consider the other case with the condition that the digit line DL is high and the complementary digit line DLB is low. During the tag-compare operation, the threshold voltages of both transistors M7 and M8 maintain their zero-biased values since their bodies are tied to low via transistor M11, which is turned on by the logic-1 state of the internal storage node n1. Therefore, the leakage current of transistor M8, which is turned off by the logic-0 state of the complementary digit line DLB, is identical to the case without the DTMOS techniques. On the other side, transistor M10 is on since the digit line DL is high. In addition, both transistors M9 and M12 are off since the internal storage node n2 is low. Therefore, the threshold voltages of both transistors M9 and M10 are not decreased since their bodies are disconnected from the digit line DL. This implies that the leakage current in transistor M9 stays low. Consequently, the match line ML maintains its precharged high state owing to small leakage currents in both nonconducting paths of transistors M7/M8 and M9/M10.

III. PERFORMANCE AND DISCUSSION

In order to investigate the effectiveness of this low-voltage CAM cell structure using PD SOI DTMOS techniques, transient

Fig. 3. (a) Cross section of the PD SOI nMOS device and its layout used in the new CAM cell. (b) Layout of the new CAM cell with a fast tag-compare capability using PD SOI DTMOS techniques.

performance during the tag-compare operation at V_{DD} of 0.7 V has been studied. In the transient analysis typical PD SOI MOS devices with their cross section and layout as shown in Fig. 3(a) have been used. The PD SOI nMOS device used in the CAM cell has a channel length of $0.2 \mu\text{m}$, a channel width of $0.2 \mu\text{m}$, a front gate oxide of $50 \text{ \AA}$, an n+ polysilicon gate, a p-type thin film of $2000 \text{ \AA}$ doped with a density of $2 \times 10^{17} \text{ cm}^{-3}$, a buried oxide

Fig. 4. The match line (ML), the digit line (DLB), and the body voltage waveforms during the tag-compare transient of the new low-voltage SOI CAM cell using DTMO techniques and the conventional CAM cell under the “miss” condition at V_{DD} of 0.7 V based on MEDICI results.

of 5000 Å on the top of p-type substrate doped with a density of 10^{15} cm^{-3} . Considering the effect of the body contact region, a parasitic capacitance of 1 fF and a parasitic resistance of 10 kΩ have been placed at the body contact of each device.

Fig. 3(b) shows the layout of the new CAM cell with a fast-tag compare capability using PD SOI DTMO techniques. As shown in the figure, compared to the conventional CAM cell, in addition to the body contacts for the transistors in the tag-compare portion, transistors M11 and M12 have been added. The layout area of the new CAM cell is $5.97 \mu\text{m} \times 6.57 \mu\text{m}$, which is 22% larger compared to the conventional CAM cell. Accounting for the drain-body capacitances of many transistors in a large CAM circuit connected to the match line, the parasitic capacitance of the next stage, and the wiring capacitance, a parasitic capacitance of 0.25 pF is placed at the match line (ML). At the internal storage node n1 of the SRAM cell, a logic-1 value is assumed. Initially, the ML is precharged to high at 0.7 V prior to the tag-compare operation. Fig. 4 shows the ML, the complementary digit line (DLB), and the body voltage waveforms during the tag-compare transient of the new low-voltage SOI CAM cell using DTMO techniques and the conventional CAM cell under the “miss” condition at V_{DD} of 0.7 V based on a two-dimensional device simulation (MEDICI [6]) results. As shown in the figure, after the tag-compare operation is initiated at 10 ns, the complementary digit line DLB is changed from logic-0 to logic-1 and the digital line DL still remains at logic-0. After the DLB switches to high at 0.7 V, the bodies of both transistors M7 and M8 are raised to above 0.4 V by transistor M11. As a result, the ML is pulled down to 0 V quickly. Note that the bodies of both transistors M7 and M8 cannot reach 0.7 V due to the body effect. As shown in the figure, the pull-down time of the tag-compare operation for the miss access using the new CAM cell is 6.8 ns, which is 45% faster as compared to the conventional CAM cell.

In order to show the feasibility of the new CAM cell for use in a system, transient performance of the new CAM cell used in a translation lookaside buffer (TLB) [7] has been done. Fig. 5

shows the brief critical path during the read access of TLB [7] using the new CAM cell with PD SOI DTMO techniques. As shown in the figure, the ML is ANDed with a clock signal CLK2 to generate the word line for driving the corresponding SRAM cell—CLK2 serves to detect the miss/hit signal. If the ML maintains high, it indicates a hit. Under this situation, when CLK2 turns high, the SRAM word line SWL turns high, which triggers the readout of the data from the corresponding SRAM cell. The signals on the bit lines of the corresponding SRAM cell are amplified by a latch-type sense amplifier before connecting to an output buffer. If the ML turns low from high, it indicates a miss. Under this condition, when CLK2 turns high, the SWL maintains low. Thus, no data will be read out from the corresponding SRAM cell. The speed performance of the tag access is important in determining how early CLK2 can switch high without accidental readout of the data from the corresponding SRAM cell during the miss access. If the result of the tag-compare procedure is a miss, then the SWL is supposed to stay low regardless of turn-high of CLK2. If CLK2 turns high too early before the fall of the ML, the SWL may accidentally rise to high to trigger readout of the corresponding SRAM cell data unexpectedly. Therefore, CLK2 should not turn high too early. However, the timing to turn high is important since the time for CLK2 to turn high without accidental turn-high of the SRAM word line SWL determines the speed performance of the read access of the overall circuit. So, the turn-high time of CLK2 is important. CLK2 should be turned from low to high as early as possible on the condition that it will not trigger the wrong readout procedure for the corresponding SRAM cell.

Transient analysis of the brief critical path during the miss access of the TLB using the new CAM cell has been carried out using an SOI SPICE [8]. Considering the effect of the body contact region, a parasitic capacitance of 1 fF and a parasitic resistance of 10 kΩ have been placed at the body contact of each device. Considering the more complicated circuit involved, a parasitic capacitance of 0.2 pF has been placed at both the digit line and the complementary digit line DL/DLB for the case with the new CAM cell. In contrast, for the case using the conventional CAM cell, a parasitic capacitance of 0.1 pF is placed at the digital line and the complementary digit line DL/DLB. Fig. 6 shows the transient waveforms associated with the critical path during the miss access of the TLB based on the new CAM cell using PD SOI DTMO techniques based on the SOI SPICE simulation results. Also shown in the figure are the results for the case using the conventional CAM cell. During the transient, data in DI is fixed at high (node n1 is high). Initially, the ML is precharged to high. During the tag-compare procedure, if a high to low signal is placed at the complementary data in DIB, then the DLB switches from low to high. Due to a larger parasitic capacitance of 0.2 pF at the DLB, as indicated by the solid line, the new CAM cell case shows a slower rise in the DLB. On the other hand, owing to the stronger driving capability of the tag-compare portion, the new CAM cell case shows a faster pulldown in the ML. Therefore, the turn-high of CLK2 can be earlier without causing an erroneous rise in the SWL as indicated in solid lines. Thus a higher speed of the miss access has been obtained. In contrast, without using the new CAM cell, an erroneous rise in the SWL has occurred for the same CLK2 as

Fig. 5. Brief critical path during the read access of the translation lookaside buffer (TLB) using the new CAM cell with PD SOI DTMOS techniques.

Fig. 6. Transient waveforms associated with the critical path during the miss access of the TLB based on the new CAM cell using PD SOI DTMOS techniques based on the SOI-SPICE simulation results.

indicated in the figure. Note that during the hit access, since the ML stays high, there is no difference in the hit access time between the two cases with and without using the new CAM cell. As for the write access into the CAM cell, despite the slightly increased parasitic capacitances at the internal nodes n1/n2, the write access time of the new CAM cell case is about identical

to that of the conventional case based on the SOI SPICE simulation results we have observed.

IV. CONCLUSION

In this paper, a novel low-voltage CAM cell with a fast tag-compare capability using PD SOI CMOS DTMOS techniques has been reported. Using two auxiliary pass transistors to dynamically control the bodies of transistors in the tag-compare portion of CAM cell, this SOI CAM cell has a fast tag-compare capability at a low supply voltage of 0.7 V as verified by the MEDICI results.

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