A Closed-Form Back-Gate-Bias Related Inverse Narrow-Channel Effect Model for Deep-Submicron VLSI CMOS Devices Using Shallow Trench Isolation

Shih-Chia Lin, James B. Kuo, *Fellow, IEEE*, Kuo-Tai Huang, and Shih-Wei Sun

Abstract—This paper reports an analytical inverse narrow-channel effect threshold voltage model for shallow-trench-isolated (STI) CMOS devices using a conformal mapping technique to simplify the two-dimensional (2-D) analysis. As verified by the experimentally measured data and the 2-D simulation results, the analytical model predicts well the inverse narrow-channel effect threshold voltage behavior of the STI CMOS devices. Based on the study, the inverse narrow-channel effect also affects the saturation-region output conductance of a small-geometry STI CMOS device in addition to the short-channel effect.

Index Terms—Conformal mapping technique, inverse narrow-channel effect, small geometry, STI.

I. INTRODUCTION

IN ORDER to increase the device density of a VLSI circuit, deep-submicron bulk CMOS devices using shallow trench isolation technology have been developed [1]–[3]. Different from using LOCOS technology, deep-submicron CMOS devices using shallow trench technology have a unique “inverse narrow-channel effect”—when the channel width of the devices is scaled down, their threshold voltage is shrunk instead of increased as for the LOCOS devices. As a part of the inverse narrow-channel effect, due to the field crowding at the sidewall oxide trench, device behaviors and models including anomalous subthreshold conduction behavior have also been reported [4]–[6]. Recently, advanced shallow trench isolation structures to lessen the inverse narrow-channel effect by decreasing corner crowding effect have been reported [7], [8]. An inverse narrow-channel effect threshold voltage model for trench-isolated MOS devices has been reported [9]. However, the solution is not closed-form. A closed-form current hump model for the STI-related subthreshold current conduction has also been reported [10]. In this paper, a closed-form analytical inverse narrow-channel effect threshold voltage model for STI CMOS devices without using any fitting parameter is derived. It will be shown that by using a conformal mapping technique to simplify the two-dimensional (2-D) analysis, the closed-form

analytical model predicts well the inverse narrow-channel effect threshold voltage behavior of the STI CMOS devices. In the following sections, the analytical model is derived first, followed by model evaluation and discussion.

II. MODEL DERIVATION

Fig. 1 shows the SEM cross section of the 0.25 μm STI CMOS device structure with the step-down structure in the sidewall oxide trench under study [7]. An N^+ polysilicon gate above a thin oxide of 50 Å has been used. Fig. 2 shows the cross section of a bulk STI NMOS device with an N^+ polysilicon gate [7] under study. As shown in Fig. 2, the sidewall oxide trench has the step-down structure from the active device region. As shown in Fig. 1, the step-down height is $H = -0.015 \mu\text{m}$. The depth of the sidewall oxide trench structure with the step-down structure is 0.25 μm . The width of the sidewall oxide trench structure is 0.5 μm .

Fig. 3 shows the 2-D electric field contours in the STI NMOS devices with the no-step ($H = 0$ —solid lines) and the step-down ($H = -0.015 \mu\text{m}$ —dashed lines) structures in the sidewall oxide trench and with a channel width of 0.3 μm biased at the threshold voltage and back gate voltages of a) 0 V and b) -5 V based on the 2-D simulation results [10]. As shown in the figures, between the two cases, with a step-down structure in the sidewall oxide trench, the spread in the electric field distributions near the oxide trench is more. In addition, with a negative back gate bias, the corner field crowding effect increases. As a result, the spread in the electric field distributions near the sidewall oxide trench between two cases increases. Therefore, the corner field crowding effect, which is dependent on the back gate bias and the sidewall oxide trench structure, is important in determining the inverse narrow-channel effect related threshold voltage. In the following derivation, the conventional approach to regard the electrostatic potential at the corner equal to that at the center of the channel [5] is not used. Instead, by using a conformal mapping method and Gauss law, the corner electrostatic potential (Ψ_{STI}) is derived. It will be shown that by using this corner electrostatic potential model, a more accurate threshold voltage model can be obtained.

A. Threshold Voltage

Consider the STI NMOS devices with their cross sections as shown in Fig. 2. The center of the channel at the gate oxide/silicon interface (point G) is defined as the origin. The x axis is in

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S. C. Lin and J. B. Kuo are with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 106-17 R.O.C.

K. T. Huang and S. W. Sun are with the United Microelectronics Corporation, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C.

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Fig. 1. SEM cross section of the bulk STI CMOS device structure with the step-down structure in the sidewall oxide trench under study.

Fig. 2. Cross section of the bulk STI NMOS device with a step-down structure in the sidewall oxide trench under study.

the substrate direction and the y axis is in the lateral direction. The 2-D Poisson's equation is

$$\frac{\partial^2 \Psi(x, y)}{\partial x^2} + \frac{\partial^2 \Psi(x, y)}{\partial y^2} = \frac{-qN_{\text{sub}}}{\epsilon_s} \quad (1)$$

where

- Ψ electrostatic potential;
- ϵ_s permittivity of silicon;
- q electronic charge;
- N_{sub} effective doping density of the substrate.

Note that the substrate doping distribution may be nonuniform. In order to simplify the derivation, the effective doping density N_{sub} has been used. If the substrate is p-type, $N_{\text{sub}} = -N_A$, where N_A is the doping density of the p-type substrate. If the substrate is n-type, $N_{\text{sub}} = N_D$, where N_D is the doping density of the n-type substrate. Based on the potential distribution obtained from 2-D simulation, the electrostatic potential inside the device can be approximated by the following polynomial [11]:

$$\Psi(x, y) = a_0(y) + a_1(y)x + a_2(y)x^2 + a_3(y)x^3. \quad (2)$$

The above electrostatic potential equation is subject to the following four boundary conditions. First, at the top oxide interface

Fig. 3. Two-dimensional electric field contours inside the STI NMOS devices with the no-step and the step-down structures in the sidewall oxide trench biased at the back gate voltages of (a) 0 V and (b) -5 V based on the 2-D simulation results.

($x = 0$) and second, at the depletion edge ($x = w_d$) the electrostatic potentials are

$$\Psi(0, y) = \Psi_s(y) \quad (3)$$

$$\Psi(w_d, y) = \Psi_B \quad (4)$$

respectively. $\Psi_s(y)$ is the electrostatic potential at the substrate surface, and $w_d = \sqrt{(2\epsilon_s[\phi_f - \Psi_B])/(q|N_{\text{sub}}|)}$ is the width of the depletion region in the substrate. Note that in this device, the depletion width is smaller than the depth of the trench oxide ($w_d < t_t$). Ψ_B is the electrostatic potential of the substrate [$\Psi_B = V_B - \phi_f$, V_B is the back gate bias, $\phi_f = (kT/q) \ln(N_A/n_i)$ for the p-type substrate, $\phi_f = (kT/q) \ln(n_i/N_D)$ for the n-type substrate, k is the Boltzmann constant, T is the temperature in Kelvin, and n_i is the intrinsic carrier density]. The third boundary condition is at the top oxide interface ($x = 0$), the derivative of the electrostatic potential can be obtained by Gauss law and considering the voltage drop in the oxide

$$\left. \frac{d\Psi}{dx} \right|_{x=0} = -\frac{\epsilon_{\text{ox}}}{\epsilon_s} \frac{\Psi_G - \Psi_s(y)}{t_{\text{ox}}} \quad (5)$$

where

$\Psi_G = V_G + V_{fb}$	gate electrostatic potential;
V_G	front gate bias;
V_{fb}	flat-band voltage;
t_{ox}	thickness of the front oxide;
ϵ_{ox}	oxide permittivity.

The fourth boundary condition is at the depletion edge, the derivative of the electrostatic potential is zero, as follows:

$$\left. \frac{d\Psi}{dx} \right|_{x=w_d} = 0. \quad (6)$$

From (2)–(6), coefficients $a_0(y)$, $a_1(y)$, $a_2(y)$, and $a_3(y)$ can be expressed as a function of the surface electrostatic potential ($\Psi_s(y)$), as follows:

$$a_0(y) = \Psi_s(y) \quad (7)$$

$$a_1(y) = \frac{\epsilon_{ox}}{\epsilon_s} \frac{\Psi_s(y) - \Psi_G}{t_{ox}} \quad (8)$$

$$a_2(y) = -3\Psi_s(y)w_d^{-2} + 3w_d^{-2}\Psi_B - 2w_d^{-1} \frac{\epsilon_{ox}\Psi_s(y)}{\epsilon_s t_{ox}} + 2w_d^{-1} \frac{\epsilon_{ox}\Psi_G}{\epsilon_s t_{ox}} \quad (9)$$

$$a_3(y) = -2w_d^{-3}\Psi_B + 2w_d^{-3}\Psi_s(y) + w_d^{-2} \frac{\epsilon_{ox}\Psi_s(y)}{\epsilon_s t_{ox}} - w_d^{-2} \frac{\epsilon_{ox}\Psi_G}{\epsilon_s t_{ox}}. \quad (10)$$

From (1), (2), (7)–(10), and [12], since the depletion region is much smaller than the width ($w_d \ll W$), the change of $\partial^2\Psi/\partial y^2$ in the y direction is much more than that in the x direction. Therefore, $\partial^2\Psi/\partial y^2$ is mainly a function of the lateral direction (y -axis), and one obtains a differential equation in terms of surface electrostatic potential ($\Psi_s(y)$):

$$\begin{aligned} & \left[(1 - 3r^2 + 2r^3) + \frac{\epsilon_{ox}w_d}{\epsilon_s t_{ox}} r(1 - r)^2 \right] \frac{d^2\Psi_s(y)}{dy^2} \\ & + \left[(12r - 6)w_d^{-2} + (6r - 4)w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}} \right] \Psi_s(y) \\ & = \frac{-qN_{sub}}{\epsilon_s} + (12r - 6)w_d^{-2}\Psi_B - (4 - 6r) \frac{\epsilon_{ox}\Psi_G}{\epsilon_s t_{ox}} w_d^{-1} \end{aligned} \quad (11)$$

where $x = rw_d$ has been used ($r = 0.5$). The electrostatic potential at the sidewall corner ($y = \pm(W/2)$ —point C) is defined as $\Psi_{STI} = \Psi_s(y = \pm W/2)$. Solving (11) with the electrostatic potential at the sidewall corner (Ψ_{STI}) as the boundary condition, one obtains the surface electrostatic potential as in (12) below. The threshold voltage of the device is defined as the gate voltage when the surface electrostatic potential at the center of the channel ($\Psi_s(y = 0)$) reaches ϕ_f . Therefore, from (12), shown at the bottom of the page, the threshold voltage is

$$\begin{aligned} V_{th} &= C_1 + C_2\Psi_{STI} - V_{fb}, \\ C_1 &= \frac{(12r - 6)w_d^{-2} + (6r - 4)w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}}}{(6r - 4)w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}}} \\ &\quad \cdot \phi_f \left(1 - \frac{1}{\cosh\left(\alpha \frac{W}{2}\right)} \right)^{-1} \\ &\quad - \frac{\frac{qN_{sub}}{\epsilon_s} + (12r - 6)w_d^{-2}\Psi_B}{(6r - 4)w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}}}, \\ C_2 &= - \left[(12r - 6)w_d^{-2} + (6r - 4)w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}} \right] \\ &\quad \cdot \left(1 - \frac{1}{\cosh\left(\alpha \frac{W}{2}\right)} \right)^{-1} \frac{1}{\cosh\left(\alpha \frac{W}{2}\right)} \\ &\quad \cdot \frac{1}{(6r - 4)w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}}}. \end{aligned} \quad (13)$$

The above threshold voltage formula is a function of the electrostatic potential at the sidewall corner (Ψ_{STI}). Once the electrostatic potential at the sidewall corner is known, the threshold voltage is obtained.

B. Corner Electrostatic Potential (Ψ_{STI})

The electrostatic potential at the sidewall corner can be obtained by considering the fringing electric field effect from the

$$\begin{aligned} \Psi_s(y) &= \frac{\cosh(\alpha y)}{\cosh\left(\alpha \frac{W}{2}\right)} \left[\Psi_{STI} - \frac{-\frac{qN_{sub}}{\epsilon_s} + (12r - 6)w_d^{-2}\Psi_B + (6r - 4)w_d^{-1} \frac{\epsilon_{ox}\Psi_G}{\epsilon_s t_{ox}}}{(12r - 6)w_d^{-2} + (6r - 4)w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}}} \right] \\ &\quad + \frac{-\frac{qN_{sub}}{\epsilon_s} + (12r - 6)w_d^{-2}\Psi_B + (6r - 4)w_d^{-1} \frac{\epsilon_{ox}\Psi_G}{\epsilon_s t_{ox}}}{(12r - 6)w_d^{-2} + (6r - 4)w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}}}, \\ \alpha &= \sqrt{\frac{(12r - 6)w_d^{-2} + (6r - 4)w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}}}{(1 - 3r^2 + 2r^3) + \frac{\epsilon_{ox}w_d}{\epsilon_s t_{ox}} r(1 - r)^2}} \end{aligned} \quad (12)$$

corner of the sidewall oxide trench. Applying Gauss law in a Gauss box defined by $CEFG$ as shown in Fig. 2, one obtains:

$$\Phi_{GC} + \Phi_{CE} + \Phi_{EF} + \Phi_{FG} = -qN_{\text{sub}}w_d \frac{W}{2} + Q_s \quad (14)$$

where

- Q_s interface charge at the sidewall ($Q_s = qq_s w_d$);
- q_s interface charge density at the sidewall;
- Φ_{GC} surface flux along the silicon surface between points G and C , which is related to the surface electrostatic potential ($\Psi_s(y)$);
- Φ_{CE} sidewall flux along the trench oxide sidewall between points C and E , which is influenced by the fringing electric field at the corner of the sidewall oxide trench;
- Φ_{EF} flux in the substrate region between points E and F — $\Phi_{EF} = 0$; and
- Φ_{FG} flux in the substrate direction between points F and G .

Considering symmetry of the device, $\Phi_{FG} = 0$.

1) *Flux Φ_{GC}* : Flux Φ_{GC} can be obtained by integrating the vertical electric field at the top oxide interface in the oxide from the center of the channel (point G) to the sidewall corner (point C)

$$\Phi_{GC} = \epsilon_{\text{ox}} \int_0^{W/2} \frac{\Psi_G - \Psi_s(y)}{t_{\text{ox}}} dy. \quad (15)$$

At the threshold voltage, from (12), (13), and (15), Φ_{GC} becomes (16), shown at the bottom of the page.

2) *Flux Φ_{CE}* : Considering the step-down sidewall oxide trench structure as shown in Fig. 2, the analysis of flux Φ_{CE} is as follows. Flux Φ_{CE} at the sidewall between point C and point E can be expressed as

$$\Phi_{CE} = \epsilon_{\text{ox}} \int_C^E \vec{E} \cdot d\vec{l}. \quad (17)$$

Along the sidewall, from (2), (7)–(10), the electrostatic potential is:

$$\begin{aligned} \Psi\left(x, \frac{W}{2}\right) &= \begin{cases} \Psi_{\text{STI}} + D_1 x + D_2 x^2 + D_3 x^3, & \text{for } 0 \leq x \leq w_d, \\ \Psi_B, & \text{for } w_d \leq x \leq t_t \end{cases} \\ D_1 &= \frac{\epsilon_{\text{ox}}}{\epsilon_s} \frac{\Psi_{\text{STI}} - \Psi_G}{t_{\text{ox}}}, \\ D_2 &= -3\Psi_{\text{STI}}w_d^{-2} + 3w_d^{-2}\Psi_B - 2w_d^{-1} \frac{\epsilon_{\text{ox}}\Psi_{\text{STI}}}{\epsilon_s t_{\text{ox}}} \\ &\quad + 2w_d^{-1} \frac{\epsilon_{\text{ox}}\Psi_G}{\epsilon_s t_{\text{ox}}}, \\ D_3 &= -2w_d^{-3}\Psi_B + 2w_d^{-3}\Psi_{\text{STI}} + w_d^{-2} \\ &\quad \cdot \frac{\epsilon_{\text{ox}}\Psi_{\text{STI}}}{\epsilon_s t_{\text{ox}}} - w_d^{-2} \frac{\epsilon_{\text{ox}}\Psi_G}{\epsilon_s t_{\text{ox}}}. \end{aligned} \quad (18)$$

As shown in Fig. 2, Φ_{CE} is composed of Φ_{CO} and Φ_{OE} . Between points C and O , the flux Φ_{CO} can be expressed by considering the voltage difference between the gate electrode (Ψ_G) and the electrostatic potential at the oxide trench ($\Psi(x, \frac{W}{2})$)

$$\Phi_{CO} = \epsilon_{\text{ox}} \int_0^H \frac{\Psi_G - \Psi\left(x, \frac{W}{2}\right)}{t_{\text{ox}}} dx. \quad (19)$$

From (18), the above equation becomes

$$\begin{aligned} \Phi_{CO} &= \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} (P_1 + P_2 \Psi_{\text{STI}}), \\ P_1 &= C_1 H + \frac{\epsilon_{\text{ox}} C_1}{\epsilon_s t_{\text{ox}}} \frac{H^2}{2} - \left(2w_d^{-1} \frac{\epsilon_{\text{ox}}}{\epsilon_s t_{\text{ox}}} C_1 + 3w_d^{-2} \Psi_B \right) \\ &\quad \cdot \frac{H^3}{3} + \left(w_d^{-2} \frac{\epsilon_{\text{ox}}}{\epsilon_s t_{\text{ox}}} C_1 + 2w_d^{-3} \Psi_B \right) \frac{H^4}{4}, \\ P_2 &= -(1 - C_2)H - (1 - C_2) \frac{\epsilon_{\text{ox}}}{\epsilon_s t_{\text{ox}}} \frac{H^2}{2} \\ &\quad + \left(3w_d^{-2} + 2w_d^{-1} \frac{\epsilon_{\text{ox}}}{\epsilon_s t_{\text{ox}}} (1 - C_2) \right) \frac{H^3}{3} \\ &\quad - \left(2w_d^{-3} + w_d^{-2} \frac{\epsilon_{\text{ox}}}{\epsilon_s t_{\text{ox}}} (1 - C_2) \right) \frac{H^4}{4}. \end{aligned} \quad (20)$$

$$\begin{aligned} \Phi_{GC} &= -\frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} (N_1 + N_2 \Psi_{\text{STI}}), \\ N_1 &= \frac{\left[-\frac{qN_{\text{sub}}}{\epsilon_s} + (12r - 6)w_d^{-2}\Psi_B + (6r - 4)w_d^{-1} \frac{\epsilon_{\text{ox}} C_1}{\epsilon_s t_{\text{ox}}} \right] \left[\frac{W}{2} - \frac{\tanh\left(\alpha \frac{W}{2}\right)}{\alpha} \right]}{(12r - 6)w_d^{-2} + (6r - 4)w_d^{-1} \frac{\epsilon_{\text{ox}}}{\epsilon_s t_{\text{ox}}}} - C_1 \frac{W}{2}, \\ N_2 &= \frac{(6r - 4)w_d^{-1} \frac{\epsilon_{\text{ox}} C_2}{\epsilon_s t_{\text{ox}}} \left(\frac{W}{2} - \frac{\tanh\left(\alpha \frac{W}{2}\right)}{\alpha} \right)}{(12r - 6)w_d^{-2} + (6r - 4)w_d^{-1} \frac{\epsilon_{\text{ox}}}{\epsilon_s t_{\text{ox}}}} + \frac{\tanh\left(\alpha \frac{W}{2}\right)}{\alpha} - C_2 \frac{W}{2} \end{aligned} \quad (16)$$

From points O to E , the flux Φ_{OE} can be expressed by the following line integral:

$$\Phi_{OE} = \epsilon_{ox} \int_O^E \vec{E} \cdot d\vec{l}. \quad (21)$$

Due to the fringing electric field from the top gate via the trench oxide to the sidewall edge, (21) is difficult to calculate. In order to simplify the analysis, a conformal mapping transformation technique [13] has been used to transform the original $x\vec{X} + y\vec{Y}$ space in terms of the $\vec{X}$ and $\vec{Y}$ axes as shown in Fig. 2 to the $u\vec{U} + v\vec{V}$ space in terms of $\vec{U}$ and $\vec{V}$ axes as shown in Fig. 4 based on the following transfer function:

$$\begin{aligned} \left(y - \frac{W}{2}\right) \vec{Y} + n(x - H) \vec{X} &= t_{ox} \sin(u\vec{U} + v\vec{V}), \\ n &= \frac{t_{ox}}{t_t - H} \sinh \left[\cosh^{-1} \left(\frac{W_t}{2t_{ox}} \right) \right]. \end{aligned} \quad (22)$$

Using the above transformation, ABODE in the $x\vec{X} + y\vec{Y}$ coordinates is changed to $A'B'O'D'E'$ in the $u\vec{U} + v\vec{V}$ coordinates. In the $u\vec{U} + v\vec{V}$ coordinates, the distance between points A' and B' is $d = \sinh^{-1}(n(t_t - H)/t_{ox})$, the distance between points O' and D' is $d_0 = \sinh^{-1}(n(w_d - H)/t_{ox})$, and the distance between point B' and point O' is $m\pi/2$, where m must satisfy $\sin(m\pi/2) = 1$. From the 2-D simulation results, $m = 5$. From (22), $y = W/2$ is transformed into $u = 0$. Therefore, one obtains: $x = H + (t_{ox}/n) \sinh v$. Under this situation, (18) is rewritten as (23), shown at the bottom of the next page. Using the conformal mapping transformation as shown in (22), (21) becomes

$$\Phi_{OE} = \epsilon_{ox} \int_{O'}^{E'} \frac{\Psi_G - \Psi(0, v)}{\frac{m\pi}{2}} dv. \quad (24)$$

From (23) and (24), the flux Φ_{OE} becomes

$$\begin{aligned} \Phi_{OE} &= \frac{2\epsilon_{ox}}{m\pi} (S_1 + S_2 \Psi_{STI}), \\ S_2 &= -d_0 + C_2 d + (1 - C_2) \frac{\epsilon_{ox}}{\epsilon_s t_{ox}} F_1 \\ &\quad - \left(3w_d^{-2} + 2w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}} (1 - C_2) \right) F_2 \\ &\quad + \left(2w_d^{-3} + w_d^{-2} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}} (1 - C_2) \right) F_3, \\ S_1 &= d(C_1 - 1) + d_0 - \frac{\epsilon_{ox}}{\epsilon_s t_{ox}} F_1 C_1 \\ &\quad + \left(2w_d^{-1} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}} C_1 + 3w_d^{-2} \Psi_B \right) F_2 \\ &\quad - \left(w_d^{-2} \frac{\epsilon_{ox}}{\epsilon_s t_{ox}} C_1 + 2w_d^{-3} \Psi_B \right) F_3, \\ F_1 &= -d_0 H - \frac{t_{ox}}{n} (\cosh d_0 - 1), \\ F_2 &= -d_0 \left(H^2 - \frac{1}{2} \left(\frac{t_{ox}}{n} \right)^2 \right) \\ &\quad - 2H \frac{t_{ox}}{n} (\cosh d_0 - 1) \end{aligned}$$

Fig. 4. Boundary of the step-down sidewall oxide trench structure of the STI MOS device before and after conformal mapping for model derivation.

$$\begin{aligned} & - \frac{1}{4} \left(\frac{t_{ox}}{n} \right)^2 \sinh(2d_0), \\ F_3 &= -d_0 \left(H^3 - \frac{3}{2} H \left(\frac{t_{ox}}{n} \right)^3 \right) \\ & - \left(3H^2 \frac{t_{ox}}{n} - \frac{3}{4} \left(\frac{t_{ox}}{n} \right)^3 \right) (\cosh d_0 - 1) \\ & - \frac{3}{4} H \left(\frac{t_{ox}}{n} \right)^3 \sinh(2d_0) \\ & - \frac{1}{12} \left(\frac{t_{ox}}{n} \right)^3 (\cosh(3d_0) - 1). \end{aligned} \quad (25)$$

From (20) and (25), the flux Φ_{CE} is

$$\Phi_{CE} = \left(\frac{\epsilon_{ox}}{t_{ox}} P_1 + \frac{2\epsilon_{ox}}{m\pi} S_1 \right) + \left(\frac{\epsilon_{ox}}{t_{ox}} P_2 + \frac{2\epsilon_{ox}}{m\pi} S_2 \right) \Psi_{STI}. \quad (26)$$

From (14), (16), and (26), one obtains

$$\Psi_{STI} = \frac{\frac{W}{2} q(-N_{sub})w_d + Q_s - \frac{\epsilon_{ox}}{t_{ox}} (P_1 - N_1) - \frac{2\epsilon_{ox}}{m\pi} S_1}{\frac{\epsilon_{ox}}{t_{ox}} (P_2 - N_2) + \frac{2\epsilon_{ox}}{m\pi} S_2}. \quad (27)$$

From (13) and (27), the threshold voltage model is

$$\begin{aligned} V_{th} &= C_1 + C_2 \\ &\quad + \frac{\frac{W}{2} q(-N_{sub})w_d + Q_s - \frac{\epsilon_{ox}}{t_{ox}} (P_1 - N_1) - \frac{2\epsilon_{ox}}{m\pi} S_1}{\frac{\epsilon_{ox}}{t_{ox}} (P_2 - N_2) + \frac{2\epsilon_{ox}}{m\pi} S_2} \\ &\quad - V_{fb}. \end{aligned} \quad (28)$$

Equation (28) is the closed-form analytical threshold voltage model for the inverse narrow-channel effect of an STI NMOS device with a step-down structure in the sidewall oxide trench.

III. MODEL EVALUATION

In order to evaluate the effectiveness of the analytical inverse narrow-channel effect model for the STI CMOS device, the analytical model results have been compared with the 2-D simulation results and experimentally measured data. The test device under study has a gate oxide of 50 Å below an N⁺ polysilicon gate. The width of the trench oxide is 0.5 μm. The depth

Fig. 5. Surface electrostatic potential distribution in the lateral width direction at the oxide interface in the STI NMOS device with a channel width of $0.3 \mu\text{m}$ and with the no-step ($H = 0$) and the step-down ($H = -0.015 \mu\text{m}$) structures in the sidewall oxide trench, biased at the back gate voltages of 0 and -5 V , based on the analytical models and the 2-D simulation results.

of the sidewall oxide trench is $0.25 \mu\text{m}$. The step height of the step-down structure is $0.015 \mu\text{m}$.

Fig. 5 shows the surface electrostatic potential distribution in the lateral width direction at the oxide interface in the STI NMOS device with a channel width of $0.3 \mu\text{m}$ and with the no-step ($H = 0$) and the step-down ($H = -0.015 \mu\text{m}$) structures in the sidewall oxide trench, biased at the back gate voltages of 0 and -5 V , based on the analytical models and the 2-D simulation results. Compared to the case with the no-step structure, the device with the step-down structure ($H = -0.015 \mu\text{m}$) in the sidewall oxide trench, has a more noticeable corner fringing electric field. With a nonzero back gate bias, the corner fringing field effect increases.

Fig. 6 shows the threshold voltage versus the channel width of the STI, NMOS and PMOS devices with the step-down structure in the sidewall oxide trench biased at various V_B 's based on the experimentally measured data (solid circles), the 2-D simulation (dashed lines) and the analytical model results (solid lines). As

Fig. 6. Threshold voltage versus channel width of the STI: (a) NMOS and (b) PMOS devices with the step-down structure in the sidewall oxide trench biased at various V_B 's based on the experimentally measured data, the 2-D simulation, and the analytical model results.

verified by the experimentally measured data and the 2-D simulation results, considering the corner fringing electric effect, the analytical model can predict the inverse narrow-channel effect. Fig. 7 shows the threshold voltage versus the back gate bias of STI NMOS and PMOS devices with: a) no-step and b)

$$\Psi(0, v) = \begin{cases} E_0 + E_1 \sinh v + E_2 \cosh(2v) + E_3 \sinh(3v) & \text{for } 0 \leq v \leq d_0, \\ \Psi_B & \text{for } d_0 \leq v \leq d \end{cases}$$

$$E_0 = \Psi_{\text{STI}} + D_1 H + \left(H^2 - \frac{1}{2} \left(\frac{t_{\text{ox}}}{n} \right)^2 \right) D_2 + \left(H^3 - \frac{3}{2} H \left(\frac{t_{\text{ox}}}{n} \right)^3 \right) D_3,$$

$$E_1 = \frac{t_{\text{ox}}}{n} D_1 + 2H \frac{t_{\text{ox}}}{n} D_2 + \left(3H^2 \frac{t_{\text{ox}}}{n} - \frac{3}{4} \left(\frac{t_{\text{ox}}}{n} \right)^3 \right) D_3,$$

$$E_2 = \frac{1}{2} \left(\left(\frac{t_{\text{ox}}}{n} \right)^2 D_2 + 3H \left(\frac{t_{\text{ox}}}{n} \right)^2 D_3 \right),$$

$$E_3 = \frac{1}{4} \left(\frac{t_{\text{ox}}}{n} \right)^3 D_3$$
(23)

Fig. 7. Threshold voltage versus back gate bias of the STI NMOS and PMOS devices with: (a) no-step and (b) step-down structures in the sidewall oxide trench based on the experimentally measured data, the 2-D simulation and the analytical model results.

step-down structures in the sidewall oxide trench based on the experimentally measured data, the 2-D simulation and the analytical model results. As shown in the figures, for the no-step structure, at $V_B = 0$ V, when the channel width shrinks from 1 to $0.3 \mu\text{m}$, the threshold voltage of the NMOS device decreases by 0.004 V. At $V_B = -5$ V, it shrinks 0.0595 V. Therefore, with a nonzero back gate bias, the inverse narrow-channel effect is more noticeable. For the step-down structure, at $V_B = 0$ V, when the channel width shrinks from 1 to $0.3 \mu\text{m}$, the threshold voltage of the NMOS device decreases by 0.0067 V. At $V_B = -5$ V, it shrinks 0.106 V. As for the PMOS devices, a similar trend on the influence of the body effect in the inverse narrow-channel effect can be seen. Consequently, the influence of the body effect in the inverse narrow-channel effect is more serious in the STI CMOS device with the step-down structure.

IV. DISCUSSION

When a deep-submicron CMOS device using shallow-trench isolation is scaled down, small-geometry three-dimensional (3-D) effects on the device behavior become more important.

Fig. 8. Three-dimensional electrostatic potential distributions in the STI NMOS device with the step-down structure in the sidewall oxide trench with channel lengths/widths of $0.25 \mu\text{m}/0.25 \mu\text{m}$ and $2 \mu\text{m}/1 \mu\text{m}$.

Fig. 9. Normalized drain current versus drain voltage of STI NMOS devices with the step-down structure in the sidewall oxide trench with various channel lengths and widths, based on experimental data.

Fig. 8 shows the 3-D electrostatic potential distributions in the STI NMOS device with the step-down structure in the sidewall oxide trench with channel lengths/widths of $0.25 \mu\text{m}/0.25 \mu\text{m}$ and $2 \mu\text{m}/1 \mu\text{m}$. As shown in the figure, when the channel length and width are large ($>1 \mu\text{m}$), the influence of the source and the sidewall is limited to the edge portion. When the channel length and width are small ($0.25 \mu\text{m}$), the influence of the source and the sidewall is noticeably increased. As a result, the 3-D effect is important. With a short channel, the influence of the inverse narrow channel effect can be more serious. Fig. 9 shows the normalized drain current versus drain voltage of STI NMOS devices with the step-down structure in the sidewall oxide trench with various channel lengths and widths based on the experimentally measured data. As shown in the figure, with a large channel length, due to the inverse narrow-channel effect, when the channel width is shrunk, the normalized drain current increases 15.1% . In contrast, with a short channel length, due to the inverse narrow-channel effect, it increases 36.7% . Comparing the normalized drain

currents between the large-dimension ($W/L = 10\ \mu\text{m}/10\ \mu\text{m}$) and the small-dimension ($W/L = 0.3\ \mu\text{m}/0.3\ \mu\text{m}$) cases, the decrease in the threshold voltage due to short-channel and narrow-channel effects does not increase the normalized drain current. Instead, it decreases it due to the 3-D geometry effects on interfering the movement of the electrons via the electric fields in the channel length and the channel width directions. From the figure, the inverse narrow-channel effect also complicates the short-channel effects of small-geometry STI CMOS devices in terms of the output conductance in the saturation region. This implies that the electron temperature effect in a deep-submicron small-geometry STI CMOS device is also determined by the inverse STI-related narrow-channel effects in addition to the short-channel effects. (Note that in other references such as [15], the output conductance of a deep-submicron CMOS device can be characterized by the electron temperature, which is solely dependent on the channel length.)

V. CONCLUSION

In this paper, an analytical inverse narrow-channel effect threshold voltage model for deep-submicron STI VLSI CMOS devices using a conformal mapping technique to simplify the 2-D analysis has been presented. As verified by the experimentally measured data and the 2-D simulation results, the analytical model predicts well the inverse narrow-channel effect threshold voltage behavior of the STI CMOS devices. Based on the study, the inverse narrow-channel effect also affects the saturation-region output conductance of a small-geometry STI CMOS device in addition to the short-channel effect.

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Shih-Chia Lin was born in Taichung, Taiwan, R.O.C., on November 27, 1970. He received the B.S.E.E. degree from National Taiwan University (NTU), Taipei, in 1992. Currently, he is pursuing the Ph.D. degree in the Department of Electrical Engineering, NTU.

His research interest is modeling VLSI SOI CMOS devices.

James B. Kuo (F'00) received the B.S.E.E. degree from National Taiwan University (NTU), Taipei, Taiwan, R.O.C., in 1977, the M.S.E.E. degree from The Ohio State University in 1978, and the Ph.D.E.E. degree from Stanford University, Stanford, CA, in 1985.

Before the Ph.D.E.E. program, he worked in Penril Data Communications, and Racal Vadic (1978–1981) as a Research Engineer working on integrating telecommunication modem chips using CMOS technology. After the Ph.D. program

(1985–1987), he worked as an Engineering Research Associate in the IC Laboratory, Stanford University, working on BiCMOS devices. Since 1987, he has been with NTU, where he is currently a Professor. His research expertise is in the field of low-voltage CMOS VLSI circuits and SPICE compact modeling of deep-submicron bulk and SOI CMOS and BiCMOS VLSI devices. He is an IEEE Fellow for contributions to modeling of CMOS VLSI devices. He has published more than 100 international journal papers and authored eight books including *Low-Voltage CMOS VLSI Circuits* (New York: Wiley, 1999) and *CMOS VLSI Engineering: Silicon-On-Insulator (SOI)* (Boston, MA: Kluwer, 1998). He has graduated over 35 M.S. and Ph.D. students specialized in CMOS circuit designs and device modeling, currently working in leading US and Taiwan's microelectronics companies.

Dr. serves as an Associate Editor for the IEEE CIRCUITS AND DEVICES MAGAZINE and chair of the membership committee for the IEEE Electron Devices Society. He is a distinguished lecturer of the IEEE Electron Devices Society.

Kuo-Tai Huang was born in Hsinchu, Taiwan, R.O.C., in 1964. In 1987, he received the B.S. degree in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan. He received the Ph.D. degree in materials science and engineering from the University of Utah, Salt Lake City, in 1995.

In March 1996, he joined the Advanced Technology Department, United Microelectronics Corporation, Hsinchu, where he has been engaged in the development of shallow trench isolation (STI) technology. Subsequently, he concentrated on DRAM capacitor modules. Currently, his research work is on high K dielectrics, TA205 and BST, for DRAM capacitor. He has contributed to five publications and holds more than 90 patents.

Shih-Wei Sun received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1979, and the Ph.D. degree from Northwestern University, Evanston, IL, in 1985.

He joined the Advanced Products Research and Development Laboratory, Motorola, Austin, TX, in 1985. He was involved in various aspects of CMOS and BiCMOS technology development, process transfer, and product introduction. In 1995, he joined United Microelectronics Corp. (UMC), Hsinchu, Taiwan, where he managed UMC's Advanced

Technology Development Group and was responsible for UMC's overall 0.25-micron technology development. He was transferred to UMC's Fab-6A in 1999, and is currently Fab-6A's Operation Director.