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A 1.5-V CMOS All-N-Logic True-Single-Phase Bootstrapped Dynamic-Logic Circuit Suitable for Low Supply Voltage and High-Speed Pipelined System Operation

J. H. Lou and J. B. Kuo

Abstract—This paper presents a 1.5-V CMOS true-single-phase (TSP) bootstrapped dynamic-logic (BDL) circuit using all-N-logic and bootstrapped circuit techniques for high-speed operation at a low supply voltage. As confirmed by the experimental results from the test chip implemented using a 0.8- μm CMOS technology, the speed performance of this CMOS all-N-logic TSP BDL circuit with four serial inputs is 75% faster at a supply voltage of 1.5 V, as compared to the conventional TSP dynamic-logic circuit. Using an all-N-logic TSP BDL circuit, the maximum operating frequency of an implemented digital quadrature modulator is 482 MHz at 5 V, and 68 MHz at 1.5 V, which is 27% faster compared to the circuit without using the BDL circuit.

I. INTRODUCTION

For next-generation CMOS VLSI circuits, low supply voltage is the trend. Since the threshold voltages of the CMOS devices cannot be scaled down accordingly with the supply voltage, designing a CMOS dynamic circuit using a low supply voltage for the next-generation CMOS VLSI is a challenge. CMOS dynamic-logic circuit techniques [1]–[4] have been used to enhance the speed performance of VLSI pipelined systems. However, CMOS dynamic-logic circuits may have disadvantages in race and charge-sharing problems. In addition, clocks with complicated timing may be required. In NORA [2], true-single-phase (TSP) [3] and Zipper-CMOS [4] dynamic-logic circuits, the pMOS logic blocks may limit the speed performance. In Zipper-CMOS dynamic-logic circuits, dc power consumption is required. A single-phase CMOS dynamic circuit using all-N-logic has been reported [5]. However, it is not suitable for low-voltage operation. In this paper, using the bootstrapper circuit technique [6], a CMOS all-N-logic TSP dynamic-logic circuit suitable for operation with a low supply voltage is described. In the following sections, the operation principles of the new 1.5-V CMOS all-N-logic TSP bootstrapped dynamic-logic (BDL) circuit is presented first, followed by performance evaluation and discussion.

II. 1.5 V-CMOS ALL-N-LOGIC TSP BDL CIRCUIT

Fig. 1 shows the 1.5-V CMOS all-N-logic TSP BDL circuits, the N1- and N2-blocks using the all-N-logic TSP technique. The N1-block is identical to the N-block TSP dynamic-logic circuit [3], except that a bootstrapper circuit containing the bootstrap capacitor C_b has been added. In the N1-block, when CK is low, MNN is off, and the V_{dn} node is separated from the ground. Under this situation, the V_{dn} node is precharged to V_{dd} , since MNP is on. Therefore, the internal node V_I is low, hence MLP1 is on and V_b is charged to high. At

this time, in the bootstrap capacitor C_b , an amount of charge $C_b V_{dd}$ is stored. Since both MBP1 and MCN1 are off, the output of the N1-block keeps its previous state. When CK is high, MNP is off and MNN is on. Therefore, when there exists a conduction path in the N1-block, the internal-node voltage V_{dn} is pulled low, thus V_I switches from low to high and MLP1 is off and MBP1 is on. Due to the charge stored in the bootstrap capacitor, V_b is bootstrapped to exceed V_{dd} . Since MBP1 is on, therefore, the output voltage of the N1-block will be pulled up to a value V_{out1} , which may exceed V_{dd} . Owing to the N1–N2–N1–N2 block arrangement, the bootstrapped output of the N1-block may help drive the following N2-block. Note that the N2-block is used to replace the p-block TSP dynamic-logic circuit [3]. When CK is high, MPP is off, therefore the N-logic is separated from V_{dd} . At the same time, the V_{dp} node is predischarged to ground, since MPN is on. Under this situation, the output of the N2-block V_{out2} keeps its previous state since both MCP2 and MLN2 are off. When CK is low, MPP turns on and MPN is off—the logic evaluation period. If there exists a conduction path in the N2-block, V_{dp} is pulled high to $V_{dd} - V_{tn}(V_{dp})$, where $V_{tn}(V_{dp})$ is the threshold voltage of the nMOS device when its source voltage is V_{dp} , due to the body effect of the nMOS device. Therefore, MLN2 turns on, hence the output voltage V_{out2} is pulled low. The switching speed of V_{out2} and the stability of the V_{dp} level can be improved by raising the V_{dp} level by MFN and MFP. When MLN2 turns on, MFN also turns on, which pulls the node voltage V_{N1} to ground. Thus, MFP turns on and V_{dp} is pulled high to V_{dd} .

The N1–N2–N1–N2 block arrangement is required for the CMOS all-N-logic TSP dynamic-logic circuit. When the N1-blocks are in the precharge period, the N2-blocks are in the logic-evaluation period. With the bootstrapper circuit in the N1-block, the output of the N1-block may exceed V_{dd} . Therefore, the internal voltage V_{dp} of the following N2-block can be raised to $V_{out1} - V_{tn}(V_{dp})$. As a result, the output voltage can be discharged faster by an enhanced current drive of the MLN2. In the N1-block, the extent of V_b surpassing V_{dd} —the internal voltage overshoot is dependent on C_b and the equivalent load capacitance at the output node. In this design, considering a fan-out of two, the equivalent load capacitance is 25 fF at the output node. Using a C_b implemented by a pMOS device of dimension 20 $\mu\text{m}/8 \mu\text{m}$, with its source and drain tied together, during the bootstrap operation V_b surpasses 1.5 V by 0.5 V. A higher internal voltage overshoot may bring in a greater improvement in speed performance. In the CMOS bootstrapper circuit, the body of MLP1 and MBP1 is connected to V_b instead of V_{dd} . Therefore, the internal voltage overshoot at V_b does not cause the forward bias of the source-drain-substrate junction.

III. PERFORMANCE AND DISCUSSION

In order to evaluate the performance of the 1.5-V CMOS all-N-logic TSP BDL circuit, a three-input NAND circuit, which is composed of an N1-block and an N2-block, has been designed. It is worth pointing out that the N1-block is noninverting and the N2-block is inverting. At the output of the N1-block, it is $A \cdot B$. At the output of the N2-block, it is $\overline{A \cdot B \cdot C}$. Fig. 2 shows the transient waveforms at the outputs of the three-input NAND circuit. As shown in the figure, when CK is high, the output of the N1-block (V_{o1}) is bootstrapped to exceed 1.5 V. Therefore, the internal node voltage

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Fig. 1. The 1.5-V CMOS all-N-logic TSP BDL circuits—N1-block and N2-block.

Fig. 2. Transient waveforms at the outputs of the N1-block and the N2-block of a three-input NAND circuit using cascading 1.5-V CMOS all-N-logic TSP BDL circuits (N1–N2).

V_{dp} of the N2-block can be pulled up to a higher level, thus the output of the N2-block can be pulled down at a faster speed.

In order to show the effectiveness of the all-N-logic TSP BDL circuit, a 1.5-V digital quadrature modulator [7] has been integrated using a 0.8- μm CMOS technology. Fig. 3 shows the measured transient waveforms of the digital quadrature modulator with and without the all-N-logic TSP BDL circuit at 1.5 V, and with and without the all-N-logic TSP BDL circuit at 5 V. At 1.5 V, with the all-N-logic TSP BDL circuit, the modulator works at a minimum clock-cycle time of 15.9 ns; without the all-N-logic TSP BDL circuit, it works at 20.2 ns. At 5 V, with the all-N-logic TSP BDL circuit, it works at a minimum clock-cycle time of 2.1 ns; without the all-N-logic TSP BDL circuit, it works at 2.15 ns. With the all-N-logic TSP BDL circuit, it works at a faster speed. Fig. 4 shows the clock-cycle time and the maximum operating frequency versus the supply voltage of the digital quadrature modulator with and without the all-N-logic TSP BDL circuit. At 5 V, the digital quadrature modulator works at a maximum operating frequency of close to 500 MHz. With the all-N-logic TSP BDL circuit, at 5 V the maximum operating frequency is slightly higher. As the supply voltage decreases, the maximum operating frequency decreases. At 1.5 V, with the all-N-logic TSP BDL circuit, its maximum operating frequency is 68 MHz, which is 27% faster than that without the all-N-logic TSP BDL circuit.

The speed limit of the all-N-logic TSP BDL circuit has been investigated by studying the performance of the implemented frequency divider. In order to maximize the operating frequency of the digital quadrature modulator, an internal clock signal generated from an on-chip ring oscillator and an on-chip digitally controlled oscillator has been implemented using the all-N-logic TSP BDL circuits and the conventional TSP circuits. The output of the internal clock signal for the quadrature modulator chip is also used in the frequency divider. Fig. 5 shows the measured clock-cycle time and maximum operating frequency versus supply voltage of the frequency divider using our all-N-logic TSP BDL and conventional TSP circuits. As is shown in the figure, at 5 V the frequency divider works at a maximum operating frequency of close to 550 MHz. With the all-N-logic TSP BDL circuit, at 5 V the maximum operating frequency is slightly higher. As the supply voltage decreases, the performance advantage of the all-N-logic TSP BDL circuit increases. At 1.5 V, with the all-N-logic TSP BDL circuit, its maximum operating frequency is 103.9 MHz, which is 32% faster than that using the conventional TSP circuits.

Fig. 3. Measured transient waveform of the CMOS quadrature modulator (a) with and (b) without the all-N-logic TSP BDL circuit at 1.5 V, and (c) with and (d) without the all-N-logic TSP BDL circuit at 5 V.

Fig. 4. Measured clock-cycle time and maximum operating frequency versus supply voltage of the digital quadrature modulator with and without all-N-logic TSP BDL.

IV. CONCLUSION

In this paper, a 1.5-V CMOS TSP BDL circuit using all-N-logic and bootstrapped circuit techniques has been described. As confirmed by the experimental results from the test chip implemented using a 0.8- μm CMOS technology, the speed performance of this CMOS all-N-logic TSP BDL circuit with four serial inputs is 75% faster at a supply voltage of 1.5 V, as compared to the conventional TSP dynamic-logic circuit. Using the all-N-logic TSP BDL circuit, the maximum operating frequency of an implemented digital-quadrature

Fig. 5. Measured clock-cycle time and maximum operating frequency versus supply voltage of the frequency divider.

modulator is 482 MHz at 5 V and 68 MHz at 1.5 V, which is 27% faster, as compared to the circuit without using the BDL circuit.

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Variable 2-D FIR Digital Filter Design and Parallel Implementation

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Abstract—The frequency response of a variable two-dimensional (2-D) digital filter is specified by several parameters called spectral parameters. The spectral parameters independently control the shapes of the variable frequency response. It is difficult to apply the existing frequency transformation-based methods to design such general variable 2-D filters. This paper proposes a general approach by assuming each filter coefficient as a multidimensional (M -D) polynomial of the spectral parameters, then the optimal coefficients of the (M -D) polynomials are found in the least-squares sense. Also, the paper shows that the resulting variable 2-D filters can be implemented in parallel form, so that parallel signal processing is possible.

Index Terms—Constant 2-D filter, digital filter, parallel implementation, variable 2-D filter.

I. INTRODUCTION

Digital filters with adjustable frequency responses are referred to as variable filters and are useful in communication systems, image processing, and filterbank designs. The existing methods for designing variable filters are well investigated and compared in a recent paper [1]. As mentioned in [1], most of the existing methods are based on frequency transformations [2]–[7]. In a more general case, the variable frequency response is controlled by several spectral parameters independently. For example, one parameter is for controlling the passband width, and the other is for controlling the stopband width independently. In such cases, the transformation-based methods are difficult to apply due to the frequency transformation constraints. To solve this problem, more general approaches are to find the filter coefficients as multidimensional (M -D) functions of the spectral parameters [8]–[10]. But many constant filters have to be predesigned before coefficient surface fittings. Another different approach is to reduce the difficult problem of designing a variable two-dimensional (2-D) filter to the easier one that requires 2-D constant filter designs and one-dimensional (1-D) polynomial approximations [11], but the decomposition of the given variable design specification is necessary. Yoshida et al. proposed a method for obtaining a 2-D variable filter

from the predesigned prototype 3-D constant filter [12]. Although the existing 3-D constant filter design methods can be directly applied, it is difficult to obtain the 3-D constant specification from the given 2-D variable specification because the method assumes one of the three frequencies as the function of the spectral parameter. This paper proposes a more general method, which directly assumes the variable 2-D finite-impulse response (FIR) filter coefficients as the M -D polynomials of the spectral parameters. This assumption avoids the indirect specification transformation from the 2-D variable to the 3-D constant one required in the above method. The proposed method is more flexible than the transformation-based methods. The optimal polynomial coefficients in the least-squares sense can be easily found by solving linear equations through minimizing the total squared error between the variable frequency-response specification and the actual one. Also, we show that the resulting variable filter can be implemented into the parallel structure, which is suitable for parallel signal processing. A design example is given to demonstrate the proposed technique.

II. DESIGN PROBLEM FORMULATION

We assume that

$$H_d(\Psi_1, \Psi_2, \dots, \Psi_k, \omega_1, \omega_2) = M_d(\Psi_1, \Psi_2, \dots, \Psi_k, \omega_1, \omega_2) e^{j\Phi_d(\omega_1, \omega_2)} \quad (1)$$

is the given 2-D variable frequency-response specification, where $\Psi_1, \Psi_2, \dots, \Psi_k$ are spectral parameters such as cutoff frequency, central frequency in the passband, bandwidth of the passband, transition bandwidth, or just a frequency increment as in (24). The spectral parameters make the 2-D frequency response continuously variable in the interested ranges

$$\begin{aligned} \Psi_1 &\in [\Psi_{1\min}, \Psi_{1\max}] \\ \Psi_2 &\in [\Psi_{2\min}, \Psi_{2\max}] \\ &\vdots \\ \Psi_k &\in [\Psi_{k\min}, \Psi_{k\max}]. \end{aligned} \quad (2)$$

In this paper, we use the 2-D filter with real-valued coefficients to approximate the specification (1), thus the frequencies ω_1, ω_2 should be taken in the ranges $\omega_1 \in [-\pi, \pi]$, $\omega_2 \in [0, \pi]$. Also, $\Phi_d(\omega_1, \omega_2)$ is a function of only ω_1 and ω_2 , which may be linear or nonlinear, but not variable. Here, we use the variable transfer function

$$H(\Psi_1, \Psi_2, \dots, \Psi_k, z_1, z_2) = \sum_{i_1=0}^{I_1} \sum_{i_2=0}^{I_2} C_{i_1 i_2}(\Psi_1, \Psi_2, \dots, \Psi_k) \cdot z_1^{-i_1} z_2^{-i_2} \quad (3)$$

to approximate the complex-valued variable specification (1), where $C_{i_1 i_2}(\Psi_1, \Psi_2, \dots, \Psi_k)$ are k -D coefficient polynomials

$$C_{i_1 i_2}(\Psi_1, \Psi_2, \dots, \Psi_k) = \sum_{l_1=0}^{L_1} \sum_{l_2=0}^{L_2} \dots \sum_{l_k=0}^{L_k} b(i_1, i_2, l_1, l_2, \dots, l_k) \cdot \Psi_1^{l_1} \Psi_2^{l_2} \dots \Psi_k^{l_k} \quad (4)$$

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