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Investigation of self-aligned p^{++} -GaAs/n-InGaP heterojunction field-effect transistors

W.-S. Lour^{a,*}, M.-K. Tsai^b, K.-C. Chen^a, S.-W. Tan^a, Y.-W. Wu^a, Y.-J. Yang^b

^aDepartment of Electrical Engineering, National Taiwan-Ocean University, 2, Peining Road, Roosevelt Road Sec. 4, Keelung, Taiwan, ROC

^bDepartment of Electrical Engineering, National Taiwan University, 1, Sec. 4, Roosevelt Road, Taipei, Taiwan, ROC

Abstract

p^{++} -GaAs/n-InGaP heterojunction field-effect transistors (HJFETs) with a highly carbon-doped gate and a wide-gap channel were reported. A self-aligned T-shaped gate HJFET exhibits a gate of 0.6 μm in length by depositing gate metal of 1.0 μm . DC characteristics including a turn-on voltage of 2.0 V at 1 mA/mm, a gate-drain breakdown voltage up to 30 V, a drain-source breakdown voltage exceeding 25 V, a maximum available transconductance of 160 mS/mm and AC performances such as a unit-current gain frequency of 16.8 GHz, and a unit-power gain frequency of 25 GHz were obtained for a non-self-aligned HJFET. With a self-aligned processing structure, the transconductance and f_{max} were improved to 230 mS/mm and 35 GHz, respectively. © 2002 Elsevier Science B.V. All rights reserved.

Keywords: Heterojunction field-effect transistor; Self-aligned; T-shaped gate

1. Introduction

The aluminum-free InGaP/GaAs material system has recently attracted considerable attention due to the favorable energy band line-up [1,2]. It is a promising material system for optoelectronic devices in the visible wavelength and long-wavelength ranges [3] as well as for use in high-speed electronic devices such as heterojunction bipolar transistors (HBTs) [4] and many kinds of field-effect transistors (like high electron mobility transistors and metal–insulator–semiconductor) [5–7]. To date, there is no experimental result related to InGaP/GaAs junction FET (JFET) that is a possible alternative to both HEMTs and MESFET-like devices [8]. Basically, the JFET offers

advantages of easy control in uniformity, threshold voltage, and Ohmic-type gate. However, it generally suffers from minority carrier (hole) storage effect, resulting in poor high-frequency performances. In this paper, we report on another type of InGaP/GaAs JFET with a p^{++} -GaAs heterostructure gate and a wide-gap InGaP channel. As expected, this hetero-JFET (HJFET) offers several advantages as described hereafter.

First of all, hole injection into the channel under positive gate bias is substantially reduced because of a large valence-band discontinuity (VBD) of 0.3 eV existing at the p^{++} -GaAs/n-InGaP hetero-interface, allowing a higher turn-on voltage and hence a higher output power. Secondly, with respect to the material growth, extremely high hole concentrations $> 10^{20} \text{ cm}^{-3}$ are attainable [9] by using carbon as the p-type dopant in GaAs. This achievable p-type doping results in a lower gate resistance and higher

* Corresponding author. Tel.: +886-2-24622192x6233; fax: +886-2-24635408.

E-mail address: wslo@mail.ntou.edu.tw (W.-S. Lour).

modulation efficiency. Moreover, a well-established selective etching technique enables precise gate length control down to sub-micrometer dimension [10]. Proper undercutting of the gate allows self-aligned fabrication since all electrodes are Ohmic types. Furthermore, a wide-gap channel provides a much higher breakdown voltage. This tremendously increases the power capability of devices. Because the breakdown voltage is proportional to E_g , the breakdown voltage of an InGaP channel should be 1.5 times higher than that of a GaAs channel.

2. Device structure and fabrication

The p^{++} -GaAs/n-InGaP HJFET structure was grown on a (100)-oriented semi-insulating GaAs substrate by MOCVD. The epitaxial growth started with a 5000-Å GaAs sub-buffer layer and a 2000-Å InGaP buffer layer. Next, a 2500-Å, $n = 1\text{--}2 \times 10^{17} \text{ cm}^{-3}$ InGaP channel layer was grown. Finally, a 4000-Å carbon-doped p^{++} -GaAs layer up to $5 \times 10^{19} \text{ cm}^{-3}$ was deposited. Another structure with the same HJFET except for an n-GaAs channel was also grown for comparison. Fig. 1 shows a typical HJFET band diagram with the corresponding layer parameters, in which a VBD of 0.3 eV prevents holes from being injected into the wide-gap channel. Therefore, an extremely highly doped gate could be deposited to reduce the parasitic gate resistance.

The device processing started with mesa isolation. The gate metallization and lift-off technique were used to define a 1- μm gate by traditional

Fig. 1. The HJFET band diagram with the corresponding layer parameters.

Fig. 2. (a) The top view of a non-self-aligned HJFET with an air bridge between the active region and the gate pad region, and (b) the SEM picture of a self-aligned T-gate structure with a reduced gate length.

photolithography and evaporation. This gate metal (Au) was directly used as a mask for removing the p^{++} -GaAs layer by selective wet chemical etching ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 3:1:50$) with controllable undercut resulting in a T-shaped gate structure and a reduced gate length. This gate length of the devices was measured to be 0.6 μm and was able to be controlled according to the etching time. Then, AuGe/Ni was deposited and alloyed as both drain and source Ohmic contact metal. Finally, gate feeder region was patterned and defined a window. Again, selective wet chemical etching was employed to remove the materials underneath the gate feeder, resulting in an air bridge gate. Fig. 2(a) shows the top view of a fabricated non-self-aligned HJFET with a T-shaped

gate (not clearly shown) and an air bridge between the active and the gate-pad regions. In the case of self-aligned HJFETs, the 1- μm gate metal was directly deposited after mesa isolation. Then, AuGe/Ni drain and source contacts were formed by using the T-gate as the mask in fashion. In addition to the reduced gate-source and gate-drain spacing, AuGe/Ni metal overlapped upon the Au-gate also features in improving the gate resistance since we use Au-gate as a mask to form the T-gate structure. Fig. 2(b) shows the T-gate structure with a reduced gate length.

3. Experimental results and discussion

Fig. 3 shows the typical I – V curve of a $\text{p}^{++}\text{-GaAs/n-InGaP}$ heterodiode. It reveals (1) a high turn-on voltage of ~ 2.0 V at 1 mA/mm, (2) a low reverse leakage current and a high breakdown voltage up to 30 V at 1 mA/mm. For a homodiode at the same current level, it exhibits a turn-on voltage of 1.0 ± 0.3 V and a breakdown voltage of 13.0 ± 2.0 V. Obviously, the heterostructure gate with a large VBD actually provides a higher turn-on voltage. With the wide-gap channel, an enhanced breakdown field is also provided. In addition, the proposed heterodiode shows much higher device uniformity as compared with the homodiode. All measured heterodiodes in the same chip exhibit nearly equal turn-on voltages and the same breakdown behaviors. However, the homodiode has both varying over a wide range. This is because of poor control in removing $\text{p}^{++}\text{-GaAs}$ without selective etching.

The DC characteristics of the typical $0.6 \times 100 \mu\text{m}^2$ non-self-aligned and self-aligned HJFETs are shown in Figs. 4(a) and (b), respectively. The available maximum transconductances are 160 and 230 mS/mm for non-self-aligned and self-aligned HJFETs, respectively. The difference between these two values is due to the parasitic resistance ($R_s = 3 \Omega \text{ mm}$ vs. $1.2 \Omega \text{ mm}$). Also, this somewhat larger resistance may result from a wide-gap n-InGaP channel. By simple calculation, the intrinsic transconductance and gate resistance are deduced to be 310 mS/mm and $0.14 \Omega \text{ mm}$, respectively. It can also be noted that both HJFETs exhibit a very low output conductance of 0.5 and 1 mS/mm, resulting in high open-drain voltage gain as high as 320 and 230, respectively. In spite of

Fig. 3. The typical I – V curves for a $\text{p}^{++}\text{-GaAs/n-GaAs}$ homodiode and a $\text{p}^{++}\text{-GaAs/N-InGaP}$ heterodiode.

Fig. 4. The common-source characteristics for: (a) non-self-aligned and (b) self-aligned HJFETs, respectively.

the possible large parasitic resistance associated with a wide-gap InGaP channel, it, however, significantly improves the breakdown behaviors. Breakdown voltages

Fig. 5. The measured transconductance and unity-current frequency (f_t) as a function of the gate-source voltage. The available unit-power gain frequencies (f_{max} 's) for a non-self-aligned and a self-aligned HJFET are 25 and 35 GHz, respectively.

exceed 30 and 7.5 V for non-self-aligned HJFETs with 3- μm drain-source spacing and self-aligned devices, respectively. In particular, the measured drain-source breakdown voltage is even as high as 25 V at zero V_{gs} bias voltage. Another advantage associated with the $\text{p}^{++}\text{-GaAs/n-InGaP}$ heterodiode is the high turn-on voltage. We find that drain current densities are up to 350, 400 mA/mm at $V_{\text{gs}} = +1.0 \text{ V}$ and transconductance remain as high as 80% peak value for a positive gate bias up to 1.5 V. Obviously, transconductance suppression associated with the homoJFETs is improved due to the large valence-band discontinuity in our HJFETs.

In order to further verify the hole injection suppression, the S -parameters of both devices were measured by HP8510B. As shown in Fig. 5, the measured f_t 's (f_{max} 's) are 16.8 (25) and 18.5 (35) GHz for non-self-aligned and self-aligned HJFETs, respectively. According to the relationship between f_t and v_s/L_g , the electron velocity, v_s , in an n-InGaP channel is estimated to be $6.3\text{--}7.2 \times 10^6 \text{ cm/s}$. Also note

that the much higher f_{max} for a self-aligned device as compared with the non-self-aligned one should be possible due to the reduced parasitic resistance. This phenomenon could be found in their $I\text{--}V$ curve, which reveals a smaller knee voltage (drain current saturated voltage) for a self-aligned HJFET.

4. Conclusion

In conclusion, we have firstly demonstrated the DC and AC performances of T-gate $\text{p}^{++}\text{-GaAs/n-InGaP}$ heterojunction FETs. Not only DC behaviors but also AC performances are significantly improved as compared with homojunction FETs. Furthermore, the electron velocity in a wide-gap InGaP channel is also estimated to be around $6.3\text{--}7.2 \times 10^6 \text{ cm/s}$.

Acknowledgements

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