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Studies and comparisons of a N^+ -InGaP/ $\delta(P^+)$ -InGaP/n-GaAs hetero-planar-doped structure to high-linearity microwave field-effect transistors

W S Lour¹, M K Tsai², K Y Lai¹, B L Chen¹ and Y J Yang²

¹ Department of Electrical Engineering, National Taiwan-Ocean University, No 2, Peining Road, Keelung, Taiwan, Republic of China

² Department of Electrical Engineering, National Taiwan University, No 1 Sec. 4, Roosevelt Road, Taipei, Taiwan, Republic of China

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Abstract

We report a promising N^+ -InGaP/ $\delta(P^+)$ -InGaP/n-GaAs hetero-planar-doped barrier, which is used to fabricate both high-breakdown and self-aligned T-gate (SAT-gate) field-effect transistors (FETs). The characteristics of the devices and comparisons with previous reports are discussed. The enhanced conduction- and valence-band offsets associated with the new hetero-planar doped barrier show high-breakdown behaviour. In addition, high selective etching between InGaP and GaAs layers together with an ohmic gate allows the fabrication of a SAT-gate with a reduced gate-length of $0.8\ \mu\text{m}$. In the case of a high-breakdown FET, the drain–source breakdown voltage is as high as 32 V. In addition to competitive direct-current (dc) performances, a reduced knee voltage and improved frequency performances are obtained in SAT-gate FETs. The available unity-current-gain and unity-power-gain frequencies are, respectively, 19.5 and 30 GHz achieved as a $0.6\ \mu\text{m}$ gate is obtained by forming a $1\ \mu\text{m}$ metal gate. Furthermore, all the measured SAT-gate FETs exhibit high-linearity and high-uniformity dc and alternating-current performances.

1. Introduction

One of main advantages associated with planar-doped-barrier field-effect transistors (FETs) is that it is possible to engineer larger barriers inside a semiconductor than with metal–semiconductor Schottky ones [1, 2]. In general, the barrier height obtained from a planar-doped structure is determined by the parameters of the associated layers and is as large as the bandgap. Another merit of planar-doped-barrier FETs is that all electrodes including the drain, the source, and the gate are ohmic in type. Compared with conventional MESFET-like devices, the deposition sequence of the corresponding metal electrodes for planar-doped-barrier FETs is exchangeable. This indicates that the gate metal can be deposited before the formation of the drain and the source. Therefore, some self-

aligned gate FETs (SAG-FETs) have been fabricated using planar-doped-barrier structures [3]. However, the barrier height of a planar-doped structure is not fixed and varies with an applied gate voltage [2]. It reduces as the reverse gate-to-drain or gate-to-source voltage increases. Furthermore, there are still some inherent problems associated with conventional SAG-FET. For example, the breakdown voltage is very small. The reported breakdown is generally in the range 2 to 7 V. It is also difficult to precisely control the etching process before drain and source metal deposition, resulting in low processing yield and poor device uniformity. Further improvements in SAG-FETs regarding production yield and reliability are needed.

Recently, the InGaP/GaAs system has been widely used in the fabrication of novel devices, such as hetero-junction FETs (HFETs) [4, 5] and hetero-junction bipolar transistors

Figure 1. Schematic cross-section of a SAT-gate (left-hand side) and a conventional (right-hand side) FET. Note: not to scale.

(HBTs) [6–8]. More recently, an InGaP layer used in planar-doped-barrier FETs has also been reported [9]. Lour *et al* reported an improved breakdown and a reduced leakage current in [9]. However, the $\delta(P^+)$ -InGaP layer used is very thin and is not suitable for precisely controlling T-gate formation. In this paper, we further report a promising N^+ -InGaP/ $\delta(P^+)$ -InGaP/n-GaAs hetero-planar-doped structure, which is used to fabricate both high-breakdown and self-aligned T-gate FETs (SAT-gate FETs). In the case of a high-breakdown FET, a gate of $0.8 \mu\text{m}$ in length is obtained by forming a $1 \mu\text{m}$ metal gate. An enhanced barrier using an additional conduction-band offset prevents the gate-to-drain leakage before the breakdown phenomenon occurs. With considerable experience in creating high-breakdown FETs, the authors have successfully fabricated a SAT-gate FET using the same structure. By virtue of selectively over-etching the n^+ -GaAs and N^+ -InGaP layers after the gate-metal deposition, the authors have successfully fabricated a T-gate with a reduced gate dimension. The key features of the proposed device include: (1) a T-gate with two separate etching processes exhibiting a reduced capacitance and hence improving the frequency performances; (2) an SAT-gate exhibiting a reduced parasitic resistance; and (3) enhanced breakdown voltage.

2. Device structure and fabrication

The device structure used in this study is grown on a (100)-oriented semi-insulating GaAs substrate by LP-MOCVD. It consists of a $0.5 \mu\text{m}$ GaAs buffer, a $0.2 \mu\text{m}$ $n = 1 \times 10^{17} \text{ cm}^{-3}$ GaAs channel layer, a 10 nm $\delta(P^+) = 5 \times 10^{18} \text{ cm}^{-3}$ InGaP layer, a $0.2 \mu\text{m}$ $N^+ = 6 \times 10^{18} \text{ cm}^{-3}$ InGaP layer, and a $0.2 \mu\text{m}$ $n^+ = 8 \times 10^{18} \text{ cm}^{-3}$ GaAs cap layer. The n^+ -GaAs cap layer and the N^+ -InGaP layer are thick enough to prevent the gate metal from being electrically shorted to the drain and the source in the SAT-gate fabrication. The N^+ -InGaP/ $\delta(P^+)$ -InGaP/n-GaAs structure, instead of n^+ -GaAs/ $\delta(P^+)$ -InGaP/n-GaAs, forms a camel diode to voltage-modulate the channel current. The fabrication of a SAT-gate FET starts with mesa isolation. The ohmic gate is fabricated by depositing Au with a standard lift-off technique. Note also that the contact type for the gate electrodes is ohmic and thus no etching process is needed before the gate metal deposition. Au is then directly used as an etching mask and a T-gate is fabricated with two separate over-etching processes of n^+ -GaAs and N^+ -InGaP layers. First, the n^+ -GaAs layer is selectively over-etched in $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 3 : 1 : 50$ solution. The etching rate of

the GaAs layer is about $150 \text{ \AA s}^{-1}$, which is much greater than that of the InGaP layer. The N^+ -InGaP layer is then selectively over-etched using $\text{HCl}:\text{H}_3\text{PO}_4 = 1 : 1$ solution. The fact that this two-step selective etching forms a T-gate with a reduced length is the main feature of the proposed structure as compared with that in [9]. Finally, a contact metal layer for the drain and the source is deposited and alloyed. The threshold voltage is designed and/or determined by the parameters of the associated layers. The conducting current is also well controlled by precisely depositing ohmic metal upon the GaAs channel after selectively removing the highly doped layers. In other words, high-uniformity behaviours are still expected even if we use an N^+ -InGaP/ $\delta(P^+)$ -InGaP/n-GaAs camel diode. The fabrication of a high-breakdown FET is implemented using the conventional processing procedures. Figure 1 shows the corresponding cross-sections for a SAT-gate and high-breakdown FETs. It includes the processing steps and the corresponding geometrical dimensions for both devices.

Figure 2 shows the scanning electron microscopy (SEM) pictures for SAT-gate FETs with regard to some processing steps. The available metal gates formed by photolithography are 2 , 1.5 , and $1 \mu\text{m}$ in length. The measured effective gate dimensions are $1.5 \times 100 \mu\text{m}^2$ and $0.6 \times 100 \mu\text{m}^2$ as the dimensions of the deposited gate metal are $2 \times 100 \mu\text{m}^2$ and $1 \times 100 \mu\text{m}^2$, respectively. In fact, the gate length is controlled by the over-etching time. Therefore, a further downscaled gate dimension is expected. As shown in figure 2(a), in which the device after two separate over-etching processes is presented, the effective gate-length is even reduced to $0.2 \mu\text{m}$. Figures 2(b) and (c) show the top- and side-view SEM pictures for the finished SAT-FET. The over-etching processes of an n^+ -GaAs and an N^+ -InGaP layers make the effective gate-length shorter than the deposited gate metal. The measured gate-length is $0.6 \mu\text{m}$ and there exists a $0.2 \mu\text{m}$ spacing between the gate and the drain electrodes. Another SEM picture (not shown here) for a conventional $1 \mu\text{m}$ gate-metal FET shows a $0.8 \mu\text{m}$ gate-length after removing the n^+/N^+ layers. An additional AuGe layer overlapping upon the Au ohmic gate for the SAT-FET is further deposited to improve the contact resistance.

3. Experimental results and discussion

Figures 3(a) and (b) show the common-source I - V characteristics for a SAT-gate and a conventional FET,

Figure 2. The SEM pictures for (a) an ohmic gate after two separate over-etching procedures, (b) top view and (c) side view of a finished SAT-gate FET.

respectively. The gate dimension for the SAT-gate FET is $1.5 \times 100 \mu\text{m}^2$ while that for a conventional FET is $0.8 \times 100 \mu\text{m}^2$. Both I - V curves exhibit good pinch-off behaviours with nearly equal threshold voltages. All the devices fabricated on the same chip exhibit threshold voltages of -4.5 ± 0.1 V. This indicates that good device uniformity can be expected for the planar-doped-barrier FETs. The drain-to-source breakdown

Figure 3. Common-source current-voltage characteristics for (a) a SAT-gate ($1.5 \times 100 \mu\text{m}^2$) and (b) a conventional ($0.8 \times 100 \mu\text{m}^2$) FET, respectively.

voltages at $V_{GS} = 0.0$ V are found to be >10 and >23 V for SAT-gate and conventional FETs, respectively, with the maximum values obtainable being as high as 12 and 32 V, respectively.

In order to realize the high-breakdown behaviours, we refer to figure 4(a) that illustrates the band diagram of the proposed device. It is sketched by solving Poisson's equation. As shown in the figure, the $\delta(P^+)$ -InGaP layer is thin enough and assumed to be fully depleted. It is obvious that the planar-doped barrier is dominated by N^+ -InGaP/ $\delta(P^+)$ -InGaP. The adjustable barrier height could be as high as the energy gap of an InGaP layer, which is much larger than that formed by the GaAs homo-type (dashed curve). According to the band diagram shown in figure 4(a), there are extra conduction and valence barriers located at the InGaP/GaAs hetero-interface. In the case of a conventional FET, the breakdown is limited by the gate-drain behaviour. The barrier height is reduced by increasing the drain-to-source voltage (and hence the gate-drain voltage). However, the enhanced conduction-band offset is 0.2 eV and hence the effective barrier height is large enough to prevent electrons from being injected into the drain electrode. Therefore, the device reveals a small leakage current, a large output resistance and a high breakdown voltage. In contrast, the drain-source terminal limits the breakdown

Figure 4. (a) Energy band diagram of a new n^+ -GaAs/ N^+ -InGaP/ $\delta(p^+)$ -InGaP/ n -GaAs hetero-planar-doped structure. Dashed curve is for the homo-type one. (b) The measured current-voltage behaviour of the gate-drain terminal in this study and that in [2].

voltage of an SAT-gate FET since it exhibits a small drain-to-source spacing and hence a small gate-to-drain spacing, that is, the breakdown phenomenon for a SAT-gate FET that occurs before the gate barrier is seriously reduced by the gate-drain bias. Another increase in gate leakage current at a high drain-to-source voltage is caused by the holes generated by impact ionization. Thus, hole confinement should be as good as possible to prevent the holes generated by impact ionization from reaching the gate contact. Fortunately, a valance-band offset of 0.3 eV can effectively suppress any hole leakage current. Undoubtedly, the limited spacing between the T-gate and drain is also helpful in the breakdown. Figure 4(b) compares the breakdown behaviour of the proposed structure and that in [2]. In spite of the different channel approach, the voltage-dependent barrier height was also observed in those lithographically aligned FETs. We find that the leakage current gradually increases on increasing the voltage close to the breakdown regime.

Another interesting aspect is the knee voltage, which dominates the power dissipation in digital circuit applications. The corresponding values at $V_{GS} = 0.0$ V, as shown in figure 3, are 1.5 and 3.0 V for a SAT-gate FET and a conventional FET, respectively. This is a benefit of a SAT-gate structure. Due to the reduced gate-source spacing and gate-drain spacing in a SAT-gate FET, the series resistance is significantly improved and hence a smaller drain-source voltage (i.e., a smaller knee voltage) is enough to collect the output current. Figure 5 shows

Figure 5. Common-source current-voltage characteristics for a SAT-gate FET with a $0.6 \mu\text{m}$ gate.

the source-ground I - V characteristics for a SAT-FET with a $0.6 \mu\text{m}$ gate-length. It demonstrates nearly the same current and the same transconductance with a somewhat smaller breakdown voltage ($\sim 9 \pm 0.5$ V) and a much smaller knee voltage (0.5 V) compared with those shown in figure 3(a). Clearly, both the narrower drain-source spacing (1 versus $2 \mu\text{m}$) and the shorter effective gate-length (0.6 versus $1.5 \mu\text{m}$) further reduce the knee voltage in the current-voltage characteristics. Figure 6 presents the direct-current (dc) comparisons between SAT-gate FETs and a conventional FET. It shows the transconductance and the current density as a function of the gate-source voltage. The parameter used is the drain-source voltage. In the case of a conventional FET, the measured transconductance and current density are very sensitive to the applied drain-source voltages. With a fixed drain-source voltage of 2.0 V, there shows peak transconductance (60 mS mm^{-1}) and poor device linearity. Increasing the drain-source voltage to 3.5 V, the transconductance versus the gate-source voltage profile exhibits a broad plateau. The common transconductance also increases to 70 mS mm^{-1} . The current densities exhibit the same behaviour. In other words, the device linearity (current and transconductance) is not obtainable until a drain-source voltage > 3.5 V is applied. The transconductance versus the gate-source voltage profile for a SAT-gate FET, however, exhibits good device linearity even if the applied drain-source voltage is reduced to +1.5 V. The gate voltage swing with good linearity is > 3 V since the drain-source voltage is in the range of $1.5 \sim 12$ V. This is because the SAT-gate FET was fabricated with a smaller gate-drain spacing and therefore a higher electric field can be achieved by applying a low drain-source voltage ($V_{DS} = 1.5$ V). On the other hand, the conventional FET was fabricated with a larger gate-drain spacing and therefore a high electric field can be obtained only by applying a higher drain-source voltage. At $V_{DS} = 3.5$ V the behaviour of the conventional FET is close to that exhibited by a SAT-gate FET. Of course, the devices studied can be further improved by optimizing the channel doping profile and/or the channel properties [2, 9]. Another reason for the smaller transconductances compared to those previously reported is possibly due to the weaker channel modulation efficiency of a N^+ -InGaP layer. This is not altogether disappointing in terms of our consideration of the frequency performances, as will be discussed next.

Figure 6. Measured transconductance and current density as a function of the gate-source voltage. The used parameter is the drain-source voltage.

Figure 7. Measured unity-current-gain and unity-power-gain frequencies as a function of gate-source voltage.

The proposed SAT-gate is aimed at improving the frequency performance. In spite of a somewhat small transconductance, the frequency performance is directly related to the electron velocity and the gate dimension. The smaller gate-length is, the superior the frequency performance is. Therefore, we measured gains at a microwave frequency using a HP 8510 B. Figure 7 shows the unity-current-gain

and unity-power-gain frequencies as a function of the gate-source voltage for the fabricated devices. In the case of conventional FETs, the f_t seriously degrades on increasing the gate-source voltage at $V_{DS} = 2.0$ V. This behaviour is the same as the dc performance. As V_{DS} increases to 3.5 V, the measured f_t displays a broad plateau. This means the device linearity is poor until $V_{DS} = 3.5$ V. Both the 1.5 and 0.6 μm

gate SAT-gate devices, however, exhibit f_t broad plateaus at $V_{DS} = 2.0$ V. This again is a benefit of reduced parasitic resistance. The maximum f_t values (f_{max}) are 13 (21), 9 (28), and 19.5 (30) GHz for 0.8 μm gate conventional FETs, 1.5, and 0.6 μm SAT-gate devices, respectively. In addition to reduced resistance, reduced capacitance also improves frequency performances. Experimental results reveal that the downscaled gate dimension really improves and enhances the frequency performances.

4. Conclusions

We have successfully fabricated both high-breakdown and SAT-gate FETs using a promising planar-doped-barrier structure. In the case of dc performance for a SAT-gate FET, both a small knee voltage and an acceptable breakdown voltage are observed. In spite of a somewhat small extrinsic transconductance, an improved alternating-current (ac) performance is still obtainable. The key merits are a reduced parasitic resistance and a small effective capacitance by a SAT-gate with a reduced length. All the SAT-gate FETs exhibit both high-linearity and high-uniformity dc and ac performances.

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