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Dual-gate $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ pseudomorphic high electron mobility transistors with high linearity and variable gate-voltage swing

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Abstract

$\text{In}_{0.5}\text{Ga}_{0.5}\text{P}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ pseudomorphic high electron mobility transistors (PHEMTs) fabricated using single- and dual-gate methodologies have been characterized with special emphasis on precisely controlling the device linearity and the gate-voltage swing. A composite channel employing a GaAs delta-doped ($\delta(n^+)$) sheet and an undoped $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer characterizes the key features of the proposed PHEMT profile. Better carrier confinement for both the electron and the hole due to the InGaP/InGaAs hetero-interface and superior carrier transport properties at the channel/buffer interface, together with the redistributed carrier profile, contribute to high-linearity performances. On the other hand, high etching selectivity between the GaAs cap and the InGaP Schottky layers makes it possible to precisely position both of the gates. The gate-voltage dependence of transconductance for the first equivalent gate with several V_{GS2} shows that the available gate-voltage swing is in the range 0–4.0 V.

1. Introduction

The aluminium-free InGaP-based compounds lattice matched to GaAs substrates have recently attracted considerable attention due to the favourable energy band line-up [1]. The InGaP/GaAs heterostructure generally exhibits a large valence-band discontinuity (ΔE_V) and a small conduction-band discontinuity (ΔE_C), which is suitable for heterojunction bipolar transistors (HBTs). There are fewer trap-related centres and stronger resistance to oxidization compared to AlGaAs/GaAs, which is believed to improve the reliability for both HBTs and FETs. On the other hand, high etching selectivity of phosphorus-containing layers with respect to arsenic-containing layers is very promising for simplifying device fabrication. A great number of high-speed electronic devices such as HBTs [2] (HBTs) and many kinds of field-effect transistors [3–5] (FETs) have been intensively

studied and reported. There are numerous applications and business opportunities in wireless communication, data transmission, high-speed networking and cellular/PCS phones, which require billions of such high-performance electronic components. In recent years, the applications in wireless communication have maintained a steady and sustained growth. As the microwave frequencies to broadband wireless access applications, the HFET, in particular HEMT and pseudomorphic high electron mobility transistors (PHEMTs), will become the exclusive choice. In spite of the poor device linearity, the FET has its performance advantage over its rival (HBT) in terms of operation voltage. Due to the relatively high turn-on voltage, the HBT cannot operate below 2.5 V while maintaining high power efficiency. In contrast, the HEMT has demonstrated high efficiency at the operation voltage of 1.5 V. This can not only reduce the power consumption tremendously but also enhance the

Figure 1. The schematic cross section of fabricated PHEMTs with DGs and SG.

lifetime. However, the device linearity is now becoming more important as the applications of digital circuits in the future cellular/PCS phones are concerned. Therefore, it is necessary to improve the linearity of the FET. Recently, Lour *et al* [3,4] have reported InGaP/InGaAs PHEMTs with a doped channel resulting in high linearity and temperature-dependent reliability, respectively. Their experimental results reveal that such a doped-channel structure really provides the required linearity with low signal distortion. This paper is aiming to propose and fabricate a new InGaP/InGaAs PHEMT with high device linearity. In particular, dual-gate (DG) fabrication was demonstrated to precisely control the gate-voltage swing (GVS) in the range from 0 to 4.0 V. Though some high-linearity InGaP-based FETs have already been reported, DG fabrication and experimental results by InGaP/InGaAs are first reported.

2. Device structure and fabrication

The InGaP/InGaAs pseudomorphic HEMT structure was grown on a (100)-oriented semi-insulating GaAs substrate by MOCVD. As shown in figure 1, the epitaxial structure is composed of a 8000 Å GaAs buffer layer, a composite channel including a delta-doped sheet of $\delta(n^+) = 2 \times 10^{12} \text{ cm}^{-2}$ and a 100 Å undoped $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer, a 50 Å $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$ spacer, a delta-doped sheet of $\delta(n^+) = 3 \times 10^{12} \text{ cm}^{-2}$, a 300 Å $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$ Schottky layer and a 100 Å GaAs cap layer of $n^+ = 3 \times 10^{18} \text{ cm}^{-3}$. The MOCVD precursors utilized were TMGa, TMIIn, AsH₃, PH₃ and SiH₄. The upper delta-doped sheet serves as a two-dimensional electron gas (2DEG) supplying layer while the lower one is used to modify and optimize the distribution of the electrons. After the epitaxial growth was completed, the device fabrication started with mesa isolation. Both single-gate (SG) and DG PHEMTs were fabricated on the same chip for comparison. AuGe/Ni was deposited and alloyed as ohmic contacts for both the drain and the source by conventional optical lithography and evaporation. The drain-source spacing is 5 μm. Then the n^+ -GaAs cap layer was removed by selective wet chemical etching in a $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 3 : 1 : 50$ solution. Such high selectivity etching between the cap layer and the Schottky layer produces equal threshold voltages for the first and the second gates. Finally, the Au gate metal was deposited by evaporation and lifted off to define a 1 μm gate. Figure 1 shows schematic cross sections of both a SG PHEMT and a DG PHEMT. In

Figure 2. The common-source current–voltage characteristics for the SG PHEMT operated in the (a) enhancement mode and (b) depletion mode.

the case of the DG PHEMT, the first and the second gates are formed between two ohmic contacts and separated from each other by a spacing of 1 μm. In contrast, a single gate of 1 μm is located in the centre of the region between the ohmic contacts for SG PHEMT.

3. Experimental results and discussion

In this paper, a composite channel employing a GaAs delta-doped ($\delta(n^+)$) sheet and an undoped $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layer characterizes the key features of the proposed PHEMT profile. The sheet density and the electron mobility obtained by Hall measurements are 3.7×10^{12} (3.1×10^{12}) cm^{-2} and 3600 (17300) $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 300 K (77 K), respectively. In spite of a lattice mismatch of 1.43% to GaAs and/or InGaP ((5.7342 – 5.6532)/5.6532), the $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ really works well as a promising channel. Besides, the additional energy-gap difference of 0.213 eV between GaAs and $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ layers also benefits the confinement of electrons. In particular, this energy-gap difference is much more important than considering the small conduction-band discontinuity associated with the InGaP/GaAs hetero-interface. As we will see in the device characteristics, there is no parallel conduction or transconductance suppression taking place under the forward-biased condition.

Figures 2(a) and (b) are the common-source current–voltage characteristics under depletion and enhancement modes, respectively, for the SG PHEMT. The available current densities at $V_{\text{GS}} = 0$ and +2.5 V are 295 and 445 mA mm^{-1} , respectively. Note that neither parallel conduction nor severe transconductance suppression is observed even if the +2.5 forward bias is applied. It is also found that the SG PHEMT studied exhibits a low output conductance of $0.5 \pm 0.1 \text{ mS mm}^{-1}$ at $V_{\text{GS}} = -1 \text{ V}$. The insignificant negative differential resistance is believed to result from the high-field transfer electron effect. All of the experimental results reveal that both InGaP/InGaAs and InGaAs/GaAs

Figure 3. The common-source current–voltage characteristics for the DG PHEMT with the gate2–source voltage as a parameter: (a) $V_{GS2} = +0.5$ V, (b) $V_{GS2} = 0$ V, (c) $V_{GS2} = -0.5$ V and (d) $V_{GS2} = -1.0$ V. Note that the top line represents $V_{GS1} = 0$ V.

Figure 4. The current and transconductance as a function of gate–source (gate1–source) voltage.

hetero-interfaces offer enough efficiencies of confinement for electrons. Another advantage associated with the proposed structure is the highly selective etching between an InGaP Schottky and a GaAs cap layers. This makes it possible to precisely position the gate metal on the InGaP Schottky layer. More than 50 devices on the same wafer are tested, and accordingly a threshold voltage of -3.7 ± 0.1 V is obtained. According to the high uniformity available in the proposed structure, both threshold voltages of $V_{T1,2}$ will be nearly equal in the case of the DG PHEMT (subscript ‘1’ and ‘2’ specifies the first and second part of the DG PHEMT, respectively).

Figures 3(a)–(d) show the common-source current–voltage curves with $V_{GS2} = +0.5$ V at a rate of -0.5 V per step as a parameter. In order to understand the DG PHEMT behaviour, we refer to the first-order description of the DG PHEMT constructed by employing the channels of two SG devices connected in series. According to this simplified model, the second device close to the drain terminal is regarded as a load line for the first one. The I – V characteristics are

determined by intersection of the two PHEMT I – V curves. First, it is found that both gates, as expected, have identical threshold voltages of -3.7 V. The second-gate device will operate in enhancement mode and the unsaturated region with a positive V_{GS2} . Meanwhile, as shown in figure 3(a), the I – V curves of the first device in the depletion mode are almost the same as those of an SG device. Increasing the V_{GS2} more negatively, the first device approaches the unsaturated region and the second approaches the saturated region, as V_{GS1} is not large enough. This corresponds to the transconductance suppression region since the second device clamps the modulation of the channel by the first one, whereas, as shown in figures 3(c) and (d), the I – V curves of the first device still work normally with high-linearity performance at large V_{GS1} . This is much more interesting in considering one of the principal applications of the DG FET to be a high-frequency mixer, which has typically achieved very high conversion gains even with a low local oscillator (LO) power due to the strong nonlinearity of transconductance resulting from the suppression by the second gate. We find, in figure 3(b) with $V_{GS2} = 0$ V, the suppressed transconductance is smaller than 20 mS mm^{-1} at $V_{GS1} = 0$ V while it is unchanged at $V_{GS1} < -1$ V. We also find, at $V_{GS2} = -0.5$ and -1 V, the suppressed-to-normal transconductance ratios are further reduced, resulting in high nonlinearity between two operation regions.

Concerning device linearity and associated effects by the second gate in DG PHEMT, we refer to figure 4 depicting the current and transconductance as a function of V_{GS1} (V_{GS}). We find that the g_m – V_{GS} profile for the SG PHEMT really displays a broad plateau. The GVS defined as a voltage range with 80% of the peak value of g_m is even larger than 4.5 V. Clearly, the upper delta-doped sheet serving as a 2DEG-supplying layer and the lower one used to optimize the distribution of carriers really contribute to high device linearity. The

Figure 5. The relation between the GVS and bias of the second gate.

measured transconductance is 85 mS mm^{-1} . However, this is not altogether disappointing considering an available open-drain voltage gain as large as 170 ($g_m/g_d = 85/0.5$). Due to the extrinsic linearity and high uniformity obtained in SG $\text{InGaP}/\text{InGaAs}$ PHEMT, the controllable GVS in g_m versus V_{GS1} is expected by the DG approach. Referring to figure 4 again, the V_{GS2} -dependence transconductances of the first equivalent gate also display plateaux. The transconductance upon the plateau region is 90 mS mm^{-1} with extremely small output conductance. The obtained GVS is reduced, as the biased voltage of the second gate becomes more negative. Note also that output current density is reduced from 310 to 190 mA mm^{-1} as V_{GS2} is reduced from $+0.5$ to -1.0 V , corresponding to the clamp of the modulation of the channel by the second gate. Figure 5 shows the relation between the GVS and the biased voltage of the second gate. It is found that the variable VGS values are in the range of 0 – 4.0 V and are nearly proportional to V_{GS2} . By increasing the V_{GS2} positively to $+1.0 \text{ V}$ or larger, one can obtain GVS of the DG PHEMT to be the same as that of the SG PHEMT. In practice, the overall performance in our three-terminal DG PHEMT by floating the second gate (figure 6(a)) is nearly the same as in the SG HEMTs. With comparisons between figures 2(b) and 6(a), we find both have nearly equal output current densities, threshold voltages, and GVSs.

Pseudomorphic HEMTs are widely used in wireless communications at present due to their better transport properties of a narrow-gap channel like InGaAs . However, they generally suffer from both low breakdown voltage and high output conductance caused by impact ionization in their narrow-gap channels. Since the narrow-gap InGaAs channel is also employed in our PHEMT, the breakdown behaviour will be studied and discussed as follows. Basically, there are two major mechanisms responsible for device breakdown and leakage. These are the gate–drain breakdown and the drain–source breakdown. The measured gate–drain (gate1–drain) breakdown voltage is 12 V for the SG PHEMT while it is 18 V for the DG PHEMT. The breakdown voltage is defined at a leakage current of 1 mA mm^{-1} . To further investigate the effects of the second gate on this type of breakdown, we measured the gate1–drain breakdown under various V_{GD2} (gate2–drain voltage) including floating, short and $+2.0$ to -3.0 V . It is found that all measured breakdown voltages are fixed at 18 V . Thus we believe the higher breakdown as compared with SG PHEMT is attributed to the $3 \mu\text{m}$ gate–drain spacing ($2 \mu\text{m}$ for SG HEMT). In the

Figure 6. (a) The three-terminal current–voltage characteristics for the DG PHEMT measured by floating the second gate. (b) The common-source current–voltage characteristics for the DG PHEMT with the gate1–source voltage as a parameter. Note that the top line represents $V_{GS2} = 0 \text{ V}$.

case of the drain–source breakdown, we refer to the off-state breakdown in common-source characteristics for both SG and DG PHEMTs. In order to realize the effects of the second gate on this type of breakdown, figures 2(b), 3(b) and 6(a) are compared. Note that the differences between these I – V curves are SG in figure 2(b), shorted and floated second gate in figures 3(b) and 6(a), respectively. Meanwhile, all have their gate–drain leakage currents as being negligible. Experimentally, devices such as SG HEMT and DG HEMT with floating second gate exhibit similar off-state leakage and output characteristics, whereas figure 3(b) shows a smaller off-state leakage as compared with figures 2(b) and 6(a) at the same V_{DS} . This is because the effective V_{DS1} ($V_{DS} - V_{DS2}$) is insufficient to generate impact ionization. Therefore, in addition to the low output conductance, the reduced leakage, and the enhanced drain–source breakdown voltage, benefits concerning noise behaviour are expected for the DG $\text{InGaP}/\text{InGaAs}$ PHEMT.

The S parameters of a fabricated DG PHEMT are measured by directly shorting the second gate to the source, together with those of a SG PHEMT on the same wafer. The microwave measurements were performed from 0.5 to 20 GHz using an HP8510B network analyser in conjunction with the Cascade probes at room temperature. The maximum current gain cut-off frequency and maximum oscillation frequency, measured at $V_{DS} = 5 \text{ V}$ and $V_{GS(1)} = -2 \text{ V}$, are 14 (16) and 22 (30) GHz , respectively, for a DG PHEMT (SG PHEMT).

4. Conclusions

First we have demonstrated $\text{InGaP}/\text{InGaAs}$ PHEMTs fabricated using SG and DG methodologies. The SG PHEMT

shows high linearity performance with a GVS of 4.5 V. On the other hand, the V_{GS2} -dependence transconductance for the first equivalent gate shows that the GVS available is in the range 0–4.0 V. The high nonlinearity and linearity observed in transconductance suppression and action regions associated with DG PHEMT makes it very promising in applications to a mixer. Besides, the DG PHEMT is an important device in high speed digital integrated circuits. When combined with a suitable load device between its drain and a positive supply rail, the DG HEMT provides the basic logic function of a NAND gate within a very compact area. This can be seen in figure 6(b) by the modulation of channel current controlled by the second equivalent gate.

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