A 3–8 GHz Delay-Locked Loop With Cycle Jitter Calibration

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Abstract—A 3–8 GHz delay-locked loop (DLL) with cycle jitter calibration is presented. To lower the operation frequency of a voltage-controlled delay line (VCDL), this DLL adopts the dividers, an edge combiner, and the multiple VCDLs. A duty cycle correction circuit is presented to maintain the output duty cycle of 50%. This DLL has been fabricated in 90-nm CMOS process. The measured peak-to-peak jitters at 8 GHz are 11.44 and 6.67 ps before and after calibration, respectively. The power dissipation at 8 GHz is 18 mW for a supply voltage of 1.2 V, and the measured output duty cycle variation is less than 3%.

Index Terms—Calibration, cycle jitter, delay-locked loop (DLL), duty cycle correction, edge combiner.

I. INTRODUCTION

The delay-locked loop (DLL) is widely used for clock generation [1], clock deskewing [2], and data recovery [3]. In the recent years, the speed demand for the data transmission rate between chips is increasing. Although the DLL is unconditionally stable and has no jitter accumulation, it has several problems to operate the DLL at a very high frequency. First, a conventional phase/frequency detector [4] acts a phase detector (PD) in a DLL. The maximal operation frequency of a PD is limited by the reset path delay in a PD. Second, the linear detection range of a PD [4] is within ±T_{ref}, where T_{ref} is the period of the operation frequency. When the operation frequency of a DLL increases, the corresponding T_{ref} decreases. If the intrinsic delay of a voltage-controlled delay line (VCDL) is large than the linear detection range of a PD, the harmonic locking issue occurs. Third, for the charge pump (CP), when the operation frequency increases, the short turn-on pulse width may result in the current mismatch in a CP. It will induce the static phase error significantly. Fourth, once the operation frequency increases, the required bandwidth of the delay cells in a VCDL has to increase also. The VCDL will consume a lot of power.

To lower the operation frequency of a VCDL, the proposed DLL adopts the dividers, an edge combiner, and the multiple VCDLs. It not only relaxes the speed requirement of the VCDL, but also avoids the VCDL to operate at the highest frequency. However, the multiple VCDLs may contribute the undesired cycle jitter. A cycle calibration method is used to improve the cycle jitter. The proposed DLL and its circuits are discussed in Section II. The experimental results are presented in Section III. Finally, the conclusions will be given in Section IV.

II. CIRCUIT DESCRIPTION

The proposed DLL is shown in Fig. 1. It is composed of two divide-by-N dividers, the PDs, the CPs, an edge combiner, a voltage-to-current converter (V/I), the capacitors, buffers, and multiple VCDLs. The input clock C_{K_{in}} passes through the input buffer and is divided by the forward-path divide-by-N divider. The multiphase outputs P_{1}–P_{N} are realized and they pass the VCDLs to generate the outputs V_{1}–V_{N}, respectively. Note that the frequency of P_{1}–P_{N} and V_{1}–V_{N} is 1/N of the input clock. The edge combiner combines the multiphase outputs V_{1}–V_{N} to generate the output clock C_{K_{out}}, which has the same frequency of the input clock. The output clock is divided by the feedback-path divide-by-N divider, and the multiphase outputs P_{1}–P_{N} are realized. The PDs and CPs generate the controlled voltages V_{C1}–V_{CN} to control the VCDLs. In the steady state, the input and output clocks will be synchronized. To have the output duty cycle of 50%, the voltage-to-current converter is adopted to adjust the duty cycle of the output clock. By the forward-path and feedback-path divide-by-N dividers, the speed requirement for the VCDLs, the PDs, and CPs is relaxed by N times [5]. Moreover, the linear detection range of the PD is enlarged by the divide-by-N divider and is explained later.
Fig. 2 shows a simplified timing diagram of the proposed DLL with \( N = 4 \). For two divide-by-\( N \) dividers (\( N = 4 \)), they generate the multiphase outputs \( P_1 \)–\( P_4 \) and \( F_1 \)–\( F_4 \), respectively. The VCDLs generate the multiphase outputs \( V_1 \)–\( V_4 \). Assume the VCDLs are identical and they have the same delay \( T_{\text{VCDL}} \). Similarly, the buffers have the same delay \( T_{\text{buf}} \). And the intrinsic delay of two divide-by-4 dividers is \( T_{\text{div}} \). For a special case, let us compare the phases of \( F_1 \) and \( P_2 \). Once the DLL is locked in the steady state, the phase error between two inputs of a PD should be zero. That is to say that the timing delay between \( F_1 \) and \( P_2 \) should be equal to the period \( T_{\text{CK}} \) of the input clock in Fig. 2. The delay between the rising edges of \( F_1 \) and \( P_2 \) is calculated as

\[
T_{P_2-F_1} = T_{\text{VCDL}} + T_{\text{edge}} + T_{\text{buf}} + T_{\text{div}} = T_{\text{CK}} \tag{1}
\]

where the delay of the edge combiner is \( T_{\text{edge}} \). The total delay through \( CK_{\text{in}} \), \( P_1 \), VCDL, the edge combiner, the buffer, and \( CK_{\text{out}} \) can be calculated as

\[
T_{\text{Total}} = T_{\text{buf}} + T_{\text{div}} + T_{\text{VCDL}} + T_{\text{edge}} + T_{\text{buf}}. \tag{2}
\]

Compared with (1) and (2), the total delay between \( CK_{\text{in}} \) and \( CK_{\text{out}} \) is equal to \( T_{\text{CK}} \).

In general, let us compare the phases between \( F_i \) and \( P_j \) (\( i, j \) \( N \)), and \( j \neq i \). Once the DLL is locked, the total delay between \( CK_{\text{in}} \) and \( CK_{\text{out}} \) can be expressed as

\[
T_{\text{Total}} = (j-i)T_{\text{CK}}, \quad j \neq i \tag{3}
\]

or

\[
T_{\text{Total}} = jT_{\text{CK}}, \quad j = i. \tag{4}
\]

From (3), the total delay between \( CK_{\text{in}} \) and \( CK_{\text{out}} \) can be chosen as \( kT_{\text{CK}} \) where \( k \) is an integer and \( 1 \leq kN \leq 1 \). However, it is usual to select \( k = 1 \) for most applications.

In a conventional DLL, only one PD and one CP are used to control the VCDL. For our DLL, if all the VCDLs are controlled only from a PD and a CP, the phase error will be updated every \( NT_{\text{CK}} \). It is because the divide-by-\( N \) dividers are adopted. It means the jitter will be accumulated for \( N \) cycles. Moreover, the multiple VCDLs may have the mismatches. Both of them will worsen the cycle jitter. To improve the cycle jitter, a calibration method is adopted. To compare the cycle jitter before and after calibration, the proposed PDs and CPs are shown in Fig. 3. When the selection signal for eight 2-to-1 multiplexers is low, the phases between \( F_1 \) and \( P_2 \) are compared. The resulting controlled voltage \( VC_1 = VC_2 = VC_3 = VC_4 \) is used to adjust the VCDLs. It is similar to the conventional DLL. When the selection signal is high for all the multiplexers, the proposed calibration method is active. The phases for \( P_2 - F_1, P_3 - F_2, P_4 - F_3, \) and \( P_1 - F_4 \) are compared to generate the controlled voltage \( VC_1, VC_2, VC_3, \) and \( VC_4 \), respectively. The controlled voltages are used to adjust the corresponding VCDLs, respectively, as shown in Fig. 2. Once the DLL is locked, \( P_2, P_3, P_4, \) and \( P_1 \) lock with \( F_1, F_2, F_3, \) and \( F_4 \), respectively. For the output of every PD in Fig. 3, the transmission gate is used to match the delay of an inverter. In the proposed DLL, the speed requirement for PDs, CPs, and VCDLs is relaxed. So, the conventional PDs and CPs can work in the proposed DLL, even though the operation frequency is very high. Moreover, each VCDL is adjusted by an independent loop, so the mismatch among VCDLs is not important. Each VCDL is adjusted once within \( NT_{\text{CK}} \); however, there are \( N \) parallel loops. It is equivalent to adjust this DLL every \( T_{\text{CK}} \). Thus, compared with the conventional method, the jitter accumulation is improved by the proposed calibration method. Since each calibration loop works independently, it is also a first-order system as the conventional one. Thus, the proposed DLL is stable.

For a conventional PD, the ideal detection range for an input clock is \( \pm 2\pi \) or \( \pm T_{\text{CK}} \). However, the PD [4] with the finite reset path delay \( \theta \) is used to improve the dead zone problem. Fig. 4(a) shows the detection ranges of a conventional PD with and without the finite reset path delay. When the frequency of the input clock increases, the detection range is decreased. Once
Fig. 4. (a) Detection range of a PD without a divide-by-N divider. (b) Detection range of a PD with a divide-by-N divider.

Fig. 5. Forward-path divide-by-4 divider.

The intrinsic delay of a VCDL is larger than the detection range of a conventional PD, the false or harmonic locking issue occurs. For example, when the input clock of 8 GHz is applied to the conventional PD, the input period is 125 ps. In our 90-nm process, the reset path delay is around 100 ps. It is difficult to realize a PD to work at such high speed. In our proposed DLL, two divide-by-4 dividers are inserted in front of the PD, the detection range of the proposed PD is shown in Fig. 4(b). For input clock of 8 GHz and the finite reset path delay of 100 ps, the detection range of the proposed PD is ±400 ps. So, for the PD in this proposed DLL, its detection range is enhanced and the speed requirement is relaxed. The remaining circuits for this proposed DLL will be discussed as follows.

A. Forward-Path Divide-by-4 Divider

To generate the precise multiphase outputs, the forward-path divider-by-4 divider is shown in Fig. 5. It consists of ten D flip-flops (DFFs) and two AND gates. The loading of the outputs $P_1$--$P_4$ is matched by inserting the dummy devices. Fig. 6 shows its timing diagram. The signal Vst is used to enable the divide-by-4 divider. When Vst is high, the clock Vin passes through the DFF1 and an AND gate to enable Vin1. After two periods of Vin, DFF7 and DFF8 sequentially generate the divide-by-4 quadrature outputs $P_1$ and $P_2$, respectively. And, DFF2--4 and an AND gate enable Vin2. Similarly, after two periods of Vin2, DFF9 and DFF10 generate another divide-by-4 quadrature outputs $P_3$ and $P_4$, respectively. DFF5 and DFF6 are used to match the loading. The proposed divide-by-4 divider operates with only a single-ended clock. The feedback-path divide-by-4 divider is similar to Fig. 5. $T_{CK}$ in the proposed DLL.

B. Voltage-Controlled Delay Line

Fig. 7 shows the VCDL in this paper. It is composed of six inverters, and the p-type MOS (PMOS) varactors are used to adjust the delay. Although the speed requirement of the VCDL is relaxed, the variable delay range of each VCDL has to be larger than

C. Edge Combiner

Fig. 8(a) shows the edge combined cell (ECC) and its timing diagram. Each ECC [6] consists of three NAND gates and two voltage-controlled delay cells. The voltage-controlled delay cell...
is similar to the VCDL in Fig. 7. The timing diagram of an ECC is also given in Fig. 8(a). Two complementary square waves A and B are applied to the ECC. The first NAND gate combines the square wave A and its inverse delayed one to realize a short pulse. Its pulse width is determined by the voltage-controlled delay cell. The complementary square wave B and its inverse delayed one are combined similarly by the second NAND gate. The third NAND gate combines two pulses to generate the multiplying output pulse. The output pulse has the double frequency of the square wave A. The edge combiner is shown in Fig. 8(b). It is composed of 3 ECCs, a voltage-to-current converter, a buffer, and a capacitor. It is equivalent to multiply the frequency of the input square wave by 4. However, the output duty cycle of the ECC may not be 50%. The voltage-to-current converter generates a controlled voltage $V_{\text{duty}}$ to adjust the voltage-controlled delay cell in an ECC. It is expected to achieve the duty cycle of 50% for the output clock.

D. Voltage-to-Current Converter

Fig. 9 shows the voltage-to-current converter. In the differential pair M3 and M7, when $CK_{\text{out}}$ is high and $\overline{CK}_{\text{out}}$ is low, M7 conducts and the current discharges the capacitor $C_{V/2}$. When $CK_{\text{out}}$ is low and $\overline{CK}_{\text{out}}$ is high, M3 conducts and the current charges the capacitor $C_{V/2}$. The duty cycle of the output clocks $CK_{\text{out}}$ and $\overline{CK}_{\text{out}}$ is converted into an analog voltage $V_{\text{duty}}$ to adjust the voltage-controlled delay cell in an ECC. When the duty cycle of $CK_{\text{out}}$ and $\overline{CK}_{\text{out}}$ is equal, the loop will be stable and the output duty cycle is 50%.

III. EXPERIMENTAL RESULTS

The proposed DLL has been fabricated in 90-nm CMOS process. Fig. 10 shows the die photograph. The core area of the proposed MDLL is $320 \times 300 \mu m^2$. The supply voltage is 1.2 V, and the total power consumption with buffers are 12 mW at 3 GHz and 18 mW at 8 GHz, respectively. When the DLL is locked without calibration, Fig. 11 shows the measured root mean square and peak-to-peak jitters are 2.18 and 17.78 ps, respectively, at 3 GHz. With the calibration, Fig. 12 shows the measured root mean square and peak-to-peak jitters are 1.56 and 12.89 ps, respectively, at 3 GHz. Fig. 13 shows the measured input and output clocks, when the DLL is locked at 3 GHz with calibration.
Fig. 14 shows that the measured root mean square and peak-to-peak jitters are 1.37 and 11.44 ps, respectively, at 8 GHz without calibration. Fig. 15 shows the measured root mean square and peak-to-peak jitters are 0.87 and 6.67 ps, respectively, at 8 GHz with calibration. Fig. 16 shows the measured input and output clocks at 8 GHz with calibration. Fig. 17 shows the measured output clock’s jitters at different frequencies. The measured output duty cycle is around 50% with the error less than 3%.

Compared with the previous DLLs, this paper achieves the high speed and low jitter performance. The performance summary and comparison results are shown in Table I.

### IV. Conclusion

The proposed DLL with cycle jitter calibration has been fabricated in 90-nm CMOS process. The experimental results show that the proposed calibration improves the output clock’s jitter.

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### REFERENCES


