81.5–85.9 GHz injection-locked frequency divider in 65 nm CMOS

L.-C. Cho, K.-H. Tsai, C.-C. Hung and S.-I. Liu

An injection-locked frequency divider (ILFD) using the shunt-series inductive peaking technique is proposed. Fabricated in a 65 nm process, the proposed ILFD and a conventional one have the measured locking range of 81.5–85.9 and 71–77.4 GHz, respectively. Compared with the conventional ILFD, the measured free-running frequency of the proposed one is increased by 12.5%. Both ILFDs have core area of 0.036 mm² and power of 12 mW for a 1.55 V supply without buffers.

Introduction: Frequency dividers are widely used in frequency synthesizers and phase-locked loops. The injection-locked frequency divider (ILFD) [1–4] is attractive because of high operation frequency and low power consumption. The conventional ILFD is realised by an LC-tank oscillator with an injection input [1]. To maximise the operation frequency of an ILFD, the shunt-series inductive peaking technique [5] is adopted in the proposed ILFD. The conventional ILFD and the proposed one are realised in a 65 nm CMOS process by using the same active and passive devices with the same power and area. Experimental results demonstrate that the measured free-running frequency of the proposed ILFD is increased by 12.5%.

Fig. 1 Proposed ILFD and equivalent circuit

a Proposed ILFD
b Equivalent circuit

Circuit description: For a conventional ILFD [1], it is composed of an LC-tank oscillator and an injection transistor. Its output frequency is given as $1/\sqrt{LC}$ where L is the inductor and C is the total equivalent capacitance of the LC tank. To have a higher output frequency, the proposed ILFD is as shown in Fig. 1a. The inductors are split and the cross-coupled pair is appropriately reconnected. It is similar to the shunt-series inductive peaking technique in [5]. To analyse the locking range of the proposed ILFD, its differential equivalent circuit is as shown in Fig. 1b where C_1 is the total grounded capacitance at the nodes V_+ and V_- and C_2 is the total grounded capacitance at the nodes $V_{g,M4}$ and $V_{g,M5}$. The shunt inductors L_2 and the series inductors L_1 realise the shunt-series inductive peaking technique [5]. Similar to [6], when the ILFD is locked, the injection current I_{in} is decomposed into the in-phase and quadrature components as

$$I_{in} = I_i(\phi) \cos(\omega t + \phi) + I_q(\phi) \sin(\omega t + \phi) \quad (1)$$

Let the drain and source voltages of the injection transistor M_3 be defined as

$$V_+ = v_i \cos(\omega t + \phi) \quad \text{and} \quad V_- = -v_i \cos(\omega t + \phi) \quad (2)$$

The input impedance in Fig. 1b is expressed as

$$Z_{in}(S) = \frac{2sL_2 \left(\frac{2sL_1}{Z_{eq}} + 1 \right) + 2s^3 L_1 L_2 C_1}{S^4 L_1 L_2 C_1 C_2 + \frac{2s^3 L_1 L_2 C_2}{Z_{eq}} + s^2 (L_2 C_2 + L_1 C_1 + L_2 C_1) + \frac{2s(L_1 + L_2)}{Z_{eq}} + 1} \quad (3)$$

where Z_{eq} is the impedance of the injection transistor M_3 . To simplify the analysis, assume $L_1 = L_2 = L/2$, $C_1 = C/2$ and $C_2 = C/2$. Neglecting the injection transistor M_3 (i.e. Z_{eq} is infinity), the output resonant frequency of the proposed ILFD is calculated as

$$\omega_o = \sqrt{\frac{6 - 2\sqrt{5}}{LC}} \quad (4)$$

Compared with the conventional ILFD [1], the output resonant frequency of the proposed one is increased by 23.6%. Once the input frequency for the injection transistor M_3 varies, the in-phase and quadrature components of the injection current I_{in} will change. Based on (3) and assuming that Z_{eq} is modelled as an equivalent inductor, $L_{eq} = 2v_i/\omega I_q(\phi)$, the output frequency of the ILFD is increased. This is because this equivalent inductor is in parallel with the LC resonator and the total equivalent inductance is decreased and the resonant frequency is increased. Note that if the output frequency of the ILFD, ω , is close to ω_o and $\omega_o \gg I_q(\phi)/Cv_i$, the output frequency of the proposed ILFD is calculated as

$$\omega \simeq \omega_o + \frac{I_q(\phi)}{2Cv_o} \quad (5)$$

Let the maximum value of $I_q(\phi)/2v_o$ be denoted by g_{q,M_3} , the equivalent quadrature conductance of M_3 . The maximum available frequency of the ILFD is given as

$$\omega_{max} \simeq \omega_o + \frac{g_{q,M_3}}{C} \quad (6)$$

Similarly, assuming Z_{eq} is modelled as an equivalent capacitor $C_{eq} = I_q(\phi)/2v_i\omega$, the output frequency of the proposed ILFD is decreased and the minimum available frequency is

$$\omega_{min} \simeq \omega_o - \frac{g_{q,M_3}}{C} \quad (7)$$

Therefore, the input locking range denoted by $\Delta\omega_{in}$ is estimated as

$$\Delta\omega_{in} = 2(\omega_{max} - \omega_{min}) = \frac{4g_{q,M_3}}{C} \quad (8)$$

From (4) and (8), this ILFD improves the output frequency and locking range.

Experimental results: The proposed ILFD and the conventional one have been fabricated in 65 nm CMOS process. Fig. 2 shows the die photos. These two ILFDs have the same active devices and inductors. So they have the same area and power consumption. Each ILFD has the core area of 0.036 mm² without pads and the power of 12 mW from 1.55 V supply without including the output buffer and bias circuits. Fig. 3 shows the measured input sensitivity curves of the conventional and proposed ILFDs. The locking range of the conventional ILFD is from 71 to 77.4 GHz with $V_{bias} = 0.8$ V. The locking range of the proposed ILFD is from 81.5 to 85.9 GHz with $V_{bias} = 0.8$ V. Compared with the conventional ILFD, the measured free-running frequency of the proposed one is increased by 12.5%. Fig. 4 shows the measured output waveform of the proposed ILFD, where the input frequency is 85.2 GHz and $V_{bias} = 0.8$ V. In Fig. 4, the measured rms jitter and peak-to-peak jitter of the output signal are 0.46 and 3.46 ps, respectively. For input frequency of 85.9 GHz, the measured phase noise is –88.5 dBc/Hz at 500 kHz offset frequency. Table 1 summarises the performance of the frequency divider compared with the previous works.

Fig. 2 Die photo of conventional and proposed ILFDs

Fig. 3 Measured input sensitivity curves for conventional and proposed ILFDs

Fig. 4 Measured waveform and jitter at input frequency of 85.2 GHz

Table 1: Summary and comparison

Parameter	[1]	[2]	[3]	[4]	[6]	Conven. ILFD	Our ILFD
Technology	0.13 μ m CMOS	65 nm CMOS	90 nm CMOS	65 nm CMOS	0.13 μ m CMOS	65 nm CMOS	65 nm CMOS
Centre frequency	50.35 GHz	88 GHz	102 GHz	101.3 GHz	71.2 GHz	76 GHz	85.5 GHz
Divider range (GHz)	50.31–50.39*	82–94	99–105	93.5–109.1	66.4–76	71–77.4	81.5–85.9
Locking range (GHz)	0.08 (0.1%)	12 (13.6%)	6 (5.8%)	15.6 (15.3%)	9.6 (13.6%)	6.4 (8.4%)	4.4 (5.1%)
Supply (V)	1.5	0.56	1.2	1.1	1	1.55	1.55
Power (mW)	3	3.92	3.3	5.5	4.4	12	12
FOM** (GHz/mW)	0.026	3.06	1.82	2.84	2.18	0.53	0.37
Area (mm ²)	0.49 $\times$ 0.47	1.15 $\times$ 0.85	0.66 $\times$ 0.51	0.2 $\times$ 0.18***	None	0.2 $\times$ 0.18***	0.2 $\times$ 0.18***

*Input power 15 dBm; **FOM = locking range/power; ***core circuit only

Conclusion: A shunt-series peaking ILFD and a conventional one have been fabricated in a 65 nm CMOS technology. The equivalent circuit of the proposed ILFD is given and the analysis results are presented. Compared with the conventional ILFD, the measured free-running frequency of the proposed one is increased by 12.5%. Both the analysis and the experimental results are given to demonstrate the proposed circuit.

Acknowledgment: The authors thank UMC Inc. and Media-Tek Inc. for chip fabrication and NSC for support.

© The Institution of Engineering and Technology 2008

22 May 2008

Electronics Letters online no: 20081426

doi: 10.1049/el:20081426

L.-C. Cho, K.-H. Tsai, C.-C. Hung and S.-I. Liu (Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan, Republic of China)

E-mail: lsi@cc.ee.ntu.edu.tw

References

- Tiebout, M.: 'A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider', *IEEE J. Solid-State Circuits*, 2000, **39**, pp. 1170–1174
- Mayr, P., Weyers, C., and Langmann, U.: 'A 90 GHz 65 nm CMOS injection-locked frequency divider'. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Pprs, San Francisco, CA, USA, February 2007, pp. 198–199
- Tsai, K.H., Cho, L.C., Wu, J.H., and Liu, S.I.: '3.5 mW W-band frequency divider with wide locking range in 90 nm CMOS Technology'. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Pprs, San Francisco, CA, USA, February 2008, pp. 466–467
- Cho, L.C., Tsai, K.H., Hung, C.C., and Liu, S.I.: '93.5–109.4 GHz CMOS injection-locked frequency divider with 15.3% locking range'. Symp. on VLSI Circuits, June 2008, pp. 86–87
- Galal, S., and Razavi, B.: '40 Gb/s amplifier and ESD protection circuit in 0.18 μ m CMOS technology', *IEEE J. Solid-State Circuits*, 2004, **39**, pp. 2389–2396
- Wu, C.Y., and Yu, C.Y.: 'Design and analysis of a millimeter-wave direct injection-locked frequency divider with large frequency locking range', *IEEE Trans. Microw. Theory Tech.*, 2007, **55**, pp. 1649–1658