40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS

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Abstract—High-speed front-end amplifiers and CDR circuits play critical roles in broadband data receivers as the former needs to perform amplification at high data rate and the latter has to retime the data with the extracted low-jitter clock. In this paper, the design and experimental results of 40 Gb/s transimpedance-AGC amplifier and CDR circuit are described. The transimpedance amplifier incorporates reversed triple-resonance networks (RTRNs) and negative feedback in a common-gate configuration. A mathematical model is derived to facilitate the design and analysis of the RTRN, showing that the bandwidth is extended by a larger factor compared to using the shunt-series peaking technique, especially in cases when the parasitic capacitance is dominated by the next stage. Operating at 40 Gb/s, the amplifier provides an overall gain of $2\text{ k}\Omega$ and a differential output swing of 520mV_{pp} with $\text{BER} < 10^{-9}$ for input spanning from $430\mu\text{A}_{\text{pp}}$ to 4mA_{pp} . The measured integrated input-referred noise is $3.3\mu\text{A}_{\text{rms}}$. The half-rate CDR circuit employs a direction-determined rotary-wave quadrature VCO to solve the bidirectional-rotation problem in conventional rotary-wave oscillators. This guarantees the phase sequence while negligibly affecting the phase noise. With 40 Gb/s $2^{31} - 1$ PRBS input, the recovered clock jitter is $0.7\text{ps}_{\text{rms}}$ and 5.6ps_{pp} . The retimed data exhibits $13.3\text{ps}_{\text{pp}}$ jitter with $\text{BER} < 10^{-9}$. Fabricated in 90 nm digital CMOS technology, the overall amplifier consumes 75 mW and the CDR circuit consumes 48 mW excluding the output buffers, all from a 1.2 V supply.

Index Terms—Automatic gain controlled (AGC), clock/data recovery (CDR), receiver, rotary-wave oscillator, transimpedance amplifier.

I. INTRODUCTION

WITH the rapid growth of numerous multimedia applications in Internet, high-speed transceivers operating at tens of gigabits per second are required to fulfill the data transfer volume. The typical architecture of a 40 Gb/s receiver is shown in Fig. 1, which consists of a front-end amplifier and a CDR circuit. The front-end amplifier must enhance the weak input signals to several hundreds of millivolts for the subsequent clock and data recovery. The CDR circuit should extract the clock from the jittery incoming data while automatically retiming and de-multiplexing the data into lower-speed streams. Prior published 40 Gb/s amplifiers are either implemented in InP or SiGe

technologies [1]–[4], or in CMOS but with limited gains [5]–[9]. On the other hand, existing 40 Gb/s CDRs either consume a significant amount of power or only provide moderate performance with respect to the recovered clock jitter [10]–[12].

In this paper, the design and experimental results of 40 Gb/s transimpedance-AGC (TI-AGC) amplifier and CDR circuit implemented in 90 nm digital CMOS are presented. The amplifier utilizes shunt feedback around a common-gate input stage to lower its input resistance while incorporating reversed triple-resonance networks at the interfaces between stages to extend the bandwidth [13]. The CDR circuit employs a direction-determined rotary-wave quadrature VCO (QVCO) to recover the clock with low jitter while consuming only 48 mW within a small die area. The paper is organized as follows. Section II introduces the architecture of the TI-AGC amplifier and that of the CDR circuit. Section III and Section IV describes the circuit techniques involved in the design of the amplifier and the CDR circuit, respectively. The experimental results are presented in Section V. Finally, Section VI draws the conclusion.

II. ARCHITECTURE

A. Transimpedance-AGC (TI-AGC) Amplifier

The architecture of the TI-AGC amplifier is shown in Fig. 2. The first stage is a transimpedance amplifier (TIA) with an input resistance close to $50\ \Omega$. At such high data rate, the TIA should provide enough gain and moderate noise performance since many low-gain (and hence high-noise) stages are cascaded behind it to achieve a reasonable overall gain. This consideration prohibits the use of a single resistor (ex: $50\ \Omega$) connected at the input to ground, suggesting other lower-noise input stages such as common-gate or feedback topologies. Following the TIA, an AGC loop is used to keep the intermediate stages linear, reducing jitter and pulse-width distortion at high input currents [14]. The output buffer should drive the $50\ \Omega$ on-chip terminations and off-chip loads, mandating three stages tapered in size to avoid heavily loading the core. To ensure that the CML buffer completely switches at high speed, the signal swing entering the buffer is maintained as 400mV_{pp} per side by the AGC loop. The output buffer thus behaves as a soft limiter and provides an output swing of 260mV_{pp} per side on the $25\ \Omega$ equivalent loads.

B. CDR Circuit

The CDR circuit is based on the half-rate architecture shown in Fig. 3. This architecture is chosen to avoid using inductors in the D flip-flops (DFFs), which not only saves the area but also

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Fig. 1. Typical architecture of a 40 Gb/s receiver.

Fig. 2. Architecture of the transimpedance-AGC amplifier.

Fig. 3. Architecture of the CDR circuit.

makes the signal routing much easier. Though the quarter-rate architecture can further relax the speed of the flip-flops and the oscillator, the required number of sampling latches and clock phases become doubled, potentially increasing the power consumption and routing imbalance. The half-rate architecture is therefore chosen as a compromise between the speed of flip-flops, the number of clock phases, and the power consumption. The QVCO samples the incoming data every 12.5 ps through the phase detector (PD), which takes every 3 consecutive samples to generate the early or late information and then injects current to the loop filter accordingly. Using the half-rate clock to sample the data also performs 1:2 de-multiplexing, and one

of the output data streams is taken out of chip to examine the quality of the recovered data. Note that the PD employs only one rank of DFFs in order to relax the loading on the clock buffers. It causes the outputs of the XOR gates to be staggered, leading to some ripples on the control line. However, by choosing a small resistor ($\sim 30 \Omega$) in the loop filter, such effect on the clock jitter can be minimized.

III. AMPLIFIER CIRCUIT DESIGN

A. Transimpedance Amplifier (TIA)

1) *Common-Gate (CG) TIA With Feedback*: The trade-offs between input resistance, noise, and voltage headroom pose challenges in the design of high-speed TIAs. Considering the common-gate (CG) TIA depicted in Fig. 4(a), at low frequencies its input resistance, transimpedance gain and input-referred noise can be derived as the following equations:

$$Z_{in} = g_{m1}^{-1} \quad (1)$$

$$Z_T = A_2 R_{L1} \quad (2)$$

$$\overline{I}_{n,in}^2 = \frac{4kT}{R_{L1}} + \overline{I}_{n,ISS}^2 + \frac{\overline{V}_{n,A2}^2}{R_{L1}^2} \quad (3)$$

where $\overline{I}_{n,ISS}^2$ and $\overline{V}_{n,A2}^2$ denote the noise from the tail current source (I_{SS}) and the following stage (A_2), respectively. To obtain a low input resistance, the bias current should be large to maximize g_{m1} , since the size of M_1 should be kept small to reduce its input and output capacitance. According to (3), this not only raises the input-referred noise from the tail current source (I_{SS}) but also results in a small R_{L1} due to the headroom limitation, which in turn worsens the noise from the following stage (A_2).

To alleviate the above issues to some extent, the common-gate topology is modified by applying a feedback resistor connected to M_1 's source, as shown in Fig. 4(b). Intuitively, the input resistance will be lower, but the noise will become worse if the core design is not changed, since an additional noisy component is added. Due to this consideration, the load resistor is raised by m times and the bias current is decreased by the same factor accordingly. The size of M_1 is adjusted so that g_{m1} becomes m times smaller.¹ To design the circuit, the input resistance, transimpedance gain and input-referred noise at low frequencies are

¹The device size will need to be decreased by m times if the square law is assumed.

Fig. 4. (a) Conventional CG TIA. (b) Proposed CG TIA with feedback.

derived as

$$Z_{in} = \left[\frac{g_{m1}}{m} + \frac{1}{R_F} (1 + g_{m1} R_{L1} A_2) \right]^{-1} \quad (4)$$

$$Z_T = \left(\frac{R_F}{1 + 1/g_{m1} R_{L1} A_2} \right) \parallel (m A_2 R_{L1}) \quad (5)$$

$$\begin{aligned} \overline{I}_{n,in}^2 &= \frac{4kT}{R_F} \left(1 + \frac{\gamma}{g_{m1} R_F / m} \right) + \overline{I}_{n,ISS/m}^2 \\ &+ \left(\frac{4kT}{m R_{L1}} + \frac{\overline{V}_{n,A2}^2}{m^2 R_{L1}^2} \right) \left(1 + \frac{1}{g_{m1} R_F / m} \right)^2 \\ &\approx \frac{4kT}{R_F} + \overline{I}_{n,ISS/m}^2 + \frac{4kT}{m R_{L1}} + \frac{\overline{V}_{n,A2}^2}{m^2 R_{L1}^2} \end{aligned} \quad (6)$$

where $g_{m1} R_F / m \gg 1$ is assumed and will be validated later. To make the noise performance not worse than that of a common-gate TIA, the sum of the noise from $m R_{L1}$ and R_F ((6)) is made equal to that from R_{L1} ((3)), which results in

$$R_F \geq m R_{L1} / (m - 1) \quad (7)$$

Substituting (7) to (4), the design objective is to find the required A_2 that makes Z_{in} smaller than $1/g_{m1}$, which is the input resistance of the common-gate TIA. The result is shown below:

$$\begin{aligned} &\left[\frac{g_{m1}}{m} + \frac{1}{R_F} (1 + g_{m1} R_{L1} A_2) \right]^{-1} \\ &< \left[\frac{g_{m1}}{m} + \left(\frac{m-1}{m R_{L1}} \right) g_{m1} R_{L1} A_2 \right]^{-1} \\ &\leq g_{m1}^{-1} \Rightarrow A_2 \geq 1. \end{aligned} \quad (8)$$

The condition of unity gain is not difficult to meet even at such high data rate. With $A_2 > 1$, the input resistance and power consumption of the CG TIA with feedback are both lower than those of the conventional CG TIA. The noise from the tail current source and the following stage (A_2) also decreases in the

case with feedback, which can be observed by comparing (6) with (3). In the final design, we choose $m = 1.5$ and $A_2 = 6.7$ dB, which results in 32% decrease in input resistance and 33% reduction in power, compared to the CG TIA. Note that $g_{m1} = 22.5$ mS and $R_{L1} = 200 \Omega$ in this particular design, resulting in $g_{m1} R_F / m = 9 \gg 1$ and validating the previous assumption. The sufficiently large $g_{m1} R_F / m$ also guarantees that the noise contributed by M_1 will only slightly increase in the case with feedback, so that the overall noise performance will not be worse than that of the conventional CG TIA.

The above design parameters yield an input resistance of 30Ω and a transimpedance gain of 296Ω for the feedback TIA. The gain is lower compared to the non-feedback TIA. However, for the non-feedback TIA to achieve the same input resistance (30Ω), a high bias current and a small R_{L1} are essential, which reduces the gain by nearly the same factor and significantly sacrifices the input-referred noise. In order to obtain a higher bandwidth at the input node, the input resistance is intentionally designed to be smaller than 50Ω . The input reflection coefficient, Γ_{in} , equals to -12 dB and is still reasonable. Besides, considering that the values of g_{m1} and A_2 in the fabricated chip may be smaller than those predicted by the model, it is recommended to make the input resistance lower in the simulation process. In applications where an exactly 50Ω input resistance is required, R_F can be increased to ~ 2 k Ω for better matching and improved gain and noise performance.

The actual implementation of the TIA is shown in Fig. 5. A differential topology is chosen to allow an easier biasing scheme and to make the circuit more immune to bond wire inductance on the supply pads. Source followers are inserted between the feedback resistors and the second stage, avoiding the former to load the latter. To take the advantages of feedback, the loop gain must be maintained up to high frequencies, necessitating some broadband techniques. In [5], the shunt-series peaking technique increases the bandwidth by a factor of 3.5 when the parasitic capacitance is assumed to be evenly distributed between the present and the next stage. However, as shown in the subsequent text, the bandwidth extension becomes less effective when the capacitance caused by the next stage is increasingly larger than that by the present stage, even though the total capacitance remains unchanged. To extend the bandwidth more efficiently, we simply *interchange* the input and output ports of the network formed by $L_1 - R_1 - L_2$ in [5], resulting in the inductive series-shunt peaking configuration in Fig. 5. For the reasons described in the following, it is called the reversed triple-resonance network (RTRN).

2) Reversed Triple-Resonance Network (RTRN): The equivalent model of the RTRN will now be derived to facilitate the design. The parasitic capacitance is assumed to be unevenly distributed, with $C(1 - \alpha)/2$ on the present stage and $C(1 + \alpha)/2$ on the next. Since the sum of C_{GS} and Miller capacitance is usually larger than the drain-bulk junction capacitance, we tacitly assume α greater than zero in the following analysis. The network is 4th-order and simply writing the transfer function will not give us any insight about it. To simplify the circuit, the left-side of the dotted line in Fig. 6(a) is converted to its Norton equivalent circuit as shown in Fig. 6(b). Since the network now contains only paralleled branches, V_{out} can be calculated more

Fig. 5. Circuit implementation of the transimpedance amplifier.

easily. After some manipulation, the overall network can be further simplified to Fig. 6(c), where the equivalent impedance, Z_{tot} , is expressed as

$$Z_{tot}(j\omega) = (R_{eq} + j\omega L_{eq}) \parallel \frac{1}{j\omega C_{eq}} \\ = \left[\frac{R_1}{1 - \omega^2 L_2 \frac{C}{2}(1 - \alpha)} + j\omega \frac{L_1}{1 - \omega^2 L_2 \frac{C}{2}(1 - \alpha)} \right] \\ \parallel \left[\frac{1}{j\omega C} \frac{1}{1 - \omega^2 L_2 \frac{C}{4}(1 - \alpha^2)} \right]. \quad (9)$$

From (9), there are three resonance frequencies observed. The first one can be seen in the first two terms of Z_{tot} and the second one can be found in the third term. The third resonance frequency is the one that makes Z_{tot} purely real ($\text{Im}\{Z_{tot}\} = 0$). Due to this triple-resonance behavior and the fact that the network is the horizontally-flipped version of the shunt-series peaking topology, it is called the reversed triple-resonance network (RTRN).

The above analysis helps us design the frequency response of the RTRN. At

$$\omega_1 = 1/\sqrt{L_2 C(1 - \alpha)/2} \quad (10)$$

the impedance of the $R_{eq} - L_{eq}$ branch becomes infinity, so the network becomes a single capacitor C_{eq} at this frequency [Fig. 7(a)]. To design the frequency response, the location of ω_1 and the gain at this frequency should be determined. Without the loss of generality, ω_1 is chosen equal to the resonance frequency of a simply shunt-peaked amplifier

$$\omega_1 = 1/\sqrt{L_1 C} \quad (11)$$

and the gain at ω_1 is designed equal to R_1

$$|Z_{tot}(j\omega_1)| = R_1 \quad (12)$$

which is the same as the low-frequency gain [5]. According to these design criteria, the inductance can be found as

$$L_1 = (1 - \alpha)^2 C R_1^2 / 4 \quad (13)$$

$$L_2 = (1 - \alpha) C R_1^2 / 2 \quad (14)$$

which are then used to subsequently plot the overall frequency response. At

$$\omega_2 = 1/\sqrt{L_2 C(1 - \alpha^2)/4} \quad (15)$$

the impedance of the capacitor C_{eq} becomes infinity, leaving only the $R_{eq} - L_{eq}$ branch [Fig. 7(b)]. Substituting the previously obtained inductance gives us

$$|Z_{tot}(j\omega_2)| = \frac{1}{1 - (\omega_2/\omega_1)^2} \sqrt{R_1^2 + \omega_2^2 L_1^2} \\ = \sqrt{\frac{(1 + \alpha)(3 + \alpha^2)}{2}} \left(\frac{R_1}{1 - \alpha} \right) \quad (16)$$

and

$$\omega_2 = \sqrt{\frac{2}{1 + \alpha}} \omega_1 = \frac{1}{(1 - \alpha)\sqrt{1 + \alpha}} \left(\frac{2\sqrt{2}}{C R_1} \right). \quad (17)$$

From (16), a peaking at ω_2 is observed. The amount of peaking is directly related to α , which represents the partition of the capacitance between the present and the next stage. At ω_3 , which is defined as the frequency that makes Z_{tot} purely real, the gain can be found by solving

$$\text{Im}\{Z_{tot}(j\omega_3)\} = 0. \quad (18)$$

Fig. 6. (a) Model of the RTRN. (b) Simplified version of (a). (c) Final equivalent circuit of (a) used for analysis and design.

Fig. 7. Equivalent Z_{tot} when resonance occurs at (a) ω_1 and (b) ω_2 .

The result is given by

$$|Z_{tot}(j\omega_3)| = |\operatorname{Re}\{Z_{tot}(j\omega_3)\}|$$

$$= \left| \frac{1 + (\omega_3/\omega_1)^2(1-\alpha)^2/4}{1 - (\omega_3/\omega_1)^2} \right| R_1 \quad (19)$$

Fig. 8. Model of the TRN.

where

$$\omega_3 = \frac{f(\alpha)}{(1-\alpha)^2} \frac{2\sqrt[4]{6}}{CR_1}$$

$$f(\alpha) = \sqrt[4]{1 - \frac{\alpha}{3}}$$

$$\times \sqrt{\frac{-\alpha\sqrt{6-2\alpha} + \sqrt{1+4\alpha^2-2\alpha^3+\alpha^4}}{1+\alpha}}. \quad (20)$$

The -3 dB bandwidth, ω_{3dB} , exceeds ω_3 and is quite a complicated function of α . Therefore, ω_{3dB} is only calculated in terms of some specified α . For example, by letting

$$|Z_{tot}(j\omega_{3dB})|^2 = \frac{R_1^2}{2} \quad (21)$$

$$\Rightarrow \omega_{3dB} \approx 3.9/CR_1 \text{ for } \alpha = 0.2. \quad (22)$$

Note that the gain may be lower than R_1 for frequencies below ω_1 , especially when α becomes large. This issue can be remedied by increasing L_1 beyond the theoretical value ((13)), which compensates the roll-off at low frequencies ($\omega < \omega_1$) while only sacrificing (increasing) the peaking at ω_2 .² The bandwidth is negligibly affected by increasing L_1 because the last term in (9) ($1/\omega C_{eq}$) becomes much smaller than the second term (ωL_{eq}) and hence dominates the equivalent impedance as the frequency approaches ω_{3dB} .

The methodology described above can also be applied to the triple-resonance network (TRN) [5] as well, which is the shunt-series peaking configuration depicted in Fig. 8. By following a similar procedure, the equivalent impedance of the TRN can be simplified to be of the same form as (9), except that α is replaced by $-\alpha$. In addition, based on the same design criteria: (11) and (12), the three resonance frequencies and the -3 dB bandwidth of the TRN can also be found. As expected, their expressions are similar to those in the RTRN, except that α is replaced by $-\alpha$. Fig. 9 and Fig. 10 plot the locations of ω_2 and ω_3 as well as the gain at these frequencies for these two kinds of peaking networks. As α increases, the RTRN exhibits higher gain at higher frequencies compared to the TRN, implicitly showing that it extends the bandwidth more efficiently, especially when the capacitance is dominated by the next stage. To explicitly confirm

²The locations of ω_1 and ω_2 as well as the gain at ω_1 will not change with L_1 as long as L_2 remains fixed. These can be observed in (10), (15), and the last term of (9), respectively.

Fig. 9. (a) ω_2 and (b) the gain at ω_2 for different α , obtained from eq. (17) and eq. (16), respectively.

Fig. 10. (a) ω_3 and (b) the gain at ω_3 for different α , obtained from eq. (20) and eq. (19), respectively.

Fig. 11. ω_{3dB} for different α , derived from eq. (21).

Fig. 12. Simulated frequency response of the TIA with the RTRN. A TIA with the TRN and a TIA without inductors are designed with the same gain and power dissipation for comparison.

the effectiveness of the RTRN, ω_{3dB} in both cases are derived and plotted in Fig. 11. A larger bandwidth extension is achieved by the RTRN, which is simply the reversed arrangement of the TRN and requires no additional inductors.

Since the amplifier is designed to process broadband random data, the large peaking in the frequency response of the RTRN should be carefully considered. Fortunately, the finite Q of

on-chip inductors causes the peaking to be much smaller than the theoretical value (which is obtained using ideal inductors). This allows L_1 and L_2 to be realized with narrow traces, which saves the area and makes the signal routing easier. In the final design, the width of L_1 and L_2 is $1.6 \mu\text{m}$, resulting in $Q \sim 8$ at 20 GHz. The simulated frequency response of the TIA with real inductors is shown in Fig. 12. The bandwidth is extended by 3.7 times compared to the case with no inductors, while the ripple or peaking is kept less than 0.5 dB.³ Without changing any other design except the inductors, a similar TIA using the TRN is also simulated for comparison. The RTRN outperforms the TRN by 42% in terms of the -3 dB bandwidth. To examine the time domain behaviors, the 40 Gb/s output eye diagrams for these two TIAs are plotted in Fig. 13(a) and (b), respectively. The eye exhibits less jitter and larger opening in the RTRN than in the TRN, while the gain and power consumption are equal in both cases.

3) *Input Capacitance Tolerance*: The TIA is nominally connected to a photodiode in an optical receiver. With $R_{in} = 50 \Omega$, the tolerable input capacitance for $f_{3dB} = 28$ GHz (considering the 40 Gb/s data rate) is given by

$$C_{in} = \frac{1}{2\pi f_{3dB} R_{in}} \leq 114 \text{ fF}. \quad (23)$$

In this design, with only 40 fF parasitic capacitance contributed by the active devices at the input, the tolerable photodiode capacitance is about 60–80 fF.⁴ Since photodiodes with capacitance as low as 60 fF have been reported [1], [2], the bandwidth

³A higher bandwidth can be obtained if a larger in-band peaking is acceptable, which however induces more jitter in the time domain.

⁴By applying series inductive peaking at the input, the tolerable capacitance in (23) can be increased by $\sim 40\%$ [15], resulting in a total capacitance up to 160 fF.

Fig. 13. Simulated 40 Gb/s single-ended output eyes with $200\mu\text{A}_{\text{pp}}$ input swing for (a) TIA with the RTRN and (b) TIA with the TRN.

Fig. 14. Variable gain amplifier.

of the TIA will *not* be dominated by the input pole as long as the input resistance is kept lower than $50\ \Omega$.

In this particular design, however, due to the lack of such low-capacitance photodiode, the circuit is actually tested using standard instrument. This means the input impedance should reasonably match to $50\ \Omega$, otherwise the input data will all reflect back instead of coming into the circuit under test. The input matching constraint, i.e., $\Gamma_{\text{in}} \leq -10\ \text{dB}$ at 40 GHz, pose a more stringent limit on the input capacitance:

$$C_{\text{in}} = \frac{1}{\pi f R_{\text{in}}} \sqrt{|\Gamma_{\text{in}}|^2 / (1 - |\Gamma_{\text{in}}|^2)} \leq 50\ \text{fF}. \quad (24)$$

Though inductive peaking can somewhat improve the matching, the tolerable capacitance is still limited by the matching constraint rather than by the bandwidth. Therefore, to satisfy the above requirement, the input capacitance (C_{in} in Fig. 5) in this design contains only the PAD capacitance and no other explicit capacitor is integrated to emulate the photodiode. However, according to the measured input impedance (average $\text{Re}\{Z_{\text{in}}\} \sim$

$51\ \Omega$) and the above discussion, the bandwidth of the TIA is still dominated by the *internal nodes* rather than by the input, provided that a photodiode with $<80\ \text{fF}$ capacitance is available.

B. AGC Amplifier

1) *Variable Gain Amplifier (VGA)*: The VGA should provide a reasonable gain-controlled range while maintaining constant bandwidth and output common mode during gain tuning. These requirements suggest a current-steering-based topology, ex: the Gilbert Cell. Fig. 14 shows the circuit schematic of the VGA. Modified from the Gilbert Cell, the gates of $M_{3,4}$ are connected to a fixed bias rather than to the input, reducing the loading on the previous stage. Since $M_{3,4}$ are used only for current steering, their size is 1/5 times that of $M_{1,2}$. This further lowers the capacitances at the output nodes, allowing the VGA to operate at high speed.

2) *Post Amplifier*: The two gain stages following the VGA are implemented as Cherry-Hooper amplifiers with active feedback [16]. The negative Miller capacitances are realized using vertical parallel-plate capacitors [17], which have lower bottom-plate capacitances compared to MOS varactors. To reduce the

Fig. 15. AGC circuit.

Fig. 16. 40 Gb/s output buffer.

area, all the shunt-peaking inductors are made by stacked spirals. The simulated bandwidth of the post amplifier is 24 GHz,⁵ which is much lower than that of the TIA and dominates the overall frequency response. However, since the signal swing entering the post amplifier is 5–6 times larger than that experienced by the TIA, the actual operation of the post amplifier is partially determined by the switching behavior, relaxing its bandwidth requirement by some extent.

3) *AGC Circuit*: The AGC circuit contains a power detector, a V/I converter, and an integrating capacitor, as shown in Fig. 15. The reference voltage of the AGC loop is generated internally by utilizing the common mode of the data and providing the required level shift ($I_{SS}R_{REF}$).

C. Output Buffer

The circuit of the output buffer is depicted in Fig. 16. It consists of 3 stages tapered in size and tail current to deliver large output swings on the 25 Ω equivalent loads while not heavily loading the core. The size of $M_{5,6}$ is very large, so the RTRN is used again to extend the bandwidth. Since α is quite large in

⁵Using series-shunt peaking in the post amplifier will considerably improve the bandwidth at the cost of much larger area.

this case, the resultant inductor L_1 is small and can be put inside L_2 to further reduce the area. Simulation indicates that the output current can fully switch between on and off provided that the signal swing entering the buffer is larger than 400mV_{pp} per side. Actually, this determines the swing to which the AGC loop locks.

IV. CDR CIRCUIT DESIGN

A. Quadrature VCO (QVCO)

The half-rate CDR architecture inevitably requires a QVCO producing accurate clock phases. In addition, the high-frequency operation and low-jitter requirement suggest an *LC* realization. Existing *LC* QVCOs suffer from several design issues with respect to the phase noise and phase accuracy. Coupled *LC* oscillators must rely on a sufficiently large coupling factor to maintain the phase accuracy, which forces the circuit to operate away from the tank resonance frequency [18], [19]. The *LC* ring oscillator in [20] uses resistor-loaded differential pairs as delay stages, which degrades the phase noise due to the excess noise generated by the resistors. The rotary-wave oscillators are based on differential excitation of a closed-loop transmission line at evenly-spaced points, producing accurate multiple phases with low phase noise [10], [21], [22]. However,

Fig. 17. Rotary-wave oscillators: (a) conventional, (b) modified by adding the direction-determined circuit, and (c) proposed.

the circularly-symmetric nature of the rotary-wave oscillators causes two possible modes of operation, i.e., clockwise or counterclockwise rotation, resulting in uncertainties of the phase sequence [10]. Since half of the clock phases will align with data edges at lock (and hence performs metastable sampling), it is critical to obtain a *definite* and *pre-determined* phase sequence so that optimally-sampled data outputs are selected.

To eliminate the phase ambiguity, the conventional rotary-wave oscillator in Fig. 17(a) can be modified to that depicted in Fig. 17(b) [22]. A *low-strength* ring oscillator formed by inverters is superimposed on the main oscillator, connecting the four clock phases in a pre-determined sequence. Though the inverters can be made small, they present extra loading capacitances on the outputs, potentially degrading the speed and tuning range. To alleviate this issue, we propose a new oscillator topology by simply changing the interconnections of the pMOS transistors in Fig. 17(a), arriving at the circuit shown in Fig. 17(c). The idea is to use *strong* nMOS transistors as negative- g_m providers and *weak* pMOS transistors as low-strength

couplers, by recognizing the intrinsic difference between their driving capabilities. The size of nMOS transistors are designed to satisfy the start-up condition, while the size of pMOS transistors should be minimized so as not to perturb the symmetric operation of the rotary-wave oscillator.

The main difference between the proposed oscillator and the coupled LC oscillator [18], [19] is that the former relies on the symmetry of the closed-loop LC line to generate multiple phases, *not* on the strength of the coupling factor (as the latter). The coupling only determines the direction of rotation. Therefore, a very weak coupling factor still yield near-quadrature phases since the operation is primarily dominated by the rotary-wave oscillator. As the pMOS transistors are made smaller, the voltage headroom shrinks and ultimately limits the minimum achievable coupling factor. A resistor [R_B in Fig. 17(c)] instead of a current source is thus used for biasing, relaxing the headroom and eliminating the flicker noise contributed by the current source, which is more pronounced when biased at a low overdrive.

Fig. 18. Simulated phase error and phase noise versus different size of PMOS.

Fig. 19. Data sequence that causes the PD to provide no phase correction.

With $W_N = 14 \mu\text{m}$, W_P is swept from 4–10 μm and the phase noise and phase accuracy are plotted in Fig. 18. The bias resistor is adjusted accordingly to make the power consumption equal in all cases. The phase accuracy has little dependence on the coupling factor, while the phase noise gets slightly worse as the coupling becomes stronger. The minor dependence of phase noise and phase accuracy on the coupling factor confirms that the operation is indeed dominated by the rotary-wave oscillator. With $W_P = 6 \mu\text{m}$, the output common mode is close to $V_{DD}/2$ which maximizes the tuning range, while the phase noise degrades by only 0.2 dB compared to $W_P = 4 \mu\text{m}$. Considering the operation of the next stage (i.e., the clock buffer) and the required tuning range, the final design yields $W_P = 6 \mu\text{m}$.

B. Phase Detector and V/I Converter

The PD is based on the Alexander topology [23] shown in Fig. 3. Every three consecutive samples are fed to the XOR gates, which generate the early or late controls. In the absence of data transitions, the control voltage remains undisturbed, minimizing the jitter during long runs. Note that the output of the DFF sampled by $CK270$ in Fig. 3 is not used for phase comparison. This scenario reduces the data transition density and causes the PD to provide no phase correction when the input data sequence 11001100... occurs, as illustrated in Fig. 19. However, even the control voltage remains fixed, the VCO frequency and phase still change due to its intrinsic noise and temperature variations. Such frequency/phase drift will cause the CKQ phase to sample the vicinity of the data edge, providing information for phase corrections. Besides, since the CDR circuit is fed with random data rather than periodic data, such situation will not remain endlessly.

The DFFs use CML latches, while the XOR gates and V/I converter are modified from [10]. Resistors instead of current mirrors are used at the XOR outputs, resulting in larger output swings at high speed. Moreover, this allows separate optimiza-

Fig. 20. Clock buffer.

Fig. 21. Die photos of (a) transimpedance-AGC amplifier and (b) CDR circuit.

tion of the bias current of the XOR gate and that of the V/I converter, providing extra degree of freedom in the design.

C. Clock Buffer

The large loading capacitance presented by the PD (4 latches to each clock phase) suggests the use of clock buffers between the VCO and the PD. The buffers should provide large output swings for high-speed sampling while simultaneously isolating the VCO from random data transitions. Resistor-loaded buffers consume large amount of power even with inductive peaking, which is primarily due to the limited bandwidth caused by the RC pole. LC resonant buffers are able to provide high gain at tens of gigahertz because they only operate in the vicinity of the tuned frequency. Since the gain drops dramatically when the operating frequency deviates from the resonance of the LC tank, this kind of buffers poses more design risk as the center frequency of the VCO may drift due to process variations. To cover a wider frequency range, a resistor R_P is added in parallel with the LC tank as shown in Fig. 20, decreasing the Q but increasing the operation range. With $R_P = 1.5 \text{ k}\Omega$ and 3 mA bias current, simulation indicates that each clock buffer presents a gain of 10 dB and a bandwidth of 5.4 GHz, which is 3 times larger than the VCO tuning range.

V. EXPERIMENTAL RESULTS

Both circuits have been fabricated in 90 nm digital CMOS technology. Fig. 21 shows the die photos. The amplifier oc-

Fig. 22. Measured single-ended S_{11} and the corresponding input impedance.

cupies $0.86 \times 0.65 \text{ mm}^2$ and the CDR circuit occupies $0.7 \times 0.6 \text{ mm}^2$, both including the pads. The circuits have been tested on a high-speed probe station with Anritsu random data generator (MP1803A + MP1758A) providing the 40 Gb/s input. Precision Timebase Module (Agilent 86107A) and 70 GHz dual-remote sampling head (Agilent 86118A) were used to minimize the jitter caused by the oscilloscope itself.

A. Transimpedance-AGC Amplifier

To characterize the transimpedance gain, normally the two-port S parameter should be measured. However, the limited area when we taped out the chip forced us to change the output GSGSG pad to $100 \mu\text{m}$ pitch. The unequal pitches between the input and output pad makes it difficult to measure the two-port S parameter because there is no “thru” calibration kit with different pitches on its two sides. Besides, high-frequency network analyzers are mostly single-ended. Due to these reasons, only the one-port S parameter is measured and combined with the time domain measurement to determine the transimpedance gain. Fig. 22 shows the measured single-ended S_{11} , which is used to calculate the input impedance:⁶

$$Z_{\text{in}} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \quad (25)$$

where Z_0 equals to 50Ω per side. The S_{11} remains below -8 dB up to 36.5 GHz and the magnitude of the input impedance averaged from 100 MHz to 40 GHz is 106Ω differential. Since the amplifier directly drives 50Ω loads, the transimpedance gain can be obtained as follows [4], [24]:

$$\begin{aligned} Z_t &= Z_0 \frac{S_{21}}{1 - S_{11}} \\ &= Z_0 \frac{1 + S_{11}}{1 - S_{11}} A_v \end{aligned} \quad (26)$$

where A_v represents the voltage gain which is measured by the time domain test.

The output swing of the random data generator is fixed at $2V_{\text{pp}}$. To determine the maximum linear gain of the amplifier, the input swing needs to be attenuated to 11mV_{pp} per side, which is equivalent to $214\mu\text{A}_{\text{pp}}$, so that the output buffer

⁶With such a large number of stages in this amplifier chain, S_{12} is quite small and $\Gamma_{\text{in}} \sim S_{11}$ [24].

Fig. 23. The 40 Gb/s $2^{31} - 1$ eye coming out of the generator with 22mV_{pp} swing. The corresponding output is shown in Fig. 24(b).

remains unsaturated. With such input swing, the output swing is non-limited and equal to 440mV_{pp} differential, indicating a transimpedance gain of $2 \text{ k}\Omega$. Since a swing of 11mV_{pp} is too small to be clearly displayed on the oscilloscope, Fig. 23 shows the eye diagram coming out of the generator with 22mV_{pp} swing.⁷ The 40 Gb/s amplifier outputs in response to different levels of input swings are shown in Fig. 24(a)–(d). For input larger than $430\mu\text{A}_{\text{pp}}$, the output buffer limits the swing to 520mV_{pp} differential. At high input currents, low jitter and little pulse-width distortion are observed due to the activation of the AGC. The BER is less than 10^{-9} for input spanning from 0.43 to 4mA_{pp} . Comparing the input and output eye diagrams, the bandwidth is conservatively estimated to be 22 GHz (which is dominated by the post amplifier).

The integrated output noise is measured on the oscilloscope [3]. By setting the gain to maximum and then disable the input signal source, the integrated single-ended output noise is obtained by the histogram function shown in Fig. 25. Since the noise at the two outputs of a multistage differential amplifier is highly anti-correlated [25], the integrated input-referred noise can be calculated as

$$\begin{aligned} I_{n,\text{in,tot}} &= \frac{2\sqrt{(3.64 \text{ m})^2 - (1.5 \text{ m})^2}}{2k} \\ &= 3.3 \mu\text{A}_{\text{rms}} \end{aligned} \quad (27)$$

where the $1.5\text{mV}_{\text{rms}}$ noise contributed by the oscilloscope itself has been subtracted. The average input-referred noise density is

$$\begin{aligned} I_{n,\text{in,avg}} &= \frac{I_{n,\text{in,tot}}}{\sqrt{BW}} \\ &= 22\text{pA}/\sqrt{\text{Hz}}. \end{aligned} \quad (28)$$

The measured performance is summarized in Table I and compared with prior published 40 Gb/s TIAs. This CMOS design provides a moderate gain of $2 \text{ k}\Omega$ and an output swing of 520mV_{pp} for input spanning from $430\mu\text{A}_{\text{pp}}$ to 4mA_{pp} , while consuming 75 mW including the output buffer. Since the

⁷The corresponding output is shown in Fig. 24(b).

Fig. 24. Measured 40 Gb/s $2^{31} - 1$ single-ended output eyes for input swings of (a) $214 \mu A_{PP}$, (b) $430 \mu A_{PP}$, (c) $870 \mu A_{PP}$, and (d) $4 mA_{PP}$. [Horizontal scale: 5 ps/div; vertical scale: 40 mV/div in (a), 60 mV/div in (b), and 50 mV/div in (c) and (d).]

Fig. 25. Measured integrated output noise.

amplifier can also be viewed as a 50Ω -matched voltage amplifier, its performance is compared to other 40 Gb/s amplifiers in Table II. At such high data rate, the gain of this work is the highest while the power dissipation and area are smaller than those of previous works.

TABLE I
MEASURED PERFORMANCE COMPARED WITH PRIOR PUBLISHED 40 Gb/s TIAs

	[2]	[3]	[4]	[8]	This Work
Technology	160-GHz InP	160-GHz InP	200-GHz SiGe	0.18 μm CMOS	90nm CMOS
Data Rate (Gb/s)	43	40	40	N/A ⁺	40
Gain (Ω)	6k	631	282	350	2k
Dynamic Range (dB)	36 BER < 10^{-12}	N/A	N/A	N/A	19 BER < 10^{-9}
Input-Referred Noise (pA/ $\sqrt{Hz}$)	N/A	29 _{avg.}	< 20 _{avg.}	34 ⁺⁺	22 _{avg.}
Supply (V)	3.3	5.2	5.2	1.8	1.2
Power (mW)	450	458	182	60	75

⁺: No eye diagram measurement.

⁺⁺: Measured at 26 GHz.

B. CDR Circuit

The measured VCO tuning range is 1.6 GHz as depicted in Fig. 26(a). The free-running spectrum when $V_{ctrl} = 0$ is shown in Fig. 26(b), indicating a phase noise of -92 dBc/Hz at 1 MHz offset. The Q of inductors in the VCO is 30% smaller than the predicted value according to the measured output power and

TABLE II
MEASURED PERFORMANCE COMPARED WITH PRIOR
PUBLISHED 40 Gb/s AMPLIFIERS

	[5]	[6]	[7]	[9]	This Work
Technology	0.18 μ m	0.18 μ m	90nm	0.18 μ m	90nm
CMOS	CMOS	CMOS	CMOS	CMOS	CMOS
Gain (dB)	15	4	20	20	26
BW (GHz)	22 ⁺	39	23	39.4	22 ⁺
GBP (GHz)	124	62	230	394	440
Supply (V)	2.2	1.8	1.0	2.8	1.2
Power (mW)	190	140	80	250	75
Area (mm ²)	0.5	3.3	0.033 ⁺⁺	2.24	0.56

⁺: Estimated by the measured output eye diagram.

⁺⁺: Only core area.

(a)

(b)

Fig. 26. (a) Measured VCO tuning characteristic. (b) Free-running spectrum when $V_{ctrl} = 0$.

phase noise. Fig. 27(a) shows the spectrum of the clock in response to a 40 Gb/s $2^{31} - 1$ PRBS input. The in-band phase noise is suppressed to -101.5 dBc/Hz at 1 MHz offset. The waveform of the recovered clock is depicted in Fig. 27(b), suggesting an rms jitter of 0.7 ps and a peak-to-peak jitter of 5.6 ps. Fig. 28

(a)

(b)

Fig. 27. (a) Spectrum and (b) waveform of the recovered clock in response to a 40 Gb/s $2^{31} - 1$ PRBS input. [In (b), horizontal scale: 10 ps/div; vertical scale: 18 mV/div].

Fig. 28. Recovered half-rate data and clock.

plots the retimed data along with the clock. The data exhibits 13.3ps_{pp} jitter with BER < 10^{-9} . Table III summarizes the measured performance. The power consumption is 48 mW, of which 3 mW is dissipated in the VCO, 8 mW in the clock buffers driving the DFFs, and 36 mW in the PD. The measured rms jitter

TABLE III
MEASURED CDR PERFORMANCE COMPARED WITH PRIOR PUBLISHED WORKS

	[10]	[11]	[12]	This Work
Technology	0.18 μ m CMOS	149-GHz InP/InGaAs	120-GHz SiGe	90nm CMOS
Data Rate	40-Gb/s	43-Gb/s	45-Gb/s	40-Gb/s
Clock Rate	10-GHz	43-GHz	22.5-GHz	20-GHz
Rec. Clock Jitter	0.9ps _{rms} (2 ³¹ -1 PRBS)	0.48ps _{rms} (2 ³¹ -1 PRBS)	1.1ps _{rms} (2 ⁷ -1 PRBS)	0.7ps _{rms} (2 ³¹ -1 PRBS)
BER	10 ⁻⁶	N/A	N/A	10 ⁻⁹
Supply	2V	4.5V	2.5V	1.2V
Power	144mW	1.89W	650mW	48mW
Area	1.4mm ²	4mm ²	1.25 mm ²	0.42mm ²

is comparable to those of previous works while the power consumption and area are much smaller.

VI. CONCLUSION

A 40 Gb/s transimpedance-AGC amplifier and CDR circuit are designed and verified in 90 nm digital CMOS, demonstrating the potential of standard CMOS technology for receivers operating at tens of gigabits per second. The proposed circuits and design methodology resolve a number of issues and provide promising performance with lower power dissipation compared to similar circuits realized in SiGe, InP, or GaAs technologies.

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