A 0.5–5-GHz Wide-Range Multiphase DLL With a Calibrated Charge Pump

Chi-Nan Chuang, *Student Member, IEEE*, and Shen-Iuan Liu, *Senior Member, IEEE*

Abstract—A 0.5–5 GHz wide-range multiphase delay-locked loop (MDLL) with a calibrated charge pump is presented. A multiperiod-locked technique is used to enhance the input frequency range of a MDLL and avoid the harmonic-locked problem. The charge pump current is also calibrated to reduce the static phase error. This MDLL has been fabricated in 0.13- μm CMOS process. The measured root-mean-square and peak-to-peak jitters are 1.06 and 8 ps at 5 GHz, respectively. The power dissipation at 5 GHz is 36 mW for a supply voltage of 1.2 V.

Index Terms—Calibration, charge pump, delay-locked loop, multiperiod-locked technique.

I. INTRODUCTION

IN RECENT years, the delay-locked loop (DLL) is widely used for synchronization, clock generation [1], [2] and digital transceivers [3] in serial links. Owing to the rapid advance in technology, the high-speed data transmission rate is also desired. To realize the high-frequency multiphase DLL (MDLL), several problems should be considered. To increase the input frequency of the MDLL, the accuracy of the phase detector (PD), the matching between the up/down charge pump (CP) currents, and the bandwidth requirement of the delay cells in a voltage-controlled delay line (VCDL) should be considered. When the input frequency is high enough, the intrinsic phase offset of the PD will limit the phase resolution. The current mismatch between the up and down current in a CP will result in the static phase error between the input and output clocks. Once the number of the delay cells or the frequency of the input clock is increased, the total intrinsic delay of the VCDL will become an important issue. If the total intrinsic delay is greater than the period of the input clock, the harmonic-locked problem may occur. In a MDLL, once the delay of the VCDL is known, the operating range of this MDLL will be determined. So the delay range of the VCDL will directly limit the operating range of a MDLL.

To solve the above problems and enlarge the operating range of a MDLL, a multiperiod-locked technique [4] with a selectable locked period and the calibrated CP are adopted in this work. This paper is organized as follows. The multiperiod-locked technique [4] with a selectable locked period will be discussed in Section II. The circuit description will be given in Section III. The experimental results will be given in Section IV. The conclusion is given in Section V.

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The authors are with the Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10617, R.O.C. (e-mail: lsi@cc.ee.ntu.edu.tw).

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Fig. 1. Proposed multiperiod-locked MDLL with a selectable locked period.

II. MULTIPERIOD-LOCKED TECHNIQUE

The proposed multiperiod-locked MDLL with a selectable locked period is shown in Fig. 1. It is composed of the PD, a capacitor (C_L), a calibrated CP, a VCDL with eight delay cells, a duty-cycle correction (DCC) array, two divide-by- N dividers, two demultiplexers, a start-controlled circuit, and a multiplexer. The VCDL uses the differential-to-single (D2S) circuits to convert the differential clocks into single-ended one. The dummy D2S circuits are inserted in the outputs of the delay cells to match the loads. Two demultiplexers are used to select or bypass the divider to enlarge the operation frequency of this MDLL. The DCC array is used to correct the duty cycle of the output clocks. To save the output pads, the 8-to-1 multiplexer is adopted to output the clocks sequentially.

To understand the operation principle of this MDLL, a special case of $N = 3$ is explained, where N is the divider's ratio. Its timing diagram is shown in Fig. 2. First, the signal, Divider_Switch, enables the demultiplexers to select the divider-by-3 divider. When the signal, Start, is high, the input clock, CK_{in} , and the output clock, CK_{VCDL} of the VCDL are divided by three. Then, the divide-by-3 outputs, q_1 and q_2 , are connected to the start-controlled circuit. The start-controlled circuit is composed of four D-flip-flops (DFFs), and two AND gates, as shown in Fig. 1. The clock, CK_{P2} , is enabled by the DFF3, q_2 , and an AND gate; then the signal, up, is active to charge the loop filter, C_L , to decrease the delay of the VCDL to minimum. It ensures that this MDLL will be locking from the minimal VCDL to avoid the harmonic-locked problem [2]. The dummy DFF4 is used to match the delay. The clock, CK_{P1} , is enabled after three periods of the input clock CK_{in} .

Fig. 2. Timing diagram of the proposed MDLL when $N = 3$.

by the DFF1, DFF2, the AND gate and q1. When this multi-period-locked MDLL is locked, the total delay of the VCDL is equal to $NT_{\text{REF}} (= 3T_{\text{REF}})$, where T_{REF} is the period of the input clock.

To consider the general case, assume the number of the delay cells in the VCDL to be M . let N and M be co-prime. The output phase of the j th delay cell in a VCDL with respect to the input clock of the first delay cell (D1) in Fig. 1 is expressed as

$$\left(\frac{jN}{M} - \left\lfloor \frac{jN}{M} \right\rfloor \right) \cdot T_{\text{REF}}, \quad j = 1 \sim M \quad (1)$$

where N , M , and j are integers, and $\lfloor \cdot \rfloor$ denotes the Gauss symbol. Although the monotonic phase relation among the delay cells does not hold, the multiphase characteristics still exist. For example, in a conventional MDLL, if $N = 1$ and $M = 8$ in (1), the output phases of the eight delay cells will be

$$\frac{1}{8}T_{\text{REF}}, \frac{2}{8}T_{\text{REF}}, \frac{3}{8}T_{\text{REF}}, \frac{4}{8}T_{\text{REF}}, \frac{5}{8}T_{\text{REF}}, \frac{6}{8}T_{\text{REF}}, \frac{7}{8}T_{\text{REF}}, \frac{8}{8}T_{\text{REF}}. \quad (2)$$

In the proposed multiperiod-locked MDLL, if $N = 3$ and $M = 8$, the output phases of the eight delay cells will be

$$\frac{3}{8}T_{\text{REF}}, \frac{6}{8}T_{\text{REF}}, \frac{1}{8}T_{\text{REF}}, \frac{4}{8}T_{\text{REF}}, \frac{7}{8}T_{\text{REF}}, \frac{2}{8}T_{\text{REF}}, \frac{5}{8}T_{\text{REF}}, \frac{8}{8}T_{\text{REF}} \quad (3)$$

Although the phase sequence is not monotonic, the multiphase characteristics still exist. To have the monotonic phase outputs, the outputs of the delay cells can be appropriately routed.

For the proposed multiperiod-locked MDLL to work properly, the maximal delay $T_{d,\text{max}}$ and the minimal delay $T_{d,\text{min}}$ of the VCDL should satisfy the following constraint

$$T_{d,\text{max}} \geq N \cdot T_{\text{REF}} \geq T_{d,\text{min}}. \quad (4)$$

Fig. 3. (a) Transfer curve of a conventional PD (b) Transfer curve of a conventional PD with a divide-by-3 divider.

By adopting the start-controlled circuit and choosing N and M to be co-prime, the limitations of the intrinsic delay and the number of the delay cells are relaxed. It is because that the VCDL could be locked with multiple periods. Consider two special cases: $N = 1$ and $N = 3$. When $N = 1$, it is equivalent to a conventional DLL. Thus, the useful frequency range of the conventional DLL is

$$F_{\text{ref(max)}} - F_{\text{ref(min)}} = \frac{1}{T_{d,\text{min}}} - \frac{1}{T_{d,\text{max}}} \quad (5)$$

where $F_{\text{ref(max)}}$ denotes the maximal input frequency and $F_{\text{ref(min)}}$ denotes the minimal input frequency. When $N = 3$. The useful frequency range of the proposed MDLL is

$$F_{\text{ref(max)}} - F_{\text{ref(min)}} = 3 \left(\frac{1}{T_{d,\text{min}}} - \frac{1}{T_{d,\text{max}}} \right). \quad (6)$$

For a conventional MDLL without the harmonic-locked problem, the frequency range is limited as (5). For the proposed MDLL, the input frequency range is also increased by N times as shown in (6). However, the penalty is that the VCDL is increased by N times; it may consume a lot of power and degrade the output jitter performance. The jitter transfer of this DLL is similar to an all-pass function [5]. Moreover, the longer the VCDL is, the worse the jitter is. To save the VCDL and achieve the wide-range MDLL, $N = 3$ is adopted when the MDLL works within 2–5 GHz. $N = 1$ (conventional method) is adopted when the MDLL works within 0.5–2 GHz. The locked period is selected by the divider_switch in Fig. 1.

For the conventional start-controlled-circuit [2], the transfer curve of a PD is shown in Fig. 3(a). If the delay range of the VCDL is wide enough, the harmonic-locked problem may occur. If a divide-by-3 divider is added in front of this PD, its transfer curve is given in Fig. 3(b). Although this PD still has the capture range from -2π to 2π , its capture range is enlarged three times compared with a conventional PD. It is because that input frequency is reduced by three times. So, when a start-controlled circuit and a divide-by- N divider are used in a PD, its capture range is enlarged N times and without false or harmonic locking issues.

III. CIRCUIT DESCRIPTION

The detail circuits in the proposed multiperiod-locked MDLL will be discussed as follows.

Fig. 4. Calibration circuit.

A. The Calibrated CP

To design the CP in the advanced process, there are several issues have to be considered. First, the short channel effect is significant. For example, the channel length modulation will lower the output resistance of the device to degrade the analog current mirror. Second, the switching time difference between the controlling signals applied to the pMOS and nMOS switches will cause the voltage variation of the loop filter. It increases the output jitter in the DLL. The transmission gate can be added to compensate the propagation delay of the inverter. Third, due to the current mismatch in a CP, it will cause a large static phase error, even the DLL is locked. To reduce the current mismatching in the CP, a calibration circuit is adopted in this work.

Fig. 4 shows a calibration circuit to reduce the current mismatching in a main CP. It is composed of a replica CP, a voltage-to-current converter, an operational amplifier, and an additional capacitor. It is similar to the dynamic current matching CP in [6]. The main CP is composed of the devices M1-M4 and Vb1 and Vb2 are the biased voltages. The capacitor C_L is used as the loop filter in a DLL. The signals, up_{pd} and dn_{pd} , come from the outputs of a PD. To compensate the propagation delay of the inverters (Inv1, Inv2), the transmission gates (Tr1, Tr2) are added. The controlling signals, $\overline{up}$ and $\overline{dn}'$, control the main CP to charge or discharge the loop filter, respectively. To detect the offset current between the up and down currents in the main CP, the replica CP is used. Assume two CPs are matched. This replica CP is composed of M5-M8. When $\overline{dn}$ is high and $\overline{dn}'$ is low, the offset current between the up and down currents in a replica CP will charge or discharge the capacitor, C_1 . The operational amplifier will amplify the error voltage and the voltage-to-current converter will convert this error voltage into a current to compensate the offset current in C_L and C_1 . The devices, M9 and M10, and two passive resistors are used to realize the voltage-to-current conversion. The current mirrors, M11-M30, are used to realize two outputs currents of the voltage-to-current converter, which are controlled by $\overline{dn}$ and $\overline{dn}'$, respectively. In the steady state, the output current of the voltage-to-current converter will be equal to the offset current for both the CPs.

Fig. 5. (a) DLL with a normal CP. (b) DLL with a calibrated CP.

Fig. 6. Delay cell.

To enhance the current mismatch of the CP, C_1 is chosen to be smaller than C_L . However, if C_1 is too small, the clock injection from the replica CP is significant to result in a ripple on the C_1 . It will degrade the current compensation of the calibration circuit. Based on the simulation results, C_1 is chosen around $C_L/10$ in this work.

If the operational amplifier has the offset voltage, it will degrade the accuracy of the calibration circuit. Moreover, the matching requirement between the replica and main CPs is also critical. To remedy these effects, the long channel devices and careful layout should be adopted.

Compared with the dynamic current matching CP in [6], the voltage-to-current converter will provide the wide current compensation and better linearity. However, the penalty is that the power consumption will increase.

By using the proposed calibrated CP, the static phase error in a DLL can be decreased. When the CP has the current mismatch of 10% and the MDLL locked at 5 GHz, the simulated static phase error between input and output clocks is 20 ps as shown in Fig. 5(a). When the calibrated CP is adopted, Fig. 5(b) shows the simulated static phase error is reduced and is less than 1 ps.

B. Delay Cell

To generate the eight multiphase output, The VCDL is composed of eight delay cell units. The delay cell adopted in this work is similar to [7] as shown in Fig. 6. Each delay cell consists of a pseudo differential amplifier for high-speed operation. Since the strong pMOS latch will decrease the bandwidth of the delay cell, the weak pMOS latch, M3-M4 ($W/L = 2.5u/0.13u$), is adopted to speed up the signal transition of the differential pair, M1-M2 ($W/L = 4u/0.13u$). However, it will slow down the slew rate of the output signal. To improve the driving capability of the delay cell, the pMOS transistors, M5-M6 ($W/L = 2u/0.13u$), in triode are added to increase the driving capability. The pMOS transistors, M7-M8 ($W/L = 4u/0.13u$), are used to adjust the delay. The dummy

Fig. 7. DCC circuit.

Fig. 8. Die photo.

D2S circuits are inserted to ensure each delay cell to have the same loading.

C. Duty-Cycle Correction Circuit and the Divide-by- N Divider

Since the input clock and the delay cells are fully differential, the complementary phase-blending technique [8] is adopted to correct the duty cycle distortion as shown in Fig. 7. The true-single-phase-clocking technique [2] is adopted to realize the frequency divider.

IV. EXPERIMENTAL RESULTS

The proposed MDLL has been fabricated in $0.13\text{-}\mu\text{m}$ CMOS process. Fig. 8 shows the die photo. The core area of the proposed MDLL is $450 \times 239\text{ }\mu\text{m}$. The supply voltage is 1.2 V , and the total power consumption with output buffers is 36 mW . When $N = 3$, the measured eight multiphase outputs, $\phi_1 \sim \phi_8$, at 5 GHz for the proposed MDLL are shown in Fig. 9, where the vertical scale is 1.9 mV/div and the horizontal scale is 10 ps/div . Fig. 10 shows the measured root-mean-square and peak-to-peak jitters are 1.06 ps and 8 ps , respectively, at 5 GHz . When $N = 1$, Fig. 11 shows the measured eight multiphase outputs at 0.5 GHz , where the vertical scale is 67.1 mV/div and the horizontal scale is 400.2 ps/div . The measured frequency range of this MDLL is 0.5 GHz – 5 GHz . From Figs. 9 and 11, to have the monotonic phase outputs, the additional 2-to-1 multiplexers should be inserted to the outputs of the delay cells. Fig.

Fig. 9. Measured multiphase outputs at 5 GHz . Fig. 10. Measured output jitter at 5 GHz . Fig. 11. Measured multiphase outputs at 0.5 GHz .

12 shows the measured static phase error is 30 ps when the CP is not calibrated. Fig. 13 shows the measured static phase error is reduced to less than 1 ps after the CP is calibrated.

Compared with previous DLLs, this work achieves the wide range and high speed operation. The performance summary and comparison results are shown in Table I.

Fig. 12. Measured static phase error between input and output of the MDLL when the CP is not calibrated.

Fig. 13. Measured static phase error between input and output of the MDLL when the CP is calibrated.

TABLE I
PERFORMANCE COMPARISON

	This work	[4]	[9]	[10]
Process	0.13 μ m	0.09 μ m	0.18 μ m	0.18 μ m
Supply	1.2V	1V	1.8V	1.8V
Operation range	0.5–5GHz	2–5GHz	0.9–2.9GHz	0.25–2GHz
RMS jitter	1.06ps @5GHz	0.87ps @5GHz	1.62ps @2.16GHz	2.81ps @2GHz
Peak-to-peak jitter	8ps @5GHz	7.56ps @5GHz	12.9ps @2.16GHz	20ps @2GHz
Power	36mW	45mW	19.8mW	6.4mW
Area	0.107mm ²	0.121mm ²	0.27mm ²	0.046mm ²

V. CONCLUSION

The proposed multiperiod-locked MDLL has been fabricated in 0.13- μ m CMOS process. The multiperiod-locked technique and the proposed start-controlled circuit are used to avoid the harmonic-locked and long intrinsic delay problems in a high-speed MDLL. The calibrated CP is also proposed to reduce the static phase error. The experimental results have demonstrated the feasibility.

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