Spur-Suppression Techniques for Frequency Synthesizers

Che-Fu Liang, *Student Member, IEEE*, Hsin-Hua Chen, and Shen-Iuan Liu, *Senior Member, IEEE*

Abstract—A frequency synthesizer with two spur-suppression circuits has been fabricated in 0.18 μm CMOS technology. The chip area is $1.3 \text{ mm} \times 1.3 \text{ mm}$. The frequency synthesizer consumes 18.9 mW from a 1.8-V supply. Compared with the conventional frequency synthesizer without the spur-suppression circuit, the measured reference spur at 8 MHz is reduced by 18 dBc for the first spur-suppression circuit and 31 dBc for the second one. The measured switching time from 1792 to 1824 MHz is 27.89 μs within 20 ppm of the target frequency.

Index Terms—Charge pump (CP), frequency synthesizer, integer- N , spur suppression.

I. INTRODUCTION

THE reference spur for a phase-locked loop (PLL) is generated by the periodic ripples on the control line of the voltage-controlled oscillator (VCO) [1]. In a PLL-based frequency synthesizer, the mismatch in the charge pump (CP) and the timing error in the controlling signals of phase-frequency detector (PFD) generate the ripples. These nonidealities severely deteriorate the spectral performance [2]. The magnitude of the reference spur can be calculated by the narrowband frequency modulation approximation [2]. The relation between spur amplitude A_{spur} and carrier amplitude A_{carrier} is given as

$$\frac{A_{\text{spur}}}{A_{\text{carrier}}} = \frac{1}{2} \cdot \frac{K_{\text{vco}} \times V_m}{2\pi f_{\text{ref}}} \quad (1)$$

where K_{vco} (Hz/V) is the VCO gain, V_m is the amplitude of the ripple, and f_{ref} is the reference frequency. From (1), the magnitude of the spur is proportional to the amplitude of the ripple and the VCO gain. In addition, the magnitude of the spur is also inversely proportional to the frequency of the periodic ripple on the control line. Several techniques have been presented to improve the spur [3]–[9]. One of the intuitive ways is to adopt a reduced VCO gain [3]–[5]. To avoid the process variations and have a wide frequency range, the switched-capacitor technique or digital calibration circuits [2] may be needed.

Another method is to reduce the CP mismatch [6]–[9]. In [6], a digital controller calibrates the replica CP to improve the current matching. Assume both the main CP and the replica one are matched to reduce the ripple. Since two CPs operate on the different controlled voltages, it is hard to compensate the current mismatch due to the channel-length modulation. Moreover, the

mismatch between two CPs still exists. In [7], [8], the common-mode feedback circuit, an additional reference voltage, and the operational amplifier are needed. The nonideal effects of the operational amplifier have to be considered; such as the stability and offset voltage. In [9], the multiple PFDs, CPs, multiplexers, and additional delay cells are needed. It may degrade the in-band noise floor.

In this work, two spur-suppression circuits based on the delay-sampled concept are presented to suppress the spurs without sacrificing the frequency switching time. This paper is organized as follows. Section II introduces the proposed spur-suppression circuits. The building blocks are also given. The experimental results are given in Section III and the conclusion is given in Section IV.

II. CIRCUIT DESCRIPTION

To verify the proposed spur-suppression techniques, a frequency synthesizer is designed for UHF band IV and V (470–862 MHz) [10] in a DVB-H direct-conversion receiver. In order to generate the precise quadrature clocks for direct-conversion receivers, this VCO operates from 1880 to 3448 MHz, which can be divided by 4 to cover the UHF band IV and V. The proposed integer- N frequency synthesizer is shown in Fig. 1. It is composed of a conventional frequency synthesizer, a spur-suppression circuit, a lock detector, and a pseudo-random-bit-string (PRBS) generator. To cover such a wide frequency range, the four-bit controlled switched capacitors are used in the VCO to generate sixteen overlapping tuning curves. The input reference clock CK_{ref} is 8 MHz, which is divided from the external clock CK_{ext} of 16 MHz. Two spur-suppression circuits will be discussed in the following paragraphs.

A. First Spur-Suppression Circuit

The first spur suppression circuit and its timing are shown in Fig. 2(a) and (b), respectively. The basic idea is to randomize the charge redistribution time. Initially, the lock detector is unlocked, i.e., $\overline{\text{LD}} = \text{"1"}$. The lock detector selects the unlocked path and the frequency synthesizer behaves like a conventional PLL. When the lock detector is locked (i.e., $\overline{\text{LD}} = \text{"0"}$), the locked path is selected. The clocks ϕ_1 and ϕ_2 are realized by CK_{ref} , CK_{ext} , the feedback clock CK_{fdl} , and several logic circuits as shown in Fig. 2(b). The pulse position for ϕ_1 is fixed, but not for ϕ_2 . The pulse position of ϕ_2 within a reference clock period of T_{ref} is determined by the PRBS generator. Supposed that $\text{PRBS} = 1$, the pulse A is on and the pulse B is off within a reference clock period. When $\text{PRBS} = 0$, the pulse A is off and the pulse B is on. After ϕ_1 is on, the CP transfers the charges to the capacitor C_1 according to the input phase error but the low-pass filter (LPF) is isolated from C_1 . When ϕ_2 is on, the

Manuscript received December 18, 2006; revised March 6, 2007. This paper was recommended by Associate Editor S. Pavan.

The authors are with the Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10617, R.O.C. (e-mail: lsi@cc.ee.ntu.edu.tw).

Digital Object Identifier 10.1109/TCSII.2007.896938

Fig. 1. Spur-suppression frequency synthesizer.

Fig. 2. (a) First spur-suppression circuit by randomizing the charge redistribution time. (b) Its timing diagram.

charges on the capacitor and the LPF are redistributed. Ideally, the reference spur can be reduced significantly. However, the nonidealities in analog CMOS switches, such as charge injection and clock feedthrough, still periodically disturb the voltage on the LPF when ϕ_2 is off. Therefore, a PRBS generator is used to randomize these effects. Intuitively, the pulse A or B will randomly appear depending upon the PRBS generator and the peak energy of the reference spur will be dispersed. Note that since there is an intrinsic delay to generate the clocks, ϕ_1 and ϕ_2 , the up and down signals from the PFD should be appropriately delayed. To determine the required length of the PRBS generator, some analyses are made. As shown in Fig. 3, let $r(t)$ be the original waveform on the control line with the reference clock period

Fig. 3. $r(t)$ is the original waveform without a PRBS and $g(t)$ is the PRBS-disturbing waveform on the control line of a VCO.

of T_{ref} and without the proposed spur-suppression circuit. The Fourier series representation of $r(t)$ is given as

$$r(t) = a_0 + \sum_{k=1}^{\infty} a_k \cdot \cos\left(\frac{k \cdot 2\pi}{T_{\text{ref}}} t\right). \quad (2)$$

Only considering the spur at the reference frequency, the corresponding term is

$$a_1 = \frac{1}{T_{\text{ref}}} \int_0^{T_{\text{ref}}} r(t) \cdot \cos\left(\frac{2\pi}{T_{\text{ref}}} t\right) dt. \quad (3)$$

Let $g(t)$ be the PRBS-disturbing waveform with the period of mT_{ref} , where m is determined by the PRBS length. Similarly, $g(t)$ can be represented as

$$g(t) = b_0 + \sum_{j=1}^{\infty} b_j \cdot \cos\left(\frac{j \cdot 2\pi}{mT_{\text{ref}}} t\right). \quad (4)$$

Only considering the spur at the reference frequency, the corresponding term in (4) is

$$b_m = \frac{1}{mT_{\text{ref}}} \int_0^{mT_{\text{ref}}} g(t) \cdot \cos\left(\frac{2\pi}{T_{\text{ref}}} t\right) dt. \quad (5)$$

Now referring to Fig. 3, $g(t)$ can be decomposed into m periodic pulses $g'_1(t), g'_2(t), \dots$ and $g'_m(t)$ with the period of mT_{ref} . These m pulses are almost the same except for different phase shifts. Hence, (5) can be rewritten as

$$b_m = \sum_{x=1}^m c_{m-x} = \sum_{x=1}^m \frac{1}{mT_{\text{ref}}} \int_0^{mT_{\text{ref}}} g'_x(t) \cdot \cos\left(\frac{2\pi}{T_{\text{ref}}}t\right) dt. \quad (6)$$

For $x = 2 \sim m$, when the output of the PRBS is high, the coefficient c_{m-x} is given as

$$c_{m-x} = c_{m-1} \cdot \exp^{-j\frac{2\pi}{T_{\text{ref}}}(x-1)T_{\text{ref}}} = c_{m-1}. \quad (7)$$

For $x = 2 \sim m$, when the output of the PRBS is low, the coefficient c_{m-x} is given as

$$c_{m-x} = c_{m-1} \cdot \exp^{-j\frac{2\pi}{T_{\text{ref}}}(x-0.5)T_{\text{ref}}} = -c_{m-1}. \quad (8)$$

Since the number of “1” is only one more than that of “0” in a PRBS, (6) can be simplified as

$$b_m = c_{m-1} = \frac{1}{mT_{\text{ref}}} \int_0^{mT_{\text{ref}}} g'_1(t) \cdot \cos\left(\frac{2\pi}{T_{\text{ref}}}t\right) dt. \quad (9)$$

Observing the waveforms in Fig. 3, $r(t)$ and $g'_1(t)$ are identical within the time interval $[0, T_{\text{ref}}]$. Hence, the following equation is true:

$$\int_0^{mT_{\text{ref}}} g'_1(t) \cdot \cos\left(\frac{2\pi}{T_{\text{ref}}}t\right) dt = \int_0^{T_{\text{ref}}} r(t) \cdot \cos\left(\frac{2\pi}{T_{\text{ref}}}t\right) dt. \quad (10)$$

Combining (9) with (10), the following equation is obtained as:

$$b_m = \frac{1}{mT_{\text{ref}}} \int_0^{T_{\text{ref}}} r(t) \cdot \cos\left(\frac{2\pi}{T_{\text{ref}}}t\right) dt. \quad (11)$$

Comparing (11) with (3), the spur at the reference frequency is reduced by a factor of m , which is directly related to the PRBS length. It indicates that the first spur-suppression circuit can efficiently reduce the reference spur. For example, the reference spur suppression is 16.9 and 42 dB for a 3-bit PRBS generator, i.e., $m = 7$, and a 7-bit PRBS generator, i.e., $m = 127$, respectively. However, other nonidealities such as circuit imperfections, supply noise, and substrate coupling [11], [12] make the suppression lower than the prediction. According to the simulation results, a 7-bit PRBS generator is adopted in this work.

B. Second Spur-Suppression Circuit

The second spur-suppression circuit is shown in Fig. 4(a). Its principle is to suppress the spurs by doubling the spur frequency. Similarly, when $\overline{LD} = \text{“1”}$, the unlocked path is selected as a

Fig. 4. (a) Second spur-suppression circuit by doubling the spur frequency and (b) its timing diagram.

conventional PLL. When $\overline{LD} = \text{“0”}$, the locked path is selected and the two-path switched-capacitor (SC) network is enabled. This network consists of two capacitors, C_a and C_b , and four switches controlled by the clocks, ϕ_1 , ϕ_2 , and ϕ_3 . The simplified implementation for three clocks and the timing are also shown in Fig. 4(b). Once ϕ_1 is on, the CP transfers the charge to both C_a and C_b , but the LPF is isolated. Then, the clocks ϕ_2 and ϕ_3 are turned on alternatively to redistribute the charge with the LPF. Similarly, the ripple caused by the current mismatch of the CP and timing mismatch from the PFD will not be sampled on the LPF. However, the switches controlled by ϕ_2 and ϕ_3 are carefully designed to lower the charge injection and clock feedthrough. From the timing diagram in Fig. 4(b), the equivalent reference frequency for the spur is doubled and the reference spur performance is improved. Note that we do not directly double the input reference frequency because the minimum channel spacing and required division ratio are fixed. In this design, the equivalent spur frequency is doubled without changing the loop characteristics of the frequency synthesizer.

Theoretically, one can use the multiple-path SC network to achieve a higher equivalent spur frequency and reduce the spur further.

Fig. 5. Circuit implementation.

Fig. 6. A 7-bit PRBS generator.

Fig. 7. Chip photo.

C. Remaining Circuits

In Fig. 5, the VCO consists of a nMOS cross-coupled pair to compensate the loss of LC tank and a pMOS current source provides the programmable bias current for the sake of lower flicker noise. The programmable current sources provide a large current in the lower band and a small current in the higher band. The VCO utilizes four-bit controlled switched capacitors to cover a wide frequency range. The switches consist of three nMOS transistors to reduce the extra loss.

The PRBS generator is shown in Fig. 6. The PRBS generator is composed of seven D flip-flops and one XOR gate, which are all implemented in digital combinational logics to save power. This PRBS generator provides a $2^7 - 1$ pseudo random string and it is utilized in the first spur-suppression circuit.

The PFD, CP (nominal CP current is 400 μ A), and the multi-modulus divider are adopted from [3].

III. EXPERIMENTAL RESULTS

This chip has been fabricated in a 0.18 μ m CMOS technology and measured on a chip-on-board assembly. In addition, two

Fig. 8. Measured VCO tuning curve.

(a)

(b)

(c)

Fig. 9. Measured reference spurs: (a) without the spur-suppression circuit, (b) with the first spur-suppression circuit, and (c) with the second spur-suppression circuit.

spur suppression circuits have been realized in this chip. The die photo is shown in Fig. 7. The chip area is 1.3 by 1.3 mm. The synthesizer draws 18.9 mW from a 1.8-V supply. The measured tuning curves of the VCO are shown in Fig. 8. The sixteen overlapping curves cover a frequency range from 1.7–3.45 GHz. This synthesizer is realized with a bandwidth of 120 kHz and a second-order loop filter ($R_1 = 10$ kohm, $C_1 = 200$ pF, and $C_2 = 10$ pF in Fig. 1) is adopted. Fig. 9(a) shows the measured reference spur is -50 dBc at 8-MHz offset frequency without the spur suppression technique. When the first spur-suppression circuit in Fig. 2 is enabled, Fig. 9(b) shows the measured reference spur is -68 dBc. Furthermore, when the second

Fig. 10. Measured frequency switching transient responses. (a) Switching up. (b) Switching down.

one in Fig. 4 is enabled, Fig. 9(b) shows the reference spur at 8-MHz offset is -81 dBc. However, the second-harmonic spur at 16 MHz is -60.75 dBc, which is still 3 dB lower than the conventional one in Fig. 9(a).

The switching behavior of the synthesizer is measured under a 120-kHz bandwidth with the spur suppression techniques activated. No obvious distinction in switching time is observed between these two techniques. The synthesizer is switched from 1792 to 1824 MHz and vice versa. The measured results show that the up switching time is 27.89 μ s and the down switching time is 24.89 μ s within 20 ppm of the target frequency as shown in Figs. 10(a) and (b), respectively. At 1792 MHz, the measured phase noise at 1-MHz offset frequency is -109 dBc/Hz. The performance summary and comparisons are also provided in Table I.

IV. CONCLUSION

A spur-suppression frequency synthesizer is presented. Two spur-suppression circuits have been presented. The proposed circuit has been fabricated in a 0.18- μ m CMOS process. The measured reference spur can be reduced to -68 and -81 dBc

TABLE I
PERFORMANCE COMPARISONS

	[3]	[4]	[9]	This work
Process	0.18 μ m CMOS	0.25 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS
Supply	1.8V	2.5V	1.8V	1.8V
Power	36mW	13.5mW	18mW	< 18.9mW
Freq.	5.23 – 6.16GHz	5.14–5.7GHz	4.8/2.4GHz	1.8 – 3.4GHz
Ref. freq.	20MHz	10MHz	1MHz	8MHz
Loop bandwidth	60KHz	25KHz	N/A	120KHz
Loop filter	2nd	3rd	2nd	2nd
Phase noise @ 1MHz (dBc/Hz)	-113	-116	-104/-110	<-109
Ref. spur (dBc)	-74	-70	-55	-68/-81

for two spur-suppression circuits, respectively. Comparing with previous works, the proposed techniques suppress the reference spur without sacrificing the loop bandwidth and no higher order loop filter is needed.

ACKNOWLEDGMENT

The authors would like to thank Quanta Inc., NSC, and National Chip Implementation Center for the support and fabrication of this chip.

REFERENCES

- [1] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.
- [2] T. H. Lin and W. J. Kaiser, "A 900-MHz 2.5-mA CMOS frequency synthesizer with an automatic SC tuning loop," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 424–431, Mar. 2001.
- [3] C. Y. Kuo, J. Y. Chang, and S. I. Liu, "A spur-reduction technique for a 5-GHz frequency synthesizer," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 3, pp. 526–533, Mar. 2006.
- [4] S. Pellerano, S. Levantino, C. Samori, and A. L. Lacaita, "A 13.5-mW 5-GHz frequency synthesizer with dynamic-Logic frequency divider," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 378–383, Feb. 2004.
- [5] F. Herzel, G. Fischer, and H. Gustat, "An integrated CMOS RF synthesizer for 802.11a wireless LAN," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1767–1770, Oct. 2003.
- [6] H. Huh, Y. Koo, K. Y. Lee, Y. Ok, S. Lee, D. Kwon, J. Lee, J. Park, K. Lee, D. K. Jeong, and W. Kim, "A CMOS dual-band fractional-N substrate synthesizer with reference doubler and compensated charge pump," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2004, pp. 100–101.
- [7] N. D. Dalt and C. Sandner, "A subpicosecond jitter PLL for clock generation in 0.12 μ m digital CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1275–1278, Jul. 2003.
- [8] S. Cheng, H. Tong, J. S. Martinez, and A. I. Karsilayan, "Design and analysis of an ultrahigh-speed glitch-free fully differential charge pump with minimum output current variation and accurate matching," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 9, pp. 843–847, Sep. 2006.
- [9] T. C. Lee and W. L. Lee, "A spur suppression technique for phase-locked frequency synthesizers," in *Dig. Tech. Papers ISSCC*, Feb. 2006, pp. 592–593.
- [10] I. Vassiliou et al., "A 0.18 μ m CMOS, dual-band, direct-conversion DVB-H receiver," in *Dig. Tech. Papers ISSCC*, Feb. 2006, pp. 606–607.
- [11] G. Van der Plas et al., "Modeling and experimental verification of substrate coupling and isolation techniques in mixed-signal ICs on a lightly-doped substrate," in *Dig. Tech. Papers Symp. on VLSI Circuits*, Jun. 2005, pp. 280–283.
- [12] Y. Hiraoka et al., "Isolation strategy against substrate coupling in CMOS mixed-signal/RF circuits," in *Dig. Tech. Papers Symp. on VLSI Circuits*, Jun. 2005, pp. 276–279.