Sub-1 V capacitor-free low-dropout regulator

W.-J. Huang and S.-I. Liu

A CMOS capacitor-free low-dropout regulator (LDR) operated at 0.65–0.95 V supply is presented. This LDR has been fabricated in 0.18 μm CMOS technology. The maximum output current of the LDR is 50 mA at an output of 0.5 V. The active chip area is $290 \times 420 \mu\text{m}$. The LDR can also be stable even without the output capacitor.

Introduction: To reduce the power consumption in battery-operated portable devices, various low-voltage circuits operate at an ultra-low supply voltage close to 0.5 V, such as the ADC [1], filter [2] and SRAM [3]. Integrated low dropout regulators (LDRs) [4] are widely used in portable devices, especially in noise-sensitive circuitry to provide a stable and low-noise supply voltage. Thus, a low-voltage LDR is required for integrated circuits operated at a supply lower than 1 V. To be fully integrated in a single chip, an external capacitor for an LDR is not desired. In this Letter, a sub-1 V capacitor-free LDR is presented to provide an output of 0.5 V with maximum output current of 50 mA.

Circuit description: Fig. 1 shows the proposed capacitor-free LDR. It is composed of two gain stages, a power PMOS transistor (M_P), a biasing circuit, a resistor feedback network and two Miller compensation capacitors. The first gain stage is realised by $M_1 - M_4$. The second gain stage is composed of $M_5 - M_8$. The feedback resistor network consists of the resistors R_{F1} and R_{F2} . The bodies of the NMOS transistors, $M_3 - M_6$, are connected to the gate of the diode-connected transistor, M_3 . It lowers their threshold voltages in order to operate at an ultra-low supply voltage. For reasons of access to the body terminals of the NMOS transistors, triple-well devices are used. Similarly, the bodies of the PMOS transistors, $M_7 - M_8$, are connected to the gate of the diode-connected transistor M_7 to reduce the threshold voltage.

Fig. 1 Proposed sub-1 V capacitor-free LDR

Fig. 2 Die photo

In addition, to operate over a wide supply voltage range, the differential pair of the first gain stage, $M_1 - M_2$, and the power

PMOS transistor, M_P , should be correctly biased by a biasing circuit. In Fig. 1, the proposed biasing circuit is composed of $M_{B1} - M_{B4}$ and the resistor, R_B . It generates the output voltage, V_B , to automatically track the variations of the supply voltage. When the supply voltage is close to 0.65 V, the transistors, M_{B3} and M_{B4} , operate in the cutoff region. Then, the transistor M_{B2} and the resistor R_B generate a low output voltage, $V_B = 0.35$ V. When the supply voltage increases, the transistors, M_{B3} and M_{B4} , turn on to allow V_B to track the supply voltage. The maximum V_B is designed to be 0.85 V when the supply voltage is close to 0.95 V.

Fig. 3 Measured line and load regulation

a Line regulation
b Load regulation

To get an insight into understanding the design principle of this LDR, the following analysis is made. Let g_{m1} , g_{m2} and g_{mp} , be the transconductance of the first gain stage, the second gain stage and the power PMOS transistor, respectively. R_{O1} , R_{O2} , C_{P1} and C_{P2} are the output resistances and capacitances at the outputs of the two gain stages, respectively. $R_{OUT} (= R_L || R_{Op} || (R_{F1} + R_{F2}))$ is the equivalent output resistance, where R_{Op} is the output resistance of the power PMOS transistor and R_L is the equivalent load resistance. C_{m1} and C_{m2} are Miller compensation capacitances. Assume that $g_{mp} \gg g_{m1}$, g_{m2} and $g_{m1}R_{O1}$, $g_{m2}R_{O2}$, $g_{mp}R_{OUT} \gg 1$ and neglect C_{P1} and C_{P2} . The corresponding small-signal loop transfer function is given as

$$L(s) = \frac{A_0(1 - sC_{m2}g_{mp}^{-1} - s^2C_{m1}C_{m2}g_{m2}^{-1}g_{mp}^{-1})}{(1 + (s/p_{-3dB}))(1 + (s/p_{nd}))} \quad (1)$$

where the DC loop gain $A_0 = g_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT}R_{F2}/(R_{F1} + R_{F2})$, the dominant pole $p_{-3dB} = (C_{m1}g_{m2}g_{mp}R_{O1}R_{O2}R_{OUT})^{-1}$, and the non-dominant pole $p_{nd} = g_{m2}C_{m2}^{-1}$, respectively. Since the two zeros occur at very high frequencies and even much higher than the non-dominant pole, their effects are neglected. It is possible to design the non-dominant pole to be much higher than the unity-gain frequency. It allows this LDR to have a single pole within the unity-gain frequency,

and this LDR is unconditionally stable. To meet the above requirement, the following equation should be satisfied:

$$\frac{g_{m2}}{C_{m2}} \gg \frac{g_{m1}R_{F2}}{C_{m1}(R_{F1} + R_{F2})} \quad (2)$$

By using the proposed body biasing circuit, the gain and output swing for every gain stage can be optimised for the supply voltage within 0.65–0.95 V. Simulation results show that this LDR has a DC loop gain of 80 dB, a unity-gain frequency of 100 kHz, and a phase margin larger than 60° for a supply voltage of 0.65–0.95 V.

Experimental results: This capacitor-free LDR has been fabricated in a 0.18 µm CMOS process. The die photo is shown in Fig. 2 and the active area is 290 × 420 µm. The measured maximum output current is 50 mA with a dropout voltage of 150 mV. The proposed LDR generates an output of 0.5 V for a supply voltage of 0.65–0.95 V. Its quiescent current is 12.72 µA for a supply voltage of 0.65 V. Fig. 3 shows the measured line and load regulations of this LDR. The measured line regulations for the output current $I_{OUT,min} = 0$ mA and $I_{OUT,max} = 50$ mA are 0.363 and 0.046%/V, respectively. In addition, the measured load regulation is 376.3 ppm/mA for a supply voltage of 0.65 V. Fig. 4 shows the measured transient response of the LDR with the output current switching from 0 to 50 mA for different supply voltages. When the supply voltage is decreased from 0.95 to 0.65 V, the output voltage dips are increased from 0.23 to 0.3 V, and the settling time is increased from 3 to 10 µs with an error less than 0.5%. The measured performance summary of the LDR is given in Table 1.

Fig. 4 Measured transient response for different supply voltages

Table 1: Measured performance summary

Process	0.18 µm CMOS	
Supply voltage (V_{IN})	0.65–0.95 V	
Output voltage	0.5 V	
Maximum output current	50 mA	
Dropout voltage	150 mV	
Quiescent current ($V_{IN} = 0.65$ V)	12.72 µA	
Line regulation	$I_{OUT} = 0$ mA	0.363%/V
	$I_{OUT} = 50$ mA	0.046%/V
Load regulation ($V_{IN} = 0.65$ V)	376.3 ppm/mA	
Settling time (at 0.5% error), Voltage dips	$V_{IN} = 0.95$ V	3 µs, 0.23 V
	$V_{IN} = 0.8$ V	6 µs, 0.24 V
	$V_{IN} = 0.65$ V	10 µs, 0.3 V
Active area	290 × 420 µm	

Conclusions: A sub-1 V CMOS capacitor-free LDR is presented. It has been fabricated in 0.18 µm CMOS process. This LDR operates from an ultra-low supply voltage of 0.65–0.95 V. Moreover, this LDR can be stable even when the output capacitor is eliminated. The experimental results confirm the proposed sub-1 V LDR.

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