0.5-V 5.6-GHz CMOS Receiver Subsystem

Hsiao-Chin Chen, *Member, IEEE*, Tao Wang, Hung-Wei Chiu,
Tze-Huei Kao, and Shey-Shi Lu, *Senior Member, IEEE*

Abstract—The building blocks of a 0.5-V receiver, including a receiver front-end and a low-pass filter (LPF), are fabricated using 0.18- μm CMOS technology. At 5.6 GHz, the receiver front-end achieves a voltage gain of 17.1 dB and a noise figure of 8.7 dB, while dissipating at 19.4 mW. The fifth-order low-pass Chebyshev filter achieves a corner frequency of 2.6 MHz and an input-referred noise of 28.5 nV/sqrt (Hz) at 6.8 mW. The receiver front-end is further integrated with the LPFs to form a highly integrated receiver subsystem at ultra-low voltage.

Index Terms—CMOS, direct conversion, front-end, local oscillator (LO) self-mixing, quadrature coupler (QC), receivers, subharmonic mixers, transformers.

I. INTRODUCTION

LATELY, CMOS technology has become very popular in the field of analog integrated circuits. Gate length shrinkage has caused transistor cutoff frequencies to rise to tens of gigahertz. This improvement favors the designs of CMOS circuit at high frequencies; meanwhile, manufacturers provide complete device libraries along with reliable high-frequency models. As CMOS RF gradually enters the mainstream of solid-state circuit design, the degree of integration of single-chip systems is effectively improved. However, to prevent transistors from fatal damage, the low voltage operation of circuits fabricated using modern CMOS technologies is crucial. RF/analog circuit designers definitely have to face serious challenges. This issue has drawn attention for a long time and many studies have focused on the low-voltage operation of RF/analog circuits [1]–[6]. These studies have successfully demonstrated the validity of using CMOS technology to implement ultra-low-voltage single-chip systems, encouraging the application of proposed techniques to other circuit topologies.

This study is concerned with the design of a 0.5-V subharmonic local oscillator (LO) pumped direct-conversion receiver for 5-GHz band wireless applications. Although the receiver

Fig. 1. Block diagram of receiver subsystem based on subharmonic-LO pumped architecture.

architecture has been demonstrated elsewhere [7], operating a system at 0.5 V is very challenging. Therefore, the receiver front-end developed elsewhere is newly modified herein to cope with ultra-low supply voltage. Based on leapfrog topology, a fifth-order low-pass Chebyshev filter is implemented with low-voltage operational transconductance amplifiers (OTAs), which employ standard transistors whose threshold voltage is reduced by forward-biasing the n-MOSFET bodies as performed elsewhere [4], [5]. Of priority concern is to increase the OTA unity-gain frequency, thus facilitating the use of the low-pass filter (LPF) in a broadband access system. The LPF is then incorporated with the RF front-end to demonstrate a highly integrated ultra-low-voltage receiver subsystem.

The remainder of this paper is organized as follows. Section II describes the receiver subsystem architecture. Section III discusses the circuit design of each building block. Section IV presents experimental results. Section V briefly summarizes the results of this study, along with recommendations for future research.

II. RECEIVER ARCHITECTURE

Fig. 1 shows a block diagram of a receiver subsystem based on subharmonic-LO pumped architecture. This receiver subsystem has a low-noise amplifier (LNA), a quadrature coupler (QC), a pair of subharmonic-LO pumped mixers (SHMs) and LPFs. The received signal is amplified by the single-ended LNA and then split into I/Q branches by the QC, which is a lump alternative to the 3-dB directional coupler [7]. On-chip transformers with stacked structures are designed to perform single-to-differential conversion in RF/LO paths and must be treated as components of impedance matching networks. Resistor-capacitor poly-phase shifters are adopted to generate the required LO signals of the doubly balanced SHMs.

Manuscript received July 25, 2008; revised November 21, 2008. First published January 09, 2009; current version published February 06, 2009. This work was supported by the National Science Council (NSC) of the R.O.C., Taiwan under Contract NSC 94-2215-E-002-032, Contract NSC 94-2218-E-002-045, and Contract NSC 97-2218-E-011-001.

H.-C. Chen is with the Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei 10617, Taiwan.

T. Wang and S.-S. Lu are with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan (e-mail: sslu@ntu.edu.tw).

H.-W. Chiu is with the Department of Electronic Engineering, National Taiwan University of Science and Technology, Taipei 10617, Taiwan.

T.-H. Kao is with Morning Star Semiconductor Inc., Chu-Pei 302, Taiwan.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TMTT.2008.2011165

Fig. 2. RF building blocks of receiver front-end.

III. CIRCUIT DESIGN

A. Receiver Front-End

Fig. 2 schematically depicts all of the RF building blocks, including the LNA, the directional coupler, and the SHMs [7], where all of the active devices are low-threshold-voltage MOSFETs, and each circuit can thus function well at ultra-low voltage. To prevent re-radiation, an *LC*-folded cascode configuration was utilized to obtain favorable reverse isolation without increasing the number of stacked transistors in the LNA. Additionally, a low-gain mode can be easily switched on by simply turning off the common-gate PMOS. As presented in Fig. 2, the *LC*-folded-cascode configuration is also incorporated into the SHM to achieve low-voltage operation and high LO self-mixing rejection. For direct conversion receivers, dc-offset at the mixer output is always a concern since it may cause considerable signal-to-noise ratio (SNR) degradation. However, using analog/digital calibration techniques to cancel dc offset that is induced by LO self-mixing is difficult because such an offset is dynamic. Therefore, SHM topology is adopted to eliminate the similarity between the frequencies of RF and LO in conventional direct-conversion receivers. Moreover, when an extra low-resistance path for out-of-resonance signals is offered, the bandpass characteristic of the *LC*-folded-cascode configuration favors an SHM more than does a conventional mixer in terms of LO-to-RF isolation, which makes the proposed SHM highly suited to direct-conversion receivers. To prevent an increase in system complexity and power consumption, the directional coupler was designed for IQ generation in the RF signal path, in preference to the use of octet-phase generation in sub-harmonically pumped LO signals to achieve I/Q receiver outputs. Fig. 2 presents the lump equivalent circuit of the directional coupler. The main elements of the coupler are two interleaved inductors, which provide the required inductance and capacitance to support a compact design.

B. LPF

A fifth-order low-pass Chebyshev filter is designed on the basis of leap-frog topology, as shown in Fig. 3. This LPF is constructed from ultra-low-voltage OTAs. Fig. 4 schematically depicts the OTA. Low threshold-voltage transistors are not used; instead, the bodies of the n-MOSFETs are forward biased to reduce the threshold voltage, while a low biasing level (0.1 V) is applied to bias the bodies of p-MOSFETs for the same purpose. Initially, a two-stage OTA topology proposed elsewhere [4] was adopted, but it was later modified, as shown in Fig. 4. In this study, the forward-biased nMOS-bodies of the OTA 1st stage are separated from bodies of the OTA second stage. The reason for this modification will be explained later.

The ultra-low supply voltage limits the use of traditional biasing methods, and therefore, active feedback loops are required to apply stable body biases to the OTAs. First, an inverter with a fixed switching threshold of 0.25 V is designed; it serves as an error amplifier (or voltage comparator) in the feedback loops [4]. The inverter output reflects the difference between the input voltage and the 0.25-V switching threshold. To achieve a fixed switching threshold of 0.25 V, a *V_{amp}*, which is a voltage generated by the circuit block shown in Fig. 5, is applied to the nMOS bodies in the inverters. Through a negative feedback loop formed from three identical inverters, the switching threshold is accurately set to 0.25 V. When other replica inverters are biased with this *V_{amp}*, they also act like error amplifiers with a switching threshold of 0.25 V.

The biasing circuit for nMOS bodies in the OTA is formed from a feedback loop, presented elsewhere [4], as shown in Fig. 6, in which an external 0.4-V reference voltage is applied to a replica OTA as an input common-mode voltage. The biasing circuit is based on a master-slave architecture, where the bias condition of the master circuit (the replica OTA) is effectively controlled by the negative feedback loop, which is shown in Fig. 6. The nMOS bodies of the OTA are then biased at the nMOS body bias voltage of the replica OTA. Theoretically, the

Fig. 3. Low-voltage fifth-order low-pass Chebyshev filter.

Fig. 4. Schematic of the two-stage operational amplifier.

Fig. 5. nMOS body biasing circuit for error amplifiers.

Fig. 6. Negative feedback route in two-stage OP using a single nMOS body biasing circuit.

output dc common-mode voltage of the original OTA (slave circuit) is set to the desired value (0.25 V) if the two OTAs match each other [4].

Careful consideration of the biasing circuit reveals the existence of a positive feedback loop, as illustrated by Fig. 7. A small increase in the body bias may reduce the output dc common-mode voltage of the OTA first stage and increase the output dc common-mode voltage of the OTA second stage, increasing the body bias. Although the output dc common-mode

voltage of the OTA can be set to the desired value using the negative feedback loop that is shown in Fig. 5, the inadequate dc common-mode voltage at the output of the first stage can cause the OTA to malfunction.

In this study, the nMOS body biases in the first and second stages are separated, as shown in Fig. 8, to prevent the OTA from the previously described malfunction. Fig. 9(a) and (b) displays biasing circuits of nMOS bodies in the first stage and the

Fig. 10. Die photograph of receiver subsystem.

Fig. 11. Measured and simulated S_{11} curves of receiver front-end.

imbalances are very sensitive to complex port impedances, the discrepancies between the measured and simulated phases [see Fig. 12(a)] exceed those between measured and simulated magnitudes [see Fig. 12(b)].

The input transistor size ($100\ \mu\text{m}/0.24\ \mu\text{m}$) of the LNA and the SHMs is determined using Lee's power-constrained noise optimization method [8]. Fig. 13 plots the measured and simulated noise figures with RF centered at 5.6 GHz. The circuit was designed using the noise parameters of the $0.18\text{-}\mu\text{m}$ mixed-mode CMOS process obtained from the United Microelectronics Corporation (UMC), where only the thermal noise is included. Therefore, the characteristics of the simulated and measured NF curves do not match closely below 1 MHz due to the lack of flicker noise in device modeling. At a baseband frequency of 20 MHz, the simulated and measured spot noise figures are 7.6 and 8.7 dB, respectively. This 1.1-dB discrepancy may result from the inaccuracy in the model of the thermal noise of low threshold-voltage transistors and the underestimated losses of passive elements over the band of interest.

The LPF is tested on a printed-circuit board (PCB). The power consumption of the LPF is 6.8 mW. Fig. 14 plots the measured frequency responses of the LPF, and a corner frequency of 2.6 MHz is observed. As shown in Fig. 3, the two marked resistors of the LPF are implemented using external resistors. Varying their values from 1 M Ω to 4.7 K Ω enables the LPF to deliver a voltage gain from 0 to 9.7 dB.

In this study, input NMOS transistor sizes of $285\ \mu\text{m}/0.54\ \mu\text{m}$ and $380\ \mu\text{m}/0.36\ \mu\text{m}$ are selected in the first and second stages

Fig. 12. Measured and simulated I/Q: (a) phase and (b) amplitude imbalances at baseband outputs of receiver front-end. (Accuracies of measurement of magnitude and phase are 0.2 dB and 0.0001° , respectively.)

of the two-stage OTA, respectively. Therefore, the input transistor transconductance (gm) of the two-stage OTA is large enough to achieve low input referred noise and a high gain-bandwidth product. The measured input-referred noise of the LPF is 28.5 nV/sqrt(Hz). The low input-referred noise and the corner frequency of 2.6 MHz indicate that the 0.5-V LPF is suitable for broadband access systems. Table I summarizes the performance of the realized ultra-low-voltage CMOS RF/analog circuits.

Table II presents the performance of the 0.5-V receiver front-end and those previously reported elsewhere for comparison. Although the receiver front-end operates at a higher

Fig. 13. Measured and simulated noise figures of receiver front-end.

Fig. 14. Measured frequency response of LPF.

TABLE I
SUMMARY OF 0.5-V CIRCUITS

Front-End	
Freq.	5.6 GHz
Power	19.4 mW
I/Q error* (5.5 ~ 5.8 GHz)	< 0.8 dB / < 0.7°
S11	-12.1 dB
Av	17.1 dB
NF	8.6 dB
IIP3	-17.9 dBm
LOR	43.3 dB
LO leakage	-60.3 dBm
2XLO leakage	-84.2 dBm
LPF	
Power	6.8 mW
Bandwidth	2.6 MHz
Gain range	0-10 dB
Input referred noise	28.5 nV/sqrt(Hz)
In-band IIP3	-26.33 dBV

*: Magnitude and phase measurement accuracies are 0.2 dB and 0.0001 degree, respectively.

frequency, it has a lower noise figure than in two other studies [3] and [5]. Moreover, it employs *LC*-folded cascode SHMs to reduce LO self-mixing. The achieved LO-to-RF leakage of -60.3 dBm and LO signal rejection of 43.3 dB yield an input-referred dynamic dc offset of -103.6 dBm, which is below the wireless local area network (WLAN) receiver input noise floor (-100.9 dBm), when a 20-MHz bandwidth is considered.

TABLE II
COMPARISON WITH PREVIOUSLY REPORTED 0.5-V CIRCUITS

Item	Our work	[3]	[5]
Freq.	5.6 GHz Rx Front-end	0.9 GHz Rx Front-end	2.4 GHz Rx
Power	19.4 mW	7.4 mW	8 mW
I/Q error	< 0.8 dB < 0.7°	NAV	NAV
S11	-12.1 dB	-26dB**	NAV
Av	17.1 dB	12 dB	~ 50 dB
NF	8.6 dB	9.0 dB	~ 18 dB
IIP3	-17.9 dBm	-14 dBm	~ -22 dBm
LOR	43.3 dB	0 dB	0 dB
LO leakage	-60.3 dBm	NAV	NAV
2XLO leakage	-84.2 dBm	NAV	NAV

** : off-chip matching

Fig. 15. Measured frequency response of receiver sub-system.

The 0.5-V receiver subsystem comprising the receiver front-end and the LPFs is also tested on a PCB. Since the bond-wires and metal traces on PCBs affect the input impedance, off-chip surface mount devices (SMDs) were used to obtain 50-Ω impedance matching. Fig. 15 plots the measured frequency response of the 0.5-V receiver subsystem; the corner frequency is 1.6 MHz.

Notably, the 0.5-V receiver subsystem and the circuits in other studies [3]–[5] may suffer from a critical problem. Since supply voltage scaling depends on reducing the threshold voltage, the bodies of MOS transistors are forward biased and some circuits include low threshold-voltage devices, exponentially increasing the leakage current. Even when the transistors are turned off, the current leaks through them and the static power is significantly increased.

V. SUMMARY

This study describes the feasibility of ultra-low-voltage CMOS RF/analog circuits. The OTA design technique proposed in another study [4] was improved by preventing the potential OTA malfunction. The LPF implemented with this newly modified OTA exhibits a low input-referred noise spectral density of 28.5 nV/sqrt(Hz) and a corner frequency of 2.6 MHz. The RF design technique proposed elsewhere [7] is proven to be feasible for use in ultra-low-voltage system-on-chip (SOC) since the presented receiver front-end has a higher frequency,

a larger gain, and a lower noise figure than those in earlier studies. A 0.5-V receiver subsystem, comprising the receiver front-end and the LPFs, is demonstrated using 0.18- μm CMOS technology.

ACKNOWLEDGMENT

The United Microelectronics Corporation (UMC), Hsin-Chu, Taiwan, is appreciated for its assistance with chip fabrication, as well as Nano Device Laboratories, Hsin-Chu, Taiwan, for its assistance with on-wafer measurements. T. Knoy is appreciated for his editorial assistance.

REFERENCES

- [1] M. Harada, T. Tsukahara, J. Kodate, A. Yamagishi, and J. Yamada, "2-GHz RF front-end circuits in CMOS/SIMOX operation at extremely low voltage of 0.5 V," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 2000–2004, Dec. 2000.
- [2] M.-N. El-Gamal, K.-H. Lee, and T.-K. Tsang, "Very low-voltage (0.8 V) CMOS receiver front-end for 5 GHz RF applications," *Proc. Inst. Elect. Eng.—Circuits Devices Syst.*, vol. 149, no. 516, pp. 355–362, Oct./Dec. 2002.
- [3] N. Stanić, P. Kinget, and Y. Tsividis, "A 0.5 V 900 MHz CMOS receiver front end," in *IEEE VLSI Circuits Symp. Tech. Dig.*, Jun. 2006, pp. 228–229.
- [4] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2373–2387, Dec. 2005.
- [5] N. Stanić, A. Balankutty, P. Kinget, and Y. Tsividis, "0.5-V analog circuit techniques and their application in OTA and filter design," in *IEEE RFICs Symp.*, Jun. 2007, pp. 2373–2387.
- [6] X.-P. Yu, M.-A. Do, J.-G. Ma, W.-M. Lim, K.-S. Yeo, and X.-L. Yan, "Sub-1 V low power wide range injection-locked frequency divider," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 7, pp. 528–530, Jul. 2007.
- [7] H.-C. Chen, T. Wang, and S.-S. Lu, "A 5–6 GHz 1-V CMOS direct-conversion receiver with an integrated quadrature coupler," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1963–1975, Sep. 2007.
- [8] T. Lee, *The Design of CMOS RF IC*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004, ch. 12.

Hsiao-Chin Chen (M'07) was born in Taipei, Taiwan, on Oct. 6, 1976. She received the B.S. and M.S. degrees in electrical engineering and Ph.D. degree in electronics engineering from National Taiwan University, Taipei, Taiwan in 1998, 2000, and 2007, respectively, from National Taiwan University, Taipei, Taiwan in the summer of 2007.

From 2000 to 2003, she was with the Airoha Technology Corporation, as a Circuit-Design Engineer. She then joined the Department of Electrical Engineering, National Taiwan University of Science

and Technology, where she is currently an Assistant Professor.

Her research interests are in the area of CMOS RF integrated circuits for wireless communications.

Tao Wang was born in Taipei, Taiwan, in 1980. He received the B.S. degree in electronics engineering from Chang Gung University, Taoyuan, Taiwan, in 2002, and the M.S. degree in electronics engineering and Ph.D. degree in electronics engineering from National Taiwan University, Taipei, Taiwan, in 2004 and 2008, respectively.

He is currently serving in the Chinese Army. His research interests are in the areas of RF integrated circuits and micromachined RF components.

Hung-Wei Chiu was born in Taipei, Taiwan, in 1976. He received the B.S. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 1998, and the M.S. and Ph.D. degrees from National Taiwan University, Taipei, Taiwan, in 2000 and 2003, respectively, all in electrical engineering.

In 2004, he joined the Taiwan Semiconductor Manufacturing Company (TSMC), as a Designer with the Mixed-Mode and RF Library Division. Since then, he has been involved in the area of the automation of mixed-mode and RF circuit design.

In August 2005, he joined the Department of Electronic Engineering and Graduate Institute of Computer and Communication Engineering, National Taipei University of Technology, Taipei, Taiwan, where he is currently an Assistant Professor.

Tze-Huei Kao was born in Taipei, Taiwan, in 1981. She received the B.S. degree and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2003 and 2006, respectively.

In 2006, she joined Morning Star Semiconductor Inc., Chu-Pei, Taiwan, where she is currently a Circuit Design Engineer. Her research interests are in the areas of analog baseband circuits for wireless communications and power electronics.

Shey-Shi Lu (S'89–M'91–SM'99) was born in Taipei, Taiwan, on October 12, 1962. He received the B.S. degree from the National Taiwan University, Taipei, Taiwan, in 1985, the M.S. degree from Cornell University, Ithaca, NY, in 1988, and the Ph.D. degree from the University of Minnesota at Minneapolis–St. Paul, in 1991, all in electrical engineering. His M.S. thesis concerned the planar doped barrier hot electron transistor. His doctoral dissertation concerned the uniaxial stress effect on the AlGaAs/GaAs quantum well/barrier structures.

In August 1991, he joined the Department of Electrical Engineering, National Taiwan University, where he is currently a Professor. Since August 2007, he has also served as the Director of the Graduate Institute of Electronics Engineering, National Taiwan University. His current research interests are in the areas of RF integrated circuit (RFIC)/monolithic microwave integrated circuits (MMICs), and micromachined RF components.