A 0.7–2-GHz Self-Calibrated Multiphase Delay-Locked Loop

Hsiang-Hui Chang, *Student Member, IEEE*, Jung-Yu Chang, *Student Member, IEEE*,
Chun-Yi Kuo, *Student Member, IEEE*, and Shen-Iuan Liu, *Senior Member, IEEE*

Abstract—A 0.7–2-GHz precise multiphase delay-locked loop (DLL) using a digital calibration circuit is presented. Incorporating with the proposed digital calibration circuit, the mismatch-induced timing error among multiphase clocks in the proposed DLL can be self-calibrated. When the calibration procedure is finished, the digital calibration circuit can be turned off automatically to save power dissipations and reduce noise generations. A start controlled circuit is proposed to enlarge the operating frequency range of the DLL. Both the start-controlled circuit and the calibration circuit require an external reset signal to ensure the correctness of the calibration after temperature, operating frequency, and power supply voltage are settled. This DLL with the digital calibration circuit has been fabricated in a 0.18- μm CMOS process. The measured results show the DLL exhibits a lock range of 0.7–2 GHz while the peak-to-peak jitter and rms jitter is 18.9 ps and 2.5 ps at 2 GHz, respectively. When the calibration procedure is completed and the DLL operates at 1 GHz, the maximum mismatch-induced timing error among multiphase clocks is reduced from 20.4 ps (7.34 degree) to 3.5 ps (1.26 degree).

Index Terms—Delay-locked loop (DLL), calibration, multiphase.

I. INTRODUCTION

DELAY-LOCKED LOOPS (DLLs) have been widely used in clock synchronization [1]–[3], clock multiplication [4], [5], and clock and data recovery circuits (CDRs) [7]. When the DLL is locked to the external clock, the delay time of the voltage controlled delay line (VCDL) may be equal to the multiple clock periods. However, it does not guarantee that each delay stage has the identical delay time due to process and voltage and temperature (PVT) variations. For clock multiplication circuits using edge-combining schemes [4], [5], the mismatch-induced timing error among delay stages will induce the fixed pattern jitter at the multiplied clock output. Similarly, a CDR using multiphase sampling schemes [6]–[8], the phase accuracy of the multiphase clocks will limit the jitter performance and the bit error rate. Unequal phase spacing will decrease the timing margin of the clocking system and produce a huge amount of unwanted jitter at outputs. With advances in CMOS technologies, the gate length of MOS devices is continuously shrinking to raise the operating speed and increase the integration. However, the accom-

panying device mismatch will induce timing errors to become the bottleneck of the high-speed synchronization circuits.

Many researches aim to reduce the mismatches among delay cells in a DLL or PLL [9], [11]–[13]. One of the solutions to reduce the mismatch is to increase the transistor size. However, parasitic capacitance will increase. When the clocking speed increases, the delay cell with minimum channel lengths may be chosen for the sake of higher speed. Such a delay cell suffers from poor matching which may induce significant timing errors among delay cells. Moreover, the clock buffers are needed to distribute the outputs of the VCDL to the whole system. Inevitably, the wiring or threshold mismatch from clock buffers will induce timing skews. In addition, in order to barely interfere with the main DLL, the loop bandwidth of the calibration circuit should be much smaller than that of the main DLL. Consequently, a large amount of on/off-chip capacitors is required if the calibration circuit operates in the analog domain [9]–[11].

In this paper, a digitally self-calibrating multiphase DLL is presented to generate precise multiphase clocks against PVT variations. Moreover, when the calibration procedure is finished, the digital calibration circuit will be turned off automatically to save power dissipations and reduce noise influences. Due to the finite digital quantization error, the calibrated phase error will be inevitably larger than that of the analog approaches [9], [10]. But the proposed digital calibration circuit with almost no analog extensions will promote cost-effective integration with other circuits or migration over different processes. Moreover, with benefits from scaling CMOS technologies, the digital calibration circuit has a lower supply voltage and the potential for good power-management.

This paper is organized as follows. The digital calibration algorithm is introduced in Section II. The architecture and detail circuits of the proposed self-calibrated multiphase DLL are described in Section III. The measured results are demonstrated in Section IV. The conclusions are given in Section V.

II. DIGITAL CALIBRATION ALGORITHM

Fig. 1 shows a conventional multiphase DLL composed of N delay cells and $N + 1$ output buffers. The total delay of the VCDL is locked to the multiple periods of the external clock, T_{clock} . The multiphase clocks are easily generated from output buffers. In order to maximize the effective sampling rate, the multiphase DLL is desired to lock the delay which is equal one clock period. Assume that $T_{\text{cell}}(i)$ is the delay time of the i th delay cell, $B(i)$ is the delay time of the i th output buffer, and N is the number of delay stages. Ideally, when the DLL achieves

Manuscript received April 7, 2005; revised February 1, 2006. The work of H.-H. Chang was supported in part by MediaTek Inc. and a MediaTek Fellowship.

The authors are with the Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10617, R.O.C. (e-mail: lsi@cc.ee.ntu.edu.tw).

Digital Object Identifier 10.1109/JSSC.2006.874036

Fig. 1. Multiphase DLL with N delay cells and $N + 1$ output buffers.

lock state, the timing relationships among the output buffers corresponding to different delay cells should be satisfied with the following two equations:

$$\sum_{i=1}^N T_{\text{cell}}(i) + B(N) - B(0) = T_{\text{clock}} \quad (1)$$

and

$$T_{\text{cell}}(i) + B(i) - B(i-1) = \frac{T_{\text{clock}}}{N}, \quad (i = 1 \sim N). \quad (2)$$

Equation (2) indicates the phase spacing among buffer outputs will be equal without any mismatch existing among delay cells and output buffers. Unfortunately, in practice, each delay cell or output buffer may introduce different delay time due to device mismatch or wiring mismatch. The equal phase spacing at outputs is impossible without any calibration mechanism. Fig. 2 shows 1000 points Monte-Carlo simulation results for static timing errors among $N (= 5)$ delay cells, where the input frequency is 2 GHz and 0.1 V threshold voltage mismatch of the delay cells are added (they will be discussed in the following section). In our 0.18- μm CMOS technology, the threshold voltage mismatch of 0.1 V for the delay cells will cause the delay time mismatch of 40 ps.

The operation of the proposed digital calibration circuit is shown in Fig. 3 where N is 5 in our work. The operation principle is similar to [11]. The relative phase comparison can mitigate the dependency of the absolute value of two successive phases. Since the proposed calibration circuit performs the phase comparison in the digital domain, the quantization error, q_e , is unavoidable. $d(i)$ represents the relative phase error among $(i-1)$ th, i th, and $(i+1)$ th clock outputs and it can be expressed as

$$d(i) = [B(i) + T_{\text{cell}}(i) - B(i-1)] - \{B[\text{mod}_N(i+1)] + T_{\text{cell}}[\text{mod}_N(i+1)] - B[\text{mod}_N(i)]\} \quad (3)$$

where $\text{mod}_N()$ represents the signed remainder after division by N . If the absolute value of $d(i)$ larger than q_e , the digitally relative phase detector (DRPD) will output an “up” or

Fig. 2. Delay time mismatch due to the delay cell with the threshold voltage mismatch of 0.1 V @ 2 GHz.

“down” signal. It digitally updates $B(i)$ or $T_{\text{cell}}(i)$, by a unit time step, Δt . In order not to influence the main loop operation, the method to adjust $B(i)$ is preferred. The updated relative phase error can be expressed as $d(i) \pm \Delta t$ where the negative sign denotes that the DRPD outputs an “up” signal and vice versa. If the absolute value of $d(i)$ is smaller than q_e , the phase of the i th clock, ck_i , will not be changed whether $d(i)$ is positive or negative. This digital calibration circuit will correct the phase error by adjusting $B(i)$, where $i = 1 \sim N$, sequentially. In every N calibration cycle, the delay time of the N th output buffer, $B(N)$, may be changed. According to (1), the main loop will correct the phase error by changing the delay time of the VCDL. Assume the updated phase error will be equally compensated to each delay cell in the VCDL. The relative phase error $d(i)$ can be expressed as

$$\begin{aligned} & \left[B(i) + T_{\text{cell}}(i) \pm \frac{\Delta t}{N} - B(i-1) \right] \\ & - \left\{ B[\text{mod}_N(i+1)] + T_{\text{cell}}[\text{mod}_N(i+1)] \right. \\ & \quad \left. \pm \frac{\Delta t}{N} - B[\text{mod}_N(i)] \right\} \pm k_i \Delta t = d(i) \pm k_i \Delta t \quad (4) \end{aligned}$$

where k_i is an integer and Δt is a unit time step. When the calibration procedure is finished, all the absolute values of $d(i)$ are no more than the quantization error, q_e , i.e.,

$$|d(i) \pm k_i \Delta t| \equiv |e(i)| \leq q_e, \quad i = 1 \sim N. \quad (5)$$

For our work with $N = 5$ and substituting (5) into to (3), we can get

$$e(1) + e(2) + e(3) + e(4) + e(5) = 0. \quad (6)$$

Fig. 3. Operation of the proposed calibration circuit.

Combining (1), (5), and (6), the maximum phase spacing between the i th and $(i-1)$ th buffer outputs deviated from the ideal value for all delay cells and output buffers is

$$\begin{aligned} \text{MAX}_{i=1 \sim 5} \left[B(i) + T_{\text{cell}}(i) - B(i-1) - \frac{T_{\text{clock}}}{5} \right] \\ = \left| \frac{4e(1) + 3e(2) + 2e(3) + e(4)}{5} \right| \leq \frac{6}{5}q_e \quad (7) \end{aligned}$$

where $\text{MAX}_i()$ represents maximum value. The absolute maximum phase error between the i th buffer output and the output of the buffer B_0 deviated from the ideal value is given by

$$\text{MAX}_{i=1 \sim 4} \left[B(i) + \sum_{k=1}^i T_{\text{cell}}(k) - B(0) - \frac{T_{\text{clock}}}{5} \cdot i \right] \leq \frac{8}{5}q_e. \quad (8)$$

In order to make the digital calibration totally independent of the main DLL and reduce the hardware complexity, the control codes of the last stage output buffers can be fixed. By doing so, the cost is that (6) will not hold since only $B(i)$, where $i = 1 \sim 4$, is adjusted. The maximum phase spacing between two buffer outputs deviated from the ideal value is increased as

$$\left| \frac{4e(1) + 3e(2) + 2e(3) + e(4)}{5} \right| = 2q_e. \quad (9)$$

Similarly, to satisfy (1), (5), and (9), the absolute maximum phase error between the i th buffer output and the output of the buffer B_0 deviated from the ideal value is given by

$$\text{MAX}_{i=1 \sim 4} \left[B(i) + \sum_{k=1}^i T_{\text{cell}}(k) - B(0) - \frac{T_{\text{clock}}}{5} \cdot i \right] \leq 3q_e. \quad (10)$$

Fig. 4 shows the behavioral simulation results, where $N = 5$, $T_{\text{clock}} = 500$ ps, $q_e = 5$ ps, $\Delta t = 5$ ps, and 20% random delay time mismatches are added. In these two methods, the calibration procedure is converged and the maximum phase spacing deviated from the ideal value of 100 ps is less than the boundary of 6 ps and 10 ps, respectively. The results are confirmed with (7) and (9), respectively.

III. CIRCUIT DESCRIPTIONS

The proposed multiphase DLL is composed of the phase detector (PD), the start controlled circuit, the charge pump (CP),

Fig. 4. Behavioral simulation results of the calibration procedure. (a) Case 1: the control codes of the last stage output buffer are not fixed. (b) Case 2: the control codes of the last stage output buffer are fixed.

a capacitor as the first-order loop filter, the five-stage VCDL, six digitally controlled output buffers (DCOBs), and the digital calibration circuit as shown in Fig. 5. The delay time of a

Fig. 5. Proposed self-calibrated multiphase DLL.

DCOB can be digitally adjusted by the binary-weighted control codes which are generated by the digital calibration circuit. According to the simulation results in Fig. 2, the delay range of every DCOB should be larger than 40 ps to compensate the delay mismatches. The number of control bits is set to 4. In order to make the digital calibration circuit operation totally independent of the main DLL and reduce the hardware complexity, the control codes of the last DCOB are fixed.

The operation of the proposed DLL can be explained as follows.

A. Delay Cell and DCOB

The bandwidth of the delay cell trades off both variable delay range and power dissipations. The delay cell with both wide bandwidth and large tuning range is required for the high frequency operation. The delay cell adopted in this work is similar to [14] as shown in Fig. 6. The VCDL is composed of five delay units. Each delay unit is composed of two delay cells. By adjusting the transconductance of the PMOS transistors, M7 and M8, the delay time of the delay cell can be varied. The PMOS transistors, M5 and M6, enlarge the tuning range. The cross-coupled pair, M3 and M4, ensures the waveforms at outputs to be fully differential.

The DCOBs distribute the multiphase clocks from the VCDL to the whole system and they can be controlled digitally to compensate the phase imbalances. Fig. 7 shows the DCOB which consists of inverters and varactors [15]. The delay time of a DCOB is varied by switching digitally two sets of varactor arrays at the outputs of first and second inverters, respectively. Each varactor array is composed of four identical varactors [15] with binary-weighted controlled. By so doing, capacitive loading at each output can be mitigated. Two small inverters

Fig. 6. Delay cell.

ensure the outputs to be differential. The last inverter provides enough driving capability for the DCOB. According to the results in Fig. 2, the variable delay range of the DCOB is larger than 40 ps and the characteristic is monotonously increasing.

B. Phase Detector

Low-jitter DLLs use commonly the linear PD or phase frequency detector (PFD) for the phase acquisition. However, when the clocking rate increases, the linear PD or PFD will limit the operating frequency of the DLL. Adding the dividers in front of the PD may mitigate this problem, however, the unequal delay time between the dividers will generate a significant static phase offset at the locked state. The bang-bang PD, implemented by a current-mode-logic D-flip-flop (CML DFF), is used in this work as shown in Fig. 8. The DFF actually operates at two different modes (i.e., band-band region and linear region) corresponding to the phase difference between

Fig. 7. Digitally controlled output buffer (DCOB).

Fig. 8. Bang-bang PD.

Fig. 9. Characteristics of a bang-bang PD.

Fig. 10. Start controlled circuit (single-ended version).

input and output clocks as shown in Fig. 9. When the zero crossings of input and output clocks are very close, the PD will produce an unsaturated output due to the metastability and the characteristic of the DFF. The random phase difference resulting from jitter may lead the PD to produce an incorrect voltage level. There is the possible randomness in the circuit behavior; however, the averaged results are used [16], [17]. From Fig. 9, the linear region of this bang-bang PD can be determined as [16], [17]

$$\Delta\varphi_{\max} = \frac{V_{\text{logic}}}{V_p} \exp \frac{-T_{\text{clock}}}{\tau_{\text{latch}}} \quad (11)$$

where V_{logic} is the voltage required for reliable recognition of the digital state, V_p is the amplitude of the clock, g_{m3} is the transconductance of M3 (M4) in Fig. 8, and $\tau_{\text{latch}} (= R_L C_L / (g_{m3} R_L - 1))$ is the regeneration time constant. To ensure the PD to operate linearly when the DLL nearly locks to the external clock, the maximum phase adjustment within one clock period should be

$$\Delta\varphi_{\text{update}} = K_{\text{VCDL}} \frac{I_{cp}}{C_L} < \Delta\varphi_{\max} \quad (12)$$

Fig. 11. Charge pump.

Fig. 12. Block diagram of the digital calibration circuit.

where K_{VCDL} is the gain of the VCDL, I_{CP} is the charge pump current, and C_L is the capacitance of the loop filter. Since $V_{logic} = 0.5 V_p$, $\tau_{latch} = 8.7$ ns, $K_{VCDL} = 325$ ps/V, $I_{CP} = 100$ μ A and $C_L = 42$ pF in this work, it gives $\Delta\varphi_{max} = 38$ ps and $\Delta\varphi_{update} = 0.4$ ps.

C. Start-Controlled Circuit

Fig. 10 shows the start controlled circuit. For a multiphase DLL, the total delay time of the VCDL is desired to be equal to one clock period in order to maximize effective sampling rate. To operate at high frequency, the delay cell with wide bandwidth is needed, but it may limit the maximum delay time. Furthermore, if the minimum delay time of the VCDL is less than half of T_{clock} , the DLL falls into false locking [3]. The start-controlled circuit allows the DLL not to fall into false locking and increases the operating frequency range.

Initially, the VCDL is set to the minimum delay. Before the first transition of the PD output, q , arrived, the signal *normal* is low. The start controlled circuit will force the CP circuit to charge the loop filter. The CP circuit is shown in Fig. 11. It increases the delay time of the VCDL continuously until the

Fig. 13. Timing signals generated by the timing control circuit.

first transition of the PD output is detected. After that, *normal* will go high. The CP circuit normally charges or discharges the loop filter according to the PD output and turned off unused circuits automatically. Thus, the proposed start controlled circuit prevents the DLL from false locking even when the minimum delay time of the VCDL is shorter than $0.5T_{clock}$. By using the start-controlled circuit, the operating frequency range of the DLL is extended as

$$T_{VCDL,MIN} < T_{clock} < T_{VCDL,MAX} \quad (13)$$

where $T_{VCDL,MIN}$ and $T_{VCDL,MAX}$ represents the minimum and maximum delay time of the VCDL, respectively. If the change in temperature, operating frequency, or power supply is so large that the loop fails to lock, the start-controlled circuit requires an external signal to reset the loop.

Fig. 14. Digital phase selector (DPS).

D. Digital Calibration Circuit

When the main DLL in Fig. 5 is locked, the delay time between $CK0\pm$ and $CK5\pm$ will be equal to T_{clock} . Then, the mismatch-induced timing errors among delay cells and DCOBs can be compensated by the digital calibration circuit as shown in Fig. 12. The calibration circuit can automatically operate in the background and barely interfere with the main DLL loop behavior. It consists of the digital phase selector (DPS), the digitally relative phase detector (DRPD), 4-bit UP/DOWN counters, the lock detector (LD), and the timing control circuit. Since the control bits of the first and last DCOBs are fixed, four calibration loops are generally needed. In this work, the calibration circuit only compensates the phase imbalances among the rising edges of the DCOBs. Four additional calibration loops can be added to response the falling edges of the DCOBs. In order to save power dissipations and the chip area, the calibration procedure will operate sequentially. The timing control circuit generates the required timing signals as shown in Fig. 13. In this design, $O5$ is the idle phase.

In Fig. 14, the DPS sequentially selects the successive three outputs of the DCOBs according to the timing signals, $O1 \sim O4$. Compared with the tree structure [18], this DPS reduces the latency and power dissipations. The dummy devices are added to balance the parasitic capacitances in the DPS.

After the DPS, the DRPD in Fig. 15 compares the relative phase errors among the selected signals, $S1 \sim S3$. The DRPD is composed of three interpolators [19], two DFFs, and some logic circuits. By using interpolators in Fig. 16 [19], the DRPD can perform the relative phase comparison in the digital domain and save a large amount of on/off chip capacitors. In Fig. 15, the signal $S22$ is generated by homo-interpolating of $S2$ while the signal $S13$ is generated by hetero-interpolating $S1$ and $S3$ with a precisely weighted factor of 50% [19]. When the zero crossing of $S13$ is very close to that of $S22$, the metastability of the DFF will lead the DRPD to output wrong signals to the UP/DOWN counter. Such the undetectable phase error can be considered as the quantization error, q_e . In this case, the DRPD should not update the state of the UP/DOWN counter. It can be resolved by adding another DFF and XOR gate as shown in Fig. 15. When the relative phase error is smaller than the quantization error, the signal $lockb$ will go low and freeze the state of the UP/DOWN counter. Fig. 17 shows the simulated characteristic of DRPD, where the undetectable phase error of the DRPD is around 5 ps, which is caused by the metastability of the DFF. If all values of the $lockb$, sampled by $C1$, $C2$, $C3$, and $C4$ sequentially, are low, the relative phase error among all the consecutive three outputs of the DCOBs will be smaller than the quantization error. And the calibration procedure will be accomplished. After $stop$ goes high, the LD will turn off the digital calibration circuit automat-

(a)

(b)

Fig. 20. Locked state of the proposed (a) DLL: 700 MHz; (b) DLL: 2 GHz.

(a)

(b)

Fig. 21. Measured jitter histograms of the proposed (a) DLL: 700 MHz; (b) DLL: 2 GHz.

proposed DLL when the input frequency is 700 MHz and 2 GHz, respectively. The maximum operating frequency is limited by the minimum delay time of VCDL while the minimum operating frequency is restricted by the maximum delay time of VCDL. From Fig. 20, the minimum delay time of the DLL is less than 500 ps. Thus, the proposed start-controlled circuit can prevent the DLL from false locking when the minimum delay time of the VCDL is shorter than $0.5T_{\text{clock}}$ and thus extend the operating frequency range. Fig. 21 depicts the measured jitter histogram when the DLL operates at 700 MHz and 2 GHz, respectively. When the input frequency is 2 GHz, the measured rms and peak-to-peak jitter is 2.5 ps and 18.9 ps, respectively. After *reset_cal* goes high, the calibration circuit will minimize the mismatch-induced timing error among multiphase clocks. Fig. 22(a) and (b) shows the measured maximum mismatch-induced timing error among multiphase clocks before and after calibration, respectively, when the proposed DLL operates at 1 GHz. Before the calibration, the averaged phase difference between *ck0* and *ck4* is 820.4 ps in Fig. 22(a). After the calibration, the one is reduced to be 796.8 ps in Fig. 22(b). Fig. 23 shows the measured mismatch-induced timing error among multiphase clocks. The maximum phase error among multiphase clocks is reduced from 20.4 ps (7.34 degree) to 3.5 ps (1.26 degree) when the DLL operates at 1 GHz. Table I gives the performance comparisons among the previous works and this one [20]. Due to the finite digital quantization error, the calibrated phase error is larger than that of the analog approaches [9], [10]. The active area of the proposed calibration circuit may be larger than analog approaches [9]–[11], [13]. But, a large amount of

(a)

(b)

Fig. 22. Measured maximum phase error among multiphase clocks of the proposed (a) DLL: before calibration (*reset_cal* is low); (b) DLL: after calibration (*reset_cal* is high).

TABLE I
COMPARISONS AMONG PREVIOUS WORKS

	[9]	[10]	[11]	[12]	[13]	This work
Process	0.35 μ m	0.25 μ m	0.18 μ m	0.6 μ m	0.35 μ m	0.18 μ m
Vdd	3V	2.5V	x	x	3.3V	1.8V
Operating frequency range	1.7~1.9 GHz	10~300 MHz	4~6 GHz	89MHz	130~165MHz	0.7~2 GHz
Effective sampling rate	3.4~3.8 GHz	0.08~2.4 GHz	8~12 GHz	2.85 GHz	1.3~1.65 GHz	3.5~10 GHz
Rms output jitter	x	1.95ps @250MHz	x	x	3.41ps @150MHz	2.45ps @2GHz,
Peak-to-Peak output jitter	x	16.7ps @250MHz	x	x	26.38ps @150MHz	18.9ps @2GHz
Calibration method	Analog	Analog	Analog	Digital	Analog	Digital
Before calibration Max. phase error	2.5° @1.8GHz	2.2° @125MHz	x	20% (DNL) @89MHz	22.8° @150MHz	7.34° @1GHz
After calibration Max. phase error	0.2° @1.8GHz	0.32° @125MHz	2° @5GHz	1% (DNL) @89MHz	6.1° @150MHz	1.26° @1GHz
Active area of calibration circuit	~0.16mm ²	x	0.12 mm ²	0.644 mm ²	~0	0.52 mm ²
Active area of whole circuit	0.48mm ²	1.6mm ²	4.5 mm ²	1.42 mm ²	2.25 mm ²	1.03 mm ²
Power	60mW	80mW @250MHz (Four designs)	2.7mW (with IQ generator only)	x	18mW (with I/O interfaces)	81mW @2GHz (with I/O interfaces)

x: not mentioned.

Fig. 23. Measured phase error among multiphase clocks.

on/off-chip capacitors is required if the calibration circuit operates in the analog domain [9]–[11]. Conversely, the proposed digital calibration circuit with almost no analog extensions will allow cost-effective integration with other circuits or migrated over different processes. Since the static CMOS logic circuits are used in the digital calibration circuit instead of the DRPD, the active area of the digital calibration circuit can be reduced significantly by using standard cell synthesis. Moreover, with benefits from scaling CMOS technologies, the digital calibration has a lower supply voltage and the potential for good power management.

V. CONCLUSION

In this paper, a 0.7–2-GHz precise multiphase DLL with the digital calibration circuit is presented. Using the digital calibration circuit, the mismatch-induced timing error among multiphase clocks can be reduced. A start-controlled circuit is also

proposed to prevent the DLL from false locking problem and extend the locking range. The proposed calibration circuit performed in the digital domain to save a large amount of on/off-chip capacitors. The proposed digital calibration approach is suitable for advanced CMOS technologies to reduce power dissipation and increase the maximum operating frequency.

ACKNOWLEDGMENT

The authors would like to thank Chip Implementation Center (CIC), Taiwan, for fabricating this chip. The authors would also like to thank the anonymous reviewers for their valuable comments and suggestions.

REFERENCES

- [1] R. B. Watson, Jr. and R. B. Ikaian, "Clock buffer chip with multiple target automatic skew compensation," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1267–1276, Nov. 1995.
- [2] C. H. Kim *et al.*, "A 64-Mbit, 640-Mbyte/s bidirectional data strobed, double-data-rate SDRAM with a 40-mW DLL for a 256-Mbyte memory system," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1703–1710, Nov. 1998.
- [3] Y. Moon, J. Choi, K. Lee, D. K. Jeong, and M. K. Kim, "An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance," *IEEE J. Solid-State Circuits*, vol. 35, pp. 377–384, Mar. 2000.
- [4] G. Chien and P. Gray, "A 900 MHz local oscillator using a DLL-based frequency multiplier technique for PCS applications," in *IEEE International Solid-State Circuits Conference*, Feb. 2000, pp. 202–203.
- [5] C. Kim, I.-C. Hwang, and S.-M. Kang, "A low-power small-area $\pm$ 7.28-ps-jitter 1-GHz DLL-based clock generator," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1414–1420, Dec. 2002.
- [6] X. Maillard, F. Devisch, and M. Kuijk, "A 900-Mb/s CMOS data recovery DLL using half-frequency clock," *IEEE J. Solid-State Circuits*, vol. 37, pp. 711–715, June 2002.
- [7] C.-K. K. Yang, R. Farjad-Rad, and M. A. Horowitz, "A 0.5- μ m CMOS 4.0-Gbit/s serial link transceiver with data recovery using oversampling," *IEEE J. Solid-State Circuits*, vol. 33, pp. 713–721, May 1998.
- [8] M. J. Lee, W. J. Dally, J. W. Poulton, P. Chiang, and S. E. Greenwood, "An 84-mW 4Gb/s clock and data recovery circuit for serial link applications," in *Symposium on VLSI Circuits*, 2001, pp. 149–152.

- [9] C. H. Park, O. Kim, and B. Kim, "A 1.8-GHz self-calibrated phase-locked loop with precise I/Q matching," *IEEE J. Solid-State Circuits*, vol. 36, pp. 777–783, May 2001.
- [10] L. Wu and W. C. Black, Jr., "A low-jitter skew-calibrated multi-phase clock generator for time-interleaved applications," in *International Solid-State Circuits Conference*, Feb. 2001, pp. 396–399.
- [11] S. H. Wang, J. Gil, I. Kwon, H. K. Ahn, H. Shin, and B. Kim, "A 5-GHz band I/Q clock generator using a self-calibration technique," in *28th European Solid-State Circuits Conference*, Sept. 2002, pp. 807–810.
- [12] F. Baronti, D. Lunardini, R. Roncella, and R. Saletti, "A self-calibrating delay-locked delay line with shunt-capacitor circuit scheme," *IEEE J. Solid-State Circuits*, vol. 39, pp. 384–387, Feb. 2004.
- [13] H. H. Chang, C. H. Sun, and S. I. Liu, "A low jitter and precise multiphase delay-locked loop using shifted averaging VCDL," in *International Solid-State Circuits Conference*, Feb. 2003, pp. 434–435.
- [14] W. S. T. Yan and H. C. Luong, "A 900-MHz CMOS low-phase-noise voltage-controlled ring oscillator," *IEEE Trans. Circuits and System II*, vol. 48, pp. 216–221, Feb. 2001.
- [15] A. Alvanpour, R. K. Krishnamurthy, D. Eckerbert, S. Apperson, B. Bloechel, and S. Borkar, "A 3.5 GHz, 32 mW 150 nm multiphase clock generator for high-performance microprocessors," in *IEEE International Solid-State Circuits Conference*, Feb. 2003, pp. 112–113, and 482.
- [16] B. Razavi, *Design of Integrated Circuits for Optical Communications*. : McGraw- Hill, 2003, pp. 297–298.
- [17] J. Lee, K. S. Kundert, and B. Razavi, "Analysis and modeling of bang-bang clock and data recovery circuits," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1571–1580, Sep. 2004.
- [18] A. Momtaz, C. Jun, M. Caresosa, A. Hairapetian, D. Chung, K. Vakilian, M. Green, T. Wee-Guan, J. Keh-Chee, I. Fujimori, and C. Yijun, "A fully integrated SONET OC-48 transceiver in standard CMOS," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1964–1973, Dec. 2001.
- [19] T. Saeki, M. Mitsuishi, H. Iwaki, and M. Tagishi, "A 1.3-cycle Lock time, non-PLL/DLL clock multiplier based on direct clock cycle interpolation for "clock on demand"," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1581–1590, Nov. 2000.
- [20] R. C. H. van de Beek, E. A. M. Klumperink, C. S. Vaucher, and B. Nauta, "Low jitter clock multiplication: a comparison between PLLs and DLLs," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, pp. 555–556, Aug. 2002.

Hsiang-Hui Chang (S'01) was born in Taipei, Taiwan, R.O.C., on February 4, 1975. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, in 1999, 2001, and 2004, respectively.

He is currently with Mediatek Inc., Hsinchu, Taiwan, R.O.C., working on wireless communication and consumer products. His research interests are PLL, DLL, and high-speed interfaces for gigabit transceivers.

Jung-Yu Chang (S'04) was born in Taipei, Taiwan, R.O.C., in 1980. He received B.S. degree in electric engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 2002. He is currently working toward the Ph.D. degree in electronics engineering, Taipei, Taiwan, R.O.C.

His research interests include high-speed CMOS circuit design such as phase-locked loops, delay-locked loops, and transceivers.

Chun-Yi Kuo (S'01) received his B.S. and M.S. degrees from Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, in 2002 and 2004, respectively.

He joined the RF Division, MediaTek Inc., Hsinchu, Taiwan, where he attended an intern project on RFIC design. After completing the compulsory military service, he is currently with Afa Technologies Inc. focusing on RF frequency synthesizer design. His research interest involves

mixed-signal/RF IC design for communication or signal processing applications. His previous works include CMOS PLL frequency synthesizers and SiGe BiCMOS voltage-controlled oscillators and prescalers.

Shen-Iuan Liu (S'88-M'93-SM'03) was born in Keelung, Taiwan, Republic of China, 1965. He received both the B.S. and Ph.D. degree in electrical engineering from National Taiwan University (NTU), Taipei, in 1987 and 1991, respectively.

During 1991–1993 he served as a second lieutenant in Chinese Air Force. During 1991–1994, he was an Associate Professor in the Department of Electronic Engineering of National Taiwan Institute of Technology. He joined in the Department of Electrical Engineering, NTU, Taipei, Taiwan in 1994

and he has been the Professor since 1998. His research interests are in analog and digital integrated circuits and systems.

Dr. Liu has served a chair on IEEE SSCS Taipei Chapter from 2004. He has served a general chair on the 15th VLSI Design/CAD symposium, Taiwan, 2004 and a Program Co-chair on the Fourth IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, Japan, 2004. He was the recipient of the Engineering Paper Award from the Chinese Institute of Engineers, 2003, the Young Professor Teaching Award from MXIC Inc., the Research Achievement Award from NTU, and the Outstanding Research Award from National Science Council, 2004. He served as a technical program committee member for A-SSCC and ISSCC, 2005. In 2006, he became an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS. He is a senior member of IEEE and a member of IEICE.