A High Quality Factor and Low Power Loss Micromachined RF Bifilar Transformer for UWB RFIC Applications

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Abstract—In this letter, the authors demonstrate that high quality factor and low power loss transformers can be obtained by using the CMOS process-compatible backside inductively coupled plasma (ICP) deep-trench technology to selectively remove the silicon underneath the transformers. A 62.4% (from 8.99 to 14.6) and a 205.8% (from 8.6 to 26.3) increase in the Q -factor, a 10.3% (from 0.697 to 0.769) and a 30.2% (from 0.652 to 0.849) increase in the maximum available power gain (G_{Amax}), and a 0.43- (from 1.57 to 1.14 dB) and a 1.15-dB (from 1.86 to 0.71 dB) reduction in the minimum noise figure (NF_{min}) were achieved at 5.2 and 10 GHz, respectively, for a bifilar transformer with overall dimension of $240 \times 240 \mu\text{m}^2$ after the backside ICP etching. The values of G_{Amax} of 0.769 and 0.849 are both state-of-the-art results among all reported on-chip bifilar transformers. These results indicate that the backside ICP deep-trench technology is very promising for high-performance radio frequency integrated circuit applications.

Index Terms—Inductively coupled plasma (ICP), isolation, power loss, quality factor, radio frequency integrated circuit (RFIC), transformer.

I. INTRODUCTION

IN THE DESIGN of low-voltage and high-performance CMOS radio frequency integrated circuits (RFICs) [1], [2], the power-gain (G_A) performance of the transformers used is crucial for the phase noise performance of the voltage-controlled oscillators (VCOs) and the noise figure (NF) performance of the low-noise amplifiers (LNAs). However, the G_A performance of the monolithic RF transformers fabricated on normal silicon substrates ($\sim 300 \mu\text{m}$) is usually not satisfactory mainly due to their capacitive and electromagnetic coupling with the silicon substrate. Various methods have been proposed to reduce the coupling-induced loss of RF passive devices, such as high-resistivity silicon [3], frontside and backside micromachining [4]–[7], porous silicon [8]–[10], proton implantation [11], patterned ground shields (PGS) [12], and substrate transfer [13], [14]. However, most of the proposed methods are very difficult, if not impossible, to be integrated into the standard

Fig. 1. (a) Top-view die photo of a bifilar transformer with a metal width of $10 \mu\text{m}$, a coil spacing (between the primary and the secondary coil) of $5 \mu\text{m}$, an inner dimension of $100 \times 130 \mu\text{m}^2$, and an overall dimension of $240 \times 240 \mu\text{m}^2$. (b) Process steps of the backside ICP deep-trench etching technology.

CMOS technology due to their inherent nonstandard CMOS-processing steps. For example, the classical micromachining techniques in [4]–[7] all include a wet-etching-process step, which is not compatible with the standard CMOS technology. Besides, the PGS method, while being compatible with the CMOS technology, has the drawbacks of limited improvement of the Q -factor and reduction of the self-resonant frequency. Fortunately, these problems can be improved to a large extent by our proposed backside inductively coupled plasma (ICP) deep-trench technology [15]. Compared with the traditional backside wet bulk micromachining in [6], the dry ICP etching has the advantages of forming vertical sidewalls and being fully CMOS-process compatible, since it is a standard processing technique in modern CMOS technology.

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TABLE I
DETAILED COMPARISON OF THE EXTRACTED PARAMETERS OF THE BIFILAR TRANSFORMERS IN [10] AND [13] AND THE BIFILAR TRANSFORMER IN THIS LETTER

	Transformer Structure	Overall Dimension (μm ²)	Technology	substrate resistivity (Ω·cm)	frequency (GHz)	Q ₁	Q ₂	k _{IM}	k _{Re}	x	G _{Amax}	NF _{min} (dB)		
K. Chong [10]	Thick (3.02 μm) Bifilar (on porous Si substrate)	280×280	NA	NA	5.2	9.1	9.1	0.75	0.38	1.83×10 ⁻²	0.764	1.17		
					8	6.69	6.69	0.825	0.665	1.81×10 ⁻²	0.765	1.16		
					10	2.36	2.36	0.9	0.9	3.58×10 ⁻²	0.687	1.63		
K. T. Ng [13]	Thin (0.85 μm) Bifilar (on normal Si substrate)	300×300	NA	10	5.2	2.857	2.619	0.623	0.6	1.96×10 ⁻¹	0.424	3.73		
					8	1.619	1.333	0.589	0.762	3.16×10 ⁻¹	0.342	4.66		
					10	1	0.571	0.43	0.73	7.3×10 ⁻¹	0.213	6.72		
	Thin (0.85 μm) (on quartz substrate)			∞	5.2	6.143	6.524	0.608	0.169	6.55×10 ⁻²	0.603	2.20		
					8	7.619	8.143	0.589	0.139	4.55×10 ⁻²	0.655	1.84		
					10	8	8.429	0.565	0.1	4.6×10 ⁻²	0.653	1.85		
This Work	Thin (0.99 μm) Bifilar (on normal Si substrate)	240×240	0.18 μm CMOS	10	5.2	8.99	8.9	0.54	0.464	3.3×10 ⁻²	0.697	1.57		
					8	9.44	9.34	0.515	0.571	2.81×10 ⁻²	0.716	1.45		
					10	8.6	8.49	0.456	0.525	4.63×10 ⁻²	0.652	1.86		
	Thin (0.99 μm) Bifilar (w/i backside ICP etching)				5.2	14.6	14.5	0.523	3.5×10 ⁻⁴	1.73×10 ⁻²	0.769	1.14		
					8	21.7	21.6	0.489	0.122	8.77×10 ⁻³	0.829	0.81		
					10	26.3	26.2	0.433	0.36	6.7×10 ⁻³	0.849	0.71		

$$[(R_M + j\omega L_M) \parallel \frac{1}{j\omega C_M}] = Z_{12} \text{ (or } Z_{21})$$

$$(1) \text{NF}_{\text{min}} = 10 \cdot \log\left(\frac{1}{G_{\text{Amax}}}\right)$$

$$(2) G_{\text{Amax}} = 1 + 2(x - \sqrt{x^2 + x}), \text{ in which}$$

$$x = \frac{\text{Re}(Z_{11})\text{Re}(Z_{22}) - [\text{Re}(Z_{12})]^2}{[\text{Im}(Z_{12})]^2 + [\text{Re}(Z_{12})]^2} = \frac{1 - k_{\text{Re}}^2}{k_{\text{Im}}^2 Q_1 Q_2 + k_{\text{Re}}^2},$$

in which

$$Q_1 = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} = \frac{\omega L_{s1\text{-eff}}}{R_{s1\text{-eff}}}, Q_2 = \frac{\text{Im}(Z_{22})}{\text{Re}(Z_{22})} = \frac{\omega L_{s2\text{-eff}}}{R_{s2\text{-eff}}}$$

$$k_{\text{Im}} = \frac{\text{Im}(Z_{12})}{\sqrt{\text{Im}(Z_{11})\text{Im}(Z_{22})}} \approx \frac{L_M - C_M R_M^2}{\sqrt{L_{s1\text{-eff}} L_{s2\text{-eff}}}} \approx \frac{L_M}{\sqrt{L_{s1\text{-eff}} L_{s2\text{-eff}}}}$$

$$k_{\text{Re}} = \frac{\text{Re}(Z_{12})}{\sqrt{\text{Re}(Z_{11})\text{Re}(Z_{22})}} \approx \frac{R_M}{\sqrt{R_{s1\text{-eff}} R_{s2\text{-eff}}}}$$

In contrast to a single-turn multilayer interlaced stacked (SMIS) transformer with similar range of operation frequencies [15], a bifilar transformer usually exhibits a smaller intrinsic coil-to-coil parasitic capacitance and a larger extrinsic coil-to-substrate parasitic capacitance. This means that the silicon-substrate effects on the performances of a bifilar transformer should be more prominent than that of an SMIS transformer. Therefore, in this letter, a test bifilar transformer has gone through the backside ICP etching to study its effects on the performances of bifilar transformers on silicon.

II. TRANSFORMER STRUCTURE AND DEEP-TRENCH TECHNOLOGY

Fig. 1(a) shows the top view die photo of a symmetrical bifilar transformer, which has a turn number of two, metal width

of 10 μm , coil spacing of 5 μm , inner dimension of $100 \times 130 \mu\text{m}^2$, and an overall dimension of $240 \times 240 \mu\text{m}^2$. Port-1 and Port-2 stand for the input port and the output port of the network analyzer, respectively. The transformer was fabricated with a 0.18- μm RF-CMOS technology on a p-type silicon substrate with a thickness of 300 μm and a resistivity of $10 \Omega \cdot \text{cm}$. The main features of the backend processes are as follows. There are six metal layers. We name the metal layers M1 to M6 from the bottom to the top. The thickness of M6 is 0.99 μm , and that of the others is 0.53 μm . The oxide thickness between M6 and M5, between other adjacent metal layers, and between M1 and the silicon substrate are 1, 0.85, and 1.1 μm , respectively.

The processing steps of our CMOS-compatible backside ICP deep-trench technology are shown in Fig. 1(b) and are described as follows. First, for the ease of chip handling, the front side of the die ($\sim 5 \times 5 \text{ mm}$) with transformers was stuck

to a glass substrate. Note that this process step can be omitted when applied in mass production because the wafer diameter is large. After standard photolithography processes on the backside of the die, the ICP etching (etching rate $\approx 2 \mu\text{m}/\text{min}$) was used to remove the silicon underneath the transformers. Specifically, the silicon below the rectangular area surrounded by the dashed line, as indicated in Fig. 1(a), was fully dry-etched away. The main gases used during the ICP etching process were alternate SF_6 (for etching) and C_4F_8 (for passivation) with a 17-s cycle. Finally, the adhesive and photoresist, which covered the frontside and backside of the die, respectively, were removed for test purposes.

III. MEASUREMENT RESULTS AND DISCUSSIONS

The S -parameter measurements were performed by an HP-8510C network analyzer. The expressions of the maximum available power gain (G_{Amax}), Q -factors (Q_1 and Q_2), magnetic-coupling factor (k_{Im}), and resistive coupling factor (k_{Re}) of a transformer in terms of its measured Z -parameters, which can be converted from the measured S -parameters, are listed in Table I [13]. Fig. 2(a) shows the measured Q_1 versus the frequency characteristics of the bifilar transformer. Increases of 62.4% (from 8.99 to 14.6) and 205.8% (from 8.6 to 26.3) in the Q -factor were achieved at 5.2 and 10 GHz, respectively, for the transformer after the ICP etching. The reason why the Q_1 of the ICP transformer at low frequencies has similar values as the Q_1 of the standard transformer is because the coupling between the two transformers and the silicon substrate is negligible at low frequencies [4]–[6]. In addition, the reason why the maximal Q (Q_{max}) and its corresponding frequency (f_{max}) increase after the ICP etching is because of the improvement of the substrate loss factor and the self-resonance factor due to the increase of the equivalent substrate impedance [12]. The increase of both f_{max} and Q_{max} means that the circuit designers can use the ICP transformers to design circuits with improved performance or to design higher frequency circuits. Fig. 2(a) also shows the measured k_{Im} and k_{Re} versus the frequency characteristics of the transformer. The extracted values of the mutual inductance L_M and coupling capacitance C_M in the equivalent circuit of Table I are 1.03 nH and 62.7 fF, respectively. In the frequency range of interest, the impedance of C_M is much higher than that of L_M . Therefore, to the first-order approximation, $k_{\text{Im}} \approx (L_M - C_M R_M^2) / \sqrt{L_{s1-\text{eff}} \cdot L_{s2-\text{eff}}}$ (see Table I). Clearly, an increase of C_M makes k_{Im} decrease, which in turn results in a larger x and thus a smaller G_{Amax} . At low frequencies, $R_M (\propto k_{\text{Re}})$ is close to zero, so the transformer is approximately pure inductive coupling. The decrease of k_{Im} with the increase of frequency can be regarded as an index of the degree of capacitive coupling. Apparently, the capacitive coupling of the transformer is very weak since C_M is small. The influence of the ICP etching on k_{Im} is very small because it mainly depends on the geometry of the coils. Very low k_{Re} smaller than 0.01 was achieved for frequencies up to 5.7 GHz for the transformer after the ICP etching. This is reasonable because the coupling between the coils should be predominately inductive if the silicon substrate under the transformer is etched away.

Fig. 2. Measured (a) Q -factor (Q_1), magnetic-coupling factor (k_{Im}), and resistive-coupling factor (k_{Re}) versus the frequency characteristics and (b) maximum available power gain (G_{Amax}) and minimum NF (NF_{min}) versus the frequency characteristics of the bifilar transformer before and after the backside ICP dry etching.

Fig. 2(b) shows the measured G_{Amax} versus the frequency characteristics of the bifilar transformer. Increases of 10.3% (from 0.697 to 0.769) and 30.2% (from 0.652 to 0.849) in G_{Amax} were achieved at 5.2 and 10 GHz, respectively, for the bifilar transformer after the backside ICP etching. Because the measured G_{Amax} of the ICP transformer is high enough (0.69–0.84) in the 3.1–10.6-GHz band, it is very suitable for 3.1–10.6 GHz UWB applications [16]. For passive devices, it is more suitable to report loss in decibels (i.e., minimum NF NF_{min} in Table I [17]) than gain in natural number. Therefore, the converted NF_{min} was also shown in Fig. 2(b) for comparison. A 0.43- (from 1.57 dB to 1.14 dB) and a 1.15-dB (from 1.86 dB to 0.71 dB) reductions in NF_{min} were achieved at 5.2 and 10 GHz, respectively, for the transformer after the ICP etching.

Table I shows a detailed comparison of the extracted parameters of the bifilar transformers in [10] and [13] and the bifilar transformer in this letter. As can be seen, the G_{Amax} values of 0.769 (5.2 GHz) and 0.849 (10 GHz) in this letter (top-metal thickness of $0.99 \mu\text{m}$) are better than those (0.764 and 0.687) of the bifilar transformer with a much thicker ($3.02 \mu\text{m}$) top metal (i.e., smaller metal loss per square) on a porous silicon substrate [10]. This is mainly attributed to the better

Q -factor performance of our transformer because its layout has been optimized [by “Momentum” of Agilent’s advanced design system (ADS)]. In addition, the G_{Amax} values in this letter (0.769 and 0.849) are also better than those (0.603 and 0.653) of the bifilar transformer with a top-metal thickness of $0.85\text{ }\mu\text{m}$ on a quartz substrate [13]. This is mainly attributed to the better Q -factor performance of our transformer because of its thicker top metal ($0.99\text{ }\mu\text{m}$) and its optimized layout. Moreover, the simulated results show that if the backside ICP etching in conjunction with a thick top metal of $3.02\text{ }\mu\text{m}$ (i.e., the top-metal thickness in [10]) is adopted, then very high Q -factors (Q_1 and Q_2) about 70 and G_{Amax} about 0.94 can be achieved (not shown here). This means that the most critical factors for achieving the state-of-the-art bifilar transformers are high-impedance substrate, layout optimization, and thick top metal.

IV. CONCLUSION

A CMOS-process compatible backside ICP deep-trench technology has been developed to enhance the performance of on-chip transformers. Significant improvements in both Q -factor and G_{Amax} were achieved for a test bifilar transformer after the backside ICP etching. Apparently, the proposed ICP technology is also capable of improving the isolation between the RF/analog and the digital circuits and thus paves a way for a system on a chip (SOC).

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