method. The reduction potential for biasing at the platinum-working electrode was set at -0.7V based on a voltammogram. As a result, the hydrogen ions in the enzyme-immobilised membrane were diminished due to the hydroxide ions generated by the reduction potential and the recovery time was reduced to less than 2min as compared to the 10–20min required using the conventional method.

It is anticipated that this reduced recovery time using an electrolysis method will advance the practical utilisation of ISFET glucose sensors.

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Keun-Yong Park, Minho Lee and Byung-Ki Sohn (School of Electronic and Electrical Engineering, Kyungpook National University, 1370 Sankyuk-dong, Puk-Gu, Taegu 702-701, Korea)

E-mail: mhlee@knu.ac.kr

References

- 1 VAN DER SCHOOT, B.H., and BERGVEL, P.: 'ISFET based enzyme sensors', *Biosensors*, 1988, 3, pp. 161–186
- 2 SOHN, B.K.: 'Some improvements in ISFET-based chemical sensors'. Proc. 8th Conf. Transducer'95, Eurosensor IX, 1995, pp. 890–893
- 3 KIM, C.S., SEO, H.I., LEE, C.H., and SOHN, B.K.: 'Miniaturized ISFET glucose sensor including a new structure actuation system'. Proc. Conf. Transducer'97, 1997, pp. 911–914
- 4 WESTROEK, P., TEMMERMAN, E., GOVAERT, F., KIEKENS, P., and STRYCKER, J.D.: 'Sensor system for simultaneous measurement of oxygen and hydrogen peroxide concentration during glucose oxidase activity', *Electroanalysis*, 1999, 7, pp. 517–519
- 5 SOHN, B.K., and KIM, C.S.: 'A new pH-ISFET based dissolved oxygen sensor by employing electrolysis of oxygen', *Sens. Actuators B*, 1996, 34, pp. 435–440

Low-voltage CMOS low-noise amplifier using planar-interleaved transformer

Chih-Chun Tang and Shen-Iuan Liu

A low-voltage CMOS low-noise amplifier (LNA) architecture is presented. A planar-interleaved transformer is used to couple the RF signal between cascode transistors in a conventional LNA topology. Based on the modified RF MOS model, a 5.2GHz CMOS LNA with fully on-chip input/output matching was designed to verify the low-voltage LNA architecture. The measurement results show that it can be operated with 1V supply voltage.

Introduction: With the growing popularity of wireless personal communication systems (PCNs), radio frequency (RF) ICs are in increasing great demand. The CMOS process is cheaper than the GaAs or BiCMOS process and can be integrated with base-band circuits. The characteristics of CMOS in the RF range [1] have thus been widely studied. To prolong the life of batteries in portable systems, low-voltage high-performance RF circuits are required. The design of such circuits is therefore a key issue.

The first proposed low-voltage CMOS LNA utilised a folded cascode amplifier topology [2]. There are two disadvantages of this topology. First, two LC tanks require a large die area. Secondly, the PMOS characteristics are usually poor in the RF range. An alternative low-voltage LNA topology is depicted in Fig. 1 [3]. The inductors in the LC tanks provide the DC bias current path, and the LC tanks resonate at the carrier frequency to provide large resistance. In addition to the two LC tanks, this topology requires another capacitor to bypass the RF signal from M1 to M2. The small bypass capacitor increases the noise figure (NF) rapidly because it contributes significant resistance in the RF range. To reduce the noise contribution of the bypass capacitor, one approach is to use an MIM capacitor to realise a large bypass capacitor. Unfortunately, this process requires additional masks to fabricate the MIM capacitor.

Fig. 1 Simplified schematic diagram of low-voltage CMOS LNA topology utilising LC tanks and bypass capacitor

Fig. 2 Proposed topology of low-voltage CMOS LNA utilising planar-interleaved transformer

T1 is planar-interleaved transformer

Fig. 3 Die photograph of proposed CMOS LNA

Proposed low-voltage CMOS LNA: Our proposed low voltage CMOS LNA topology is shown in Fig. 2. The input matching is achieved by designing L_g , L_s and the gate-to-source capacitance (C_{gs1}) of M1 to fulfill the following equations [4]:

$$\omega_{RF} = \frac{1}{\sqrt{(L_g + L_s)C_{gs1}}} \quad (1)$$

$$R_{source} = \frac{g_{m1}}{C_{gs1}} L_s \quad (2)$$

where ω_{RF} is the carrier frequency and R_{source} is the impedance of the signal source. The planar-interleaved transformer, T1, is used to couple the RF signal from M1 to M2. Transistor M3 is configured as an output driver stage to drive the 50Ω load. Since the planar-interleaved transformer has a higher self-resonant frequency (f_{SR}) than the stacked transformer, this topology can operate properly at the higher frequency. Owing to the fact that the planar-interleaved transformer replaces the two LC tanks and one bypass capacitor in Fig. 1, the proposed topology can operate under a low supply voltage with less die area.

RF models: The modified MOSFET model for simulation is based on the BSIM3v3 SPICE model, with some passive components added to combat the parasitic effects in the RF range [5]. The inductors and the planar-interleaved transformer were all designed and modelled by ASITIC [6]. For accuracy, each interconnection was modelled as the transmission line.

Fig. 4 Measurement results of proposed CMOS LNA with 1V supply voltage

× S11 ($S_{11} = -16.1\text{dB}$ at 5.2GHz)
 ◇ S12 ($S_{12} = -34.5\text{dB}$ at 5.2GHz)
 ○ S21 ($S_{21} = 7.87\text{dB}$ at 5.2GHz)
 + S22 ($S_{22} = -18.7\text{dB}$ at 5.2GHz)

Measurement results: The proposed low voltage CMOS LNA was fabricated using a 0.35 μm 1P4M standard digital CMOS process. Its die photograph is shown in Fig. 3. The aspect ratio of all the transistors was (100/0.35) μm . All the inductors were circular to obtain higher quality factors, and the MOS gate fingers were double-ended to reduce the noise [4]. The measured values were as follows: S11 was -16.1dB , S22 was -18.7dB , S21 was 7.87dB , S12 was -34.5dB and NF was 5.6dB at 5.2GHz, with 12.4mA being drawn from the 1V supply voltage without any off-chip tuning. Fig. 4 shows the measured S-parameters. The measured $P_{-1\text{dB}}$ is -6.2dBm and IIP_3 is $+2.8\text{dBm}$.

Conclusions: A low-voltage CMOS low-noise amplifier topology has been demonstrated and a 1V, 5.2GHz CMOS LNA has been fabricated and measured to verify this topology. The measurement results prove that the proposed CMOS LNA topology can operate properly at a high frequency with a low supply voltage. Since this LNA has been fabricated using standard CMOS technology, it can be easily integrated with other front-end circuits to build CMOS transceivers without requiring any additional mask or post-processing steps.

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Chih-Chun Tang and Shen-Iuan Liu (Lab. 328, Department of Electrical Engineering and Graduate Institute of Electronic Engineering, National Taiwan University, Taipei, Taiwan 10617, Republic of China)

References

- 1 MANKU, T.: 'Microwave CMOS — device physics and design', *IEEE J. Solid-State Circuits*, 1999, **34**, (3), pp. 277–285
- 2 ABOU-ALLAM, E., and MANKU, T.: 'A low voltage design technique for low noise RF integrated circuits', *IEEE ISCAS98*, 1998, Vol. 4, pp. 373–377
- 3 MANKU, T., BECK, G., and SHIN, E.J.: 'A low-voltage design technique for RF integrated circuits', *IEEE Trans. Circuits Syst., Part II*, 1998, **45**, (10), pp. 1408–1413
- 4 SHAFFER, D.K., and LEE, T.H.: 'A 1.5-V, 1.5-GHz CMOS low noise amplifier', *IEEE J. Solid-State Circuits*, 1997, **32**, (5), pp. 745–759

- 5 HSIAO, C.C., KUO, C.W., and CHEN, Y.J.: '6.8GHz monolithic oscillator fabricated by 0.35 μm CMOS technologies', *Electron. Lett.*, 2000, **36**, (23), pp. 1927–1928
- 6 NIKNEJAD, A.M., and MEYER, R.G.: 'Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's', *IEEE J. Solid-State Circuits*, 1998, **33**, (10), pp. 1470–1481

Deep-ridge distributed feedback waveguide for polarisation independent all-optical switching

S.-H. Jeong, T. Mizumoto, K. Nakatsuhara, M. Takenaka and Y. Nakano

Structural birefringence in a deep-ridge distributed feedback (DFB) waveguide for polarisation independent all-optical switching is investigated. The coupling coefficient of the DFB structure is also polarisation independent between the TE and TM modes.

Introduction: All-optical switches, which do not need OE/EO conversion, are indispensable components for implementation of ultrafast optical signal processing [1]. The combination of the optical Kerr effect and the distributed feedback (DFB) mechanism in nonlinear media enables all-optical bistable, thresholding and Boolean logic functions to be realised. Nonlinear waveguide devices loaded with corrugated grating can be monolithically integrated with other photonic devices, since they do not require any cleaved facets. The all-optical bistable [2], thresholding [3] and AND-logic operation [4] were reported in nonlinear distributed feedback waveguides, and all-optical bistable switching was reported in a nonlinear directional coupler loaded with Bragg reflector [5]. All of these results were achieved by launching TE-polarised lightwave into an input port of the device, since these devices intrinsically have strong structural birefringence. In the nodes of a photonic network, however, the input light is unpolarised. Hence, optical switching operations are strongly required to be insensitive to the state of polarisation of the input light. A large number of waveguide schemes such as buried structure [6] and deep-ridge structure [7] have been intensively investigated to minimise structural birefringence. The deep-ridge waveguide structure is a most promising candidate from the viewpoint of compactness, simplicity of fabrication process and integration with other photonic devices such as a wavelength converter or a semiconductor optical amplifier.

Fig. 1 Schematic diagram of deep-ridge distributed feedback waveguide

Configuration of device: Fig. 1 shows a schematic diagram of the deep-ridge distributed feedback waveguide. In the deep-ridge waveguide, structural birefringence can be eliminated by adjusting the waveguide width (W). In addition, the variation of the birefringence is strongly influenced by the waveguide parameters, such as the composition of the core (N_{co})/cladding (N_{cl}) and the thickness of the upper cladding (T_{uc})/core (T_{co}) [8]. As a preliminary experiment, the device was fabricated using a GaInAsP/InP wafer in which a 300nm-thick InP upper cladding layer and a 450nm-thick GaInAsP ($\lambda_g = 1430\text{nm}$) guiding layer were grown on an (100) InP substrate. The deep-ridge was formed by reactive ion etching using a $\text{CH}_4/\text{H}_2\text{O}/\text{O}_2$ mixture. To operate at the 1.55 μm -