Brief Papers

An 8-bit 10 MS/s Folding and Interpolating ADC Using the Continuous-Time Auto-Zero Technique

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Abstract—An 8-bit 10-MS/s folding and interpolating analog-to-digital converter (ADC) using the continuous-time auto-zero technique is presented. Compared with the conventional architecture, it can improve the nonlinear errors and enhance the signal-to-noise-and-distortion ratio (SNDR). Both architectures have been fabricated on the same die of a 0.35- μm DPDM CMOS process and measured under the same conditions with a 2.7-V supply voltage and 10-MHz sampling rate. The continuous-time auto-zero architecture shows an ENOB of 7.7 bits while the conventional one shows 5.8 bits.

Index Terms—Analog-to-digital converter, auto-zero technique, folding and interpolating.

I. INTRODUCTION

THE FOLDING and interpolating analog-to-digital converters (FIADCs) have been applied in moderate to high-resolution and high-speed applications such as hard disk channel drives [1] or communication systems [2]. The folding ADC has the advantages of high speed and reduced number of comparators compared to a flash ADC. The interpolating ADC can reduce the number of the input amplifiers and lower the input capacitance. Normally, both of the above techniques are combined to realize a so-called FIADC [1]–[5].

Theoretically, a folding circuit will preprocess the input signal and overcome the offset of the comparators. However, the mismatch in the input differential amplifier will induce a large offset, which will destroy the linearity of the ADC. For a digital CMOS technology, the offset will limit the resolution unless transistors of large area and large bias currents are used.

For the sake of this consideration, two 8-bit FIADCs with and without the continuous-time auto-zero technique have been investigated. Finally, experimental results are compared to each other, and a conclusion is given in Section V.

II. CONVENTIONAL FOLDING AND INTERPOLATING ADC

A. The 8-Bit Conventional FIADC

The conventional FIADC is shown in Fig. 1. If the 8-bit ADC is divided into a 3-bit coarse ADC and a 5-bit fine ADC, the folding circuits should make the signals nine-folded. There are 36 distributed track and hold amplifiers [6], as shown in Fig. 2, in front of the two folding stages. Thirty-six differential

output signals of these amplifiers have zero-crossing points corresponding to the reference voltages, $\text{ref1} \sim \text{ref36}$, generated by 36 equal resistors. A folding circuit is composed of two-stage folding triplets [7], as shown in Fig. 3, which are realized by the self-biased amplifiers with symmetric loads [8] in Fig. 4. Each folding amplifier of the first stage will generate three zero crossings, and that of the second stage will generate nine by combining three of the first-stage folding signals. The advantage of the two-stage folding scheme is that a larger output swing and gain can be achieved [7]. Originally, the total nine-folded signals are four. Since the active interpolating [6] technique can reduce interpolating errors, 32 nine-folded signals in front of the comparators are available by using this technique in each stage. A symmetric load is used here instead of a passive load because the passive load will occupy large area and its absolute accuracy will have effects on the common-mode voltage. Moreover, the self-biased amplifier with symmetric loads can provide a symmetric swing and a stable common-mode voltage to have good power-supply rejection capability [8]. Because the symmetric load is composed of transistors, the area and parasitic effect will be also reduced.

The active interpolating [6] circuit is shown in Fig. 5. Theoretically, if the offset voltages of the two adjacent distributed amplifiers are $v_{\text{off}1}$ and $v_{\text{off}2}$, respectively, the offset voltage of the $2\times$ interpolating output will be $v_{\text{off}} = (v_{\text{off}1} + v_{\text{off}2})/2$. Thus, the differential nonlinearity (DNL) will be lowered by a factor of two after interpolating, but the integral nonlinearity (INL) is still large. In back of the active interpolation, 32 comparators detect the zero crossings of the folding signals to carry out fine 5 LSBs. The comparator is not critical because the signal has been amplified in the previous stages. Normally, the static and dynamic offset about 40 or 50 mV of the comparator can be overcome. The circular code from the output of comparators will be fed into an encoder with three-input NAND gates to remove the bubble error [9].

Because the coarse and fine comparisons are dealt with separately, there are three misalignment regions of the coarse and fine ADC. In order to resolve this problem, six comparators and a bit synchronization [4] are used to define these regions and align the coarse and fine ADC.

B. Intrinsic Problems in the Conventional Circuit

In this architecture, there are two error sources resulting in poor performance. One is the interpolating error due to small overlapped linear regions of the folding signals, and the other is

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Fig. 1. Conventional architecture.

Fig. 2. Distributed track and hold amplifiers.

Fig. 3. Two-stage folding scheme is used for the nine-folded signals.

the random offset due to mismatch. The former can be improved by choosing enough reference folding signals or using active interpolating technique. But the latter is an intrinsic problem in

the conventional CMOS folding circuits. Although the law of $1/\sqrt{WL}$ can predict the offset voltage for the differential pairs, we do not have the exact parameters in our process. If a 10-mV

Fig. 4. Folding triplet and self-biased circuit.

Fig. 5. Active interpolating scheme.

offset voltage exists and the conversion range is 1 V, the final resolution will be about 6 bits and thus the integral or differential nonlinear errors will be worse.

III. IMPROVEMENT ON THE NONLINEAR ERRORS

The resistive averaging methods had been reported in [1], [3]. Its basic idea is described as follows. Assume that the input offset variances of the two adjacent distributed amplifiers are σ_1 and σ_2 , respectively. After averaging, the output signal will have a variance of $\sqrt{(\sigma_1)^2 + (\sigma_2)^2}/2$. If σ_1 and σ_2 are equal and not correlated, the variance will be reduced by a factor of $\sqrt{2}$, and so will the INL. The more averaging number is used, the more linearity can be achieved. Although there are a lot of advantages in this method, two problems exist. First, the gain of the amplifiers will degenerate due to the loading effect such that the offset voltage of the next stage is not easy to overcome. Second, if one would like to lower the INL by N times, N^2 distributed amplifiers are required in their linear ranges. It is not efficient when N is larger than four. In order to minimize the offset voltage of the folding amplifiers, the auto-zero technique is applied.

A. The Basic Principle of the Auto-Zero Technique

It is shown in Fig. 6 that the new folding path with an auxiliary differential pair is added to reduce the offset voltage [10]. When it is in the auto-zero mode, the input is connected to the reference and the switches of the auto-zero (AZ) signal will be on. Assume that the offset voltage of the differential pair ($m1, m2$) with transconductance Gm_1 is v_{off1} ; that of the differential pair ($m3, m4$) with transconductance Gm_2 is v_{off2} ; those of the

first and second folding stages are v_{off3} and v_{off4} , respectively. Thus, v_1 , v_2 and v_{out} can be expressed as

$$v_1 = [Gm_1 v_{off1} - Gm_2 (v_{out} + v_{off2})]R \quad (1)$$

where the load of the distributed amplifier is assumed to be R .

$$v_2 = A(v_1 + v_{off3}) \quad (2)$$

$$v_{out} = A(v_2 + v_{off4}) \quad (3)$$

By combining the above equations, v_{out} can be expressed as

$$v_{out} = \frac{A^2 Gm_1 R v_{off1} - A^2 Gm_2 R v_{off2} + A^2 v_{off3} + A v_{off4}}{1 + A^2 Gm_2 R} \quad (4)$$

When the AZ signal is off, this value will be stored in the capacitors C1 and C2. And when the input signal comes in, the equivalent offset voltage v_{off} can be expressed as

$$v_{off} = \frac{v_{off1} - \left(\frac{Gm_2}{Gm_1}\right) v_{off2} - \frac{v_{off3}}{Gm_1 R} - \frac{v_{off4}}{A Gm_1 R}}{1 + A^2 Gm_2 R} \quad (5)$$

From (5), the offset voltages have been divided by the loop gain. The gain of the two-stage folding amplifiers is $A = \sqrt{10}$; the feedback $Gm_2 R$ is 0.7; the gain of the distributed amplifier $Gm_1 R$ is 2. Because the folding circuits do not have any frequency compensation mechanism, the gain and poles should be decided carefully. The output resistance of the second folding-stage amplifier and the offset voltage storage capacitors determines the dominant pole. The first folding stage and the distributed amplifier determine the other high-order poles. These high-order poles are not far away from the unity gain frequency, and they will result in small phase margin. Thus, $[Gm_2/Gm_1]$ can be chosen as 0.35 to make the loop stable. Substituting the above data into (5), the following equation can be obtained:

$$v_{off_{comp}} = 0.125 v_{off1} - 0.043 v_{off2} - 0.0625 v_{off3} - 0.02 v_{off4} \quad (6)$$

and the original offset voltage without compensation can be expressed as

$$v_{off_{uncomp}} = v_{off1} + 0.5 v_{off3} + 0.16 v_{off4} \quad (7)$$

Fig. 6. A new folding block with offset compensation.

Fig. 7. New auto-zero folding and interpolating ADC.

The compensated input offset voltage is at least eight times lower than the uncompensated one. Because the offset storage capacitors will have a current leakage path through the switches, the offset cancellation should be continued after a period of time. Thus, a continuous-time architecture has been developed.

B. The 8-Bit FIADC with Continuous-Time Auto-Zero Technique

Because of the auto-zero structure, the active interpolating can not be applied stage by stage. The proposed architecture is presented in Fig. 7. Basically, eight folding circuits for eight nine-folded signals are required, but there is an extra one in the auto-zero mode [9], [11]. Nine folding circuits including the auto-zero technique [10] are added in the folding process. The folding amplifiers [7], [8] are still two stages. Then, $4\times$ active interpolating [6] are used in back of the folding blocks (FBs) for 32 folding signals. In Fig. 8, a single folding block and its timing diagrams are given to generate the folding signal. There are nine paths that we have to keep the offset voltages in the storage capacitors. So, clocks AZ1–AZ9 are generated for this

purpose. For each path, the auto-zero function has been done with the correspondent reference voltage R_i ($i = 1 - 9$). And, clocks AZ1–AZ9 occupy a period of the sampling clock to finish this work.

The operation of nine folding circuits are described as follows [9], [11]: In Fig. 9, the clock F_n ($n = 1-9$) controls the input switches and which folding block is auto-zeroed, and the clock U_n ($n = 1-9$) decides the down or up references. Both the clocks F_n and U_n control the outputs of the folding blocks. Initially, the first folding block (FB1) is auto-zeroed with the first reference REF1, and FB2–FB9 operate normally. When FB2 is auto-zeroed with REF2, FB1 and FB3–FB9 operate normally. The process proceeds until FB8 is auto-zeroed with REF8, FB1–FB7 and FB9 operate normally. After FB1–FB8 being auto-zeroed, FB9 is auto-zeroed with REF8 and FB1–FB8 operate normally. Then, FB8 is auto-zeroed with REF7, FB1–FB7 and FB9 operate normally. The process proceeds until FB1 is auto-zeroed with REF1 and FB2–FB9 operate normally. Thus, the auto-zero process can be done continuously. Each reference REF_i ($i = 1-8$) consists of nine reference voltages from 72 resistors.

Fig. 8. Single folding block and its timing diagrams.

TABLE I
DATA COMPARISON

	Conventional	Auto-zero
Technology	Sharp 0.35μm DPDM CMOS	
Resolution	8-bit	
Conversion rate	10MS/s	
SNDR @ 80kHz	37dB	48dB
INL	-1.56lsb ~ +0.83lsb	-0.17lsb ~ +0.29lsb
DNL	-0.30lsb ~ +0.37lsb	-0.16lsb ~ +0.19lsb
Analog input range	1V-2V	
Supply voltage	2.7V to 3.3V	
Power	85mW @ 2.7V	76mW @ 2.7V
	115mW @ 3.3V	105mW @ 3.3V
Area	2.65mm×1.61mm	2.93mm×1.71mm

IV. EXPERIMENTAL RESULTS

The two FIADCs are measured under 10 MS/s and 2.7–3.3-V supply voltages. The input range is from 1 to 2 V. Fig. 10(a) shows the output spectrum of the conventional FIADC, which has many large harmonics due to offset. The SNDR is 37 dB, and the ENOB is 5.8 bit. Fig. 10(b) shows the output spectrum of the FIADC with auto-zero technique. The SNDR is 48 dB, and the ENOB is 7.7 bit. Fig. 11(a) shows the nonlinearity of the conventional FIADC. The INL is from -1.56 LSB to $+0.83$ LSB. The results of the auto-zeroed FIADC are shown in Fig. 9. The

Fig. 9. Nine folding blocks and their timing diagrams.

INL is much smaller than previous one, which is from -0.17 LSB to $+0.29$ LSB. Both of these data are measured at 80-kHz input signal. The SNDR versus input frequency is shown in Fig. 12. The auto-zeroed FIADC has 10-dB improvement and more bandwidth than the conventional one. In order to have a higher conversion rate, the auto-zero time period has been designed with three modes: one clock, two clocks, and four clocks. But, because of the switching noise from the comparators, the ENOB is 7 bit as the clock rate higher than 20 MHz is applied. Thus, only the data measured under 10 MS/s and 2.7–3.3 V are listed and compared with each other in Table I. The die photo of these converters is shown in Fig. 13.

V. CONCLUSION

The new continuous-time auto-zeroed folding and interpolating architecture has been developed to improve INL and DNL. The maximum sampling rate is 10 MS/s, which is much lower than the previous FIADCs because the auto-zero process takes a lot of time to settle. However, we would like to demonstrate the feasibility of the proposed architecture.

Fig. 10. (a) Measured 80 kHz at 10 MS/s of the conventional ADC. (b) Measured 80 kHz at 10 MS/s of the anti-zero ADC.

Fig. 11. (a) Measured INL and DNL results of the conventional ADC. (b) Measured INL and DNL results of the auto-zero ADC.

Fig. 12. SNDR results of these two FIADCs.

Fig. 13. Die photo of the converters.

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