Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As/GaAs lattice-matched and strained doped-channel field-effect transistors grown by gas source molecular beam epitaxy

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(Received 17 August 1998; accepted for publication 3 November 1998)

Recently, it was demonstrated that doped-channel field-effect-transistor (DCFET) structure has the advantages of high breakdown voltage, high current drivability, and high turn on voltage. Therefore, a series of lattice-matched and strained Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As/GaAs ($0 \leq x \leq 0.22$) DCFETs were studied in order to find the optimized structure. Through dc and microwave measurements, we observed that the introduction of a 150-Å-thick strained In_xGa_{1-x}As ($0.15 \leq x \leq 0.22$) channel can enhance device performance, compared to the lattice-matched one ($x=0$). The optimized performance of transconductance (g_m), current-gain cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) all occurred when indium content x was between 0.15 and 0.20 for devices with 1-μm-long gate and these optimized results are comparable to those state-of-the-art results of pseudomorphic high electron mobility transistors. We also found that DCFETs are very ideal for single-voltage-supply operation. Degradation of device performance was observed for larger indium content ($x=0.22$), which is associated with strain relaxation in this highly strained channel. Experimental results showed that Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As/GaAs DCFETs with indium content x between 0.15 and 0.20 were very suitable for microwave high power device applications. © 1999 American Institute of Physics. [S0021-8979(99)00604-0]

I. INTRODUCTION

The heterostructure field-effect transistors (HFETs) based on an InGaAs pseudomorphic channel have shown excellent performance at millimeterwave frequencies¹⁻⁶ due to the good electron confinement by the potential well, high current drivability, and high transconductance. Namely, device performance is enhanced substantially by increasing the indium content in the InGaAs channel.

Recently, there is increasing interest in Ga_{0.51}In_{0.49}P/InGaAs/GaAs pseudomorphic structure because Ga_{0.51}In_{0.49}P/InGaAs/GaAs material system has some advantages compared with the AlGaAs/InGaAs/GaAs system:⁷⁻¹² (1) because no Al is involved in this system, the problem associated with Al oxidation can therefore be avoided; (2) the etching selectivity between Ga_{0.51}In_{0.49}P and GaAs is very high,⁸ which means high process uniformity and yield;^{9,10} (3) the $1/f$ noise of Ga_{0.51}In_{0.49}P is lower due to smaller surface recombination.^{11,12} Moreover, monolithic-microwave integrated circuits (MMICs) using Ga_{0.51}In_{0.49}P/InGaAs/GaAs pseudomorphic high electron mobility transistors (PHEMTs) as active devices have shown state-of-the-art 60 GHz MMIC image-rejection downconverter and direct-couple-FET-logic (DCFL) circuits.^{13,14}

Although there were a lot of reports on the performance of Ga_{0.51}In_{0.49}P/InGaAs/GaAs PHEMTs,^{9,11,13-16} there are only few but no systematic reports on the performance of Ga_{0.51}In_{0.49}P/InGaAs/GaAs doped-channel field-effect transistors (DCFETs).^{10,17} As a matter of fact, it is known that

DCFET structure has the advantages of high breakdown voltage, high current drivability, and high turn on voltage. Therefore, in this article, we would like to systematically study the lattice-matched and strained Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As/GaAs ($0 \leq x \leq 0.22$) DCFETs in order to investigate the influence of the indium content in the channel on device properties and find the optimized Ga_{0.51}In_{0.49}P/InGaAs/GaAs DCFET structure. Experimental results showed that the performance of Ga_{0.51}In_{0.49}P/In_xP/In_xAs/GaAs DCFETs with indium content x between 0.15 and 0.20 were very excellent and comparable to those state-of-the-art results of PHEMTs reported by Yamaguchi *et al.*¹⁸

II. CRYSTAL GROWTH AND DEVICE TECHNOLOGY

Lattice-matched and strained Ga_{0.51}In_{0.49}P/In_xGa_{1-x}As/GaAs ($0 \leq x \leq 0.22$) doped-channel structures with different indium contents shown in Fig. 1 were grown by gas source molecular beam epitaxy (GSMBE) as follows. First, a 5000 Å undoped GaAs buffer layer was grown on a semi-insulating (100) GaAs substrate, followed by a 150 Å In_xGa_{1-x}As n -channel layer (normally, $4 \times 10^{18} \text{ cm}^{-3}$, Si doped). Then a 200 Å undoped Ga_{0.51}In_{0.49}P insulating layer was grown on top of the active channel. Finally, a 400 Å n^+ -GaAs cap layer ($2 \times 10^{18} \text{ cm}^{-3}$, Si doped) was grown to facilitate the formation of good ohmic contacts. The growth temperature was 580 °C for GaAs and 500 °C for In_xGa_{1-x}As and Ga_{0.51}In_{0.49}P. The V/III ratio was about 2:1 with group V being hydride gases and group III being solid (metal) sources. The In_xGa_{1-x}As/Ga_{0.51}In_{0.49}P interface was grown by having the PH₃ source on the In_xGa_{1-x}As surface for 15 s before starting the Ga_{0.51}In_{0.49}P growth. That is, after growing the In_xGa_{1-x}As, we closed In and Ga shutter and

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FIG. 1. Device cross section of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) doped-channel FETs.

turned off the AsH_3 . Then we turned on the PH_3 gas and 15 s later opened the Ga and In shutters to start growing the $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ layer.

The indium content of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel layer varies from $x=0, 0.15, 0.20$ to 0.22 in order to examine how the strained channel affects the material characteristics as well as the devices performance. Because metal gate is sitting directly on the undoped high-band-gap $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ insulating layer (1.92 eV) and conduction band discontinuity at the $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}$ ($0 \leq x \leq 0.22$) heterojunction is also large (0.22–0.38 eV),^{5,11,19} higher breakdown voltage and current drivability, as compared to metal-semiconductor field-effect transistors (MESFETs) and HEMTs, can therefore be expected.^{20,21} In addition, because metal- $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ Schottky barrier is reasonably high (0.86 eV),^{19,22} and because DCFETs has no parallel conduction effect, these DCFETs have higher gate turn on voltage than MESFETs and HEMTs. In DCFETs the metal gate is on top of the insulating layer, the Schottky barrier height of the chosen insulating layer is higher than that of conducting channel layer. Because of this, the electrons in the channel layer of DCFETs “see” a higher potential barrier than the electrons in the channel layer of MESFETs when $V_{\text{GS}}=0$ V. Therefore, it takes more voltage for DCFETs to forward bias the gate-to-source diode than MESFETs do, if we define the gate turn on voltage as the voltage to reach the current level of 1 mA/mm. In the case of PHEMTs, the electrons will gradually accumulate in the electron supplying layer (e.g., doped $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ layer in PHEMTs) when V_{GS} is increasing from 0 (so-called parallel conduction phenomena in HEMT or PHEMT). The accumulated electrons in the supplying layer will see a smaller barrier and thermionically emit over it or see a thinner barrier and tunnel through it. Therefore, again, DCFETs have higher gate turn on voltage than HEMTs. In fact, the measured gate turn on voltages were all around 1.1 eV for devices with indium contents $x=0, 0.15, 0.2$, and 0.22 . These values were comparable to that (1.0 eV) of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ DCFETs and better than that (0.65) of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ HEMTs.²¹

TABLE I. Hall mobilities and sheet charge densities of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) doped-channel structures at 300 and 77 K, respectively.

	Mobility ($\text{cm}^2/\text{V s}$)		Sheet charge density (10^{12} cm^{-2})	
	300 K	77 K	300 K	77 K
$x=0.0$	1866	2277	2.99	2.47
$x=0.15$	2930	3458	4.90	4.45
$x=0.20$	3170	3804	5.66	5.11
$x=0.22$	2817	3328	5.20	4.64

After the removal of the n^+ GaAs cap layer of the heterostructures to prevent shunt conduction, Hall measurements were conducted at 300 and 77 K. These results were summarized in Table I. The Hall mobilities at 300 K increased systematically with the indium content, from 1866 $\text{cm}^2/\text{V s}$, for $x=0$, 2930 $\text{cm}^2/\text{V s}$ for $x=0.15$ to 3170 $\text{cm}^2/\text{V s}$ for $x=0.20$. The associated sheet charge densities (n_s) were 2.99×10^{12} , 4.90×10^{12} , and $5.66 \times 10^{12} \text{ cm}^{-2}$, respectively. For the $x=0.22$ layer, these values dropped to 2817 $\text{cm}^2/\text{V s}$ and $5.20 \times 10^{12} \text{ cm}^{-2}$, respectively. Mobilities were slightly higher at 77 K. Lower mobilities and higher sheet charge densities, compared with the HEMTs, is typical of the DCFETs scheme. Note that the mobility and carrier sheet charge were enhanced systematically with increasing indium content in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ channels until $x=0.20$. Hall mobility and sheet charge density drop were found in the case where $x=0.22$. The reason for this phenomenon can be explained as follows. It is known that $\text{In}_x\text{Ga}_{1-x}\text{As}$ has different lattice constant with GaAs or $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$. When $\text{In}_x\text{Ga}_{1-x}\text{As}$ is grown on top of GaAs, it will be strained if it is not “too thick.” The maximum thickness that $\text{In}_x\text{Ga}_{1-x}\text{As}$ can still remain strained and not relaxed to cause interface defects or dislocations is called critical thickness. According to Matthews and Blakeslee’s,²³ these thicknesses can be calculated to be 212, 148, and 131 Å for $x=0.15, 0.2$, and 0.22 , respectively. In the case of $x=0.22$, since the channel thickness is far beyond the critical thickness, lots of defects have been created. Some electrons are trapped in the defects and therefore sheet carrier density decreases instead of increasing. Also, because of the existence of defects, electrons encountered more scattering and hence the mobility degrades. Although our discussion is mainly based on defects, other problems, such as “In segregation,” “As/P intermixing,” and “interface roughness” resulting by changing from AsH_3 to PH_3 gas during the GSMBE growth of $\text{Ga}_{0.49}\text{In}_{0.51}\text{P}$ on top of $\text{In}_x\text{Ga}_{1-x}\text{As}$ (Ref. 19) may also contribute to the reduction of mobility.

Conventional optical lithography and mesa type wet etching technique were used to fabricate the $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) DCFETs. First, the mesa isolation was done. Then Ni/GeAu/Ni/Au (50/1200/50/1000 Å) ohmic contacts were thermally evaporated, patterned by liftoff and rapid thermal annealed (RTA) at 410 °C for 30 s. After the GaAs cap layer was selectively wet etched, 1-μm-long, 100-μm-wide Ti/Au gates were evaporated and defined by a lift-off process. The spacing between gate drain and gate source were 2 and 1 μm long, respectively, as shown in Fig. 1.

FIG. 2. (a) Typical I_{ds} - V_{ds} characteristics of the $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_{0.15}\text{Ga}_{0.85}\text{As}/\text{GaAs}$ doped-channel FETs with $1.0\text{-}\mu\text{m}$ -long gate and (b) the corresponding I_{ds} and $g_{m,\text{ext}}$ vs V_{gs} characteristics.

III. DC CHARACTERISTICS

Drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) characteristics of both lattice-matched and strained $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) DCFETs were measured by an HP4156 precise parameter analyzer. Typical I_{ds} - V_{ds} characteristics of a $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_{0.15}\text{Ga}_{0.85}\text{As}/\text{GaAs}$ pseudomorphic DCFET with $1\text{-}\mu\text{m}$ -long gate were shown in Fig. 2(a). One salient feature of the I - V characteristics is that positive gate voltage swing can be as large as 1 V, compared to traditional HEMTs (PHEMTs) and MES-FETs. As can be seen in this figure, drain current is almost symmetrical about the current level with $V_{GS} = 0$ V. The significance of this fact is that positive gate bias of this FET for class A operation in power application is possible, which means that single power supply biasing scheme for FET power amplifier is achievable. Figure 2(b) was the characteristics of I_{ds} and extrinsic transconductance ($g_{m,\text{ext}}$) versus

FIG. 3. Typical $g_{m,\text{ext}}$ vs I_{ds} characteristics of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) doped-channel FETs with $1.0\text{-}\mu\text{m}$ -long gate.

gate-source voltage (V_{gs}). A peak $g_{m,\text{ext}}$ of 350 mS/mm was obtained. The output conductance (g_{ds}) at $V_{gs} = 0$ V was 2.2 mS/mm and therefore a high dc gain ratio ($g_{m,\text{ext}}/g_{ds}$) of 159 was obtained. Moreover, the gate-drain breakdown voltage (BV_{gd}), defined as the voltage at which the gate current reaches 1 mA/mm, was 31 V. This is attributed to the high-quality undoped high-band-gap $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ insulator layer, which could sustain a very high breakdown field at the gate edge nearest to the drain.

Figure 3 shows the dependence of $g_{m,\text{ext}}$ on I_{ds} for DCFETs with different indium contents at $V_{ds} = 4$ V. A distinct feature of strained devices ($x > 0$), compared to GaAs channel devices ($x = 0$), was the significant increase of $g_{m,\text{ext}}$ and maximum channel current ($I_{ds,\text{max}}$). The characteristic curves of $g_{m,\text{ext}}$ vs I_{ds} for strained devices ($x > 0$) extended not only to higher I_{ds} values but also exhibited flatter $g_{m,\text{ext}}$ characteristics with wider drain bias current conditions, namely, 370 mA/mm for $x = 0.15$, 365 mA/mm for $x = 0.20$ and 340 mA/mm for $x = 0.22$ in contrast with 185 mA/mm for $x = 0$. The “width” of flat region was defined as the difference of two current densities corresponding to 10% drop from the maximum $g_{m,\text{ext}}$. That is, better current drivability and linearity of strained devices were achieved due to higher carrier density/mobility and better carrier confinement. Threshold voltages of the devices with different indium content x are listed in Table II. Samples with higher carrier density ($x = 0.20$ and 0.22) usually presented a more negative V_{th} . As a matter of fact, by extending the theory of two-dimensional electron gas FETs proposed by Delagebeaudeuf and Linh,²⁴ we can drive the threshold voltage as follows:

$$V_{th} = \phi_b - \Delta E_C - \frac{qN_{\text{eff}}td}{\epsilon_2} - \frac{qN_{\text{eff}}t^2}{2\epsilon_1}, \quad (1)$$

where ϵ_1 is the dielectric constant of $\text{In}_x\text{Ga}_{1-x}\text{As}$, ϵ_2 is the dielectric constant of $\text{Ga}_{0.5}\text{In}_{0.49}\text{P}$, t is the thickness of $\text{In}_x\text{Ga}_{1-x}\text{As}$, q is the electron charge, ϕ_b is the Schottky

TABLE II. Summary of dc characteristics of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) doped-channel FETs with 1.0- μm -long gate.

In content	$x=0$	$x=0.15$	$x=0.20$	$x=0.22$
$g_{m,\text{ext}}$ (mS/mm)	241 ± 3	350 ± 5	306 ± 5	275 ± 4
$I_{\text{ds,max}}$ (mS/mm)	360 ± 5	575 ± 8	630 ± 10	585 ± 10
V_{th} (V)	-0.71 ± 0.02	-1.18 ± 0.025	-1.62 ± 0.04	-1.71 ± 0.05
$I_{\text{ds,gmax}}$ (mA/mm)	190 ± 3	300 ± 4	340 ± 5	335 ± 4

barrier between metal and $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$, ΔE_c is the discontinuity in the conduction band between $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ and $\text{In}_x\text{Ga}_{1-x}\text{As}$, and N_{eff} is the effective doping density in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel. From the experimental results of V_{th} , we found that the differences in the threshold voltages of the devices with different indium content are larger than those estimated from the difference in ΔE_c . It is generally considered that the doping efficiency in MBE growth slightly depends on the content. Plugging the experimental results of V_{th} into Eq. (1), and using $\phi_b = 0.86$ eV,²² $\Delta E_c = 0.25 + 0.8 \cdot x$ eV,²⁵ effective doping densities of $2.7 \times 10^{18}/\text{cm}^3$, $3.4 \times 10^{10}/\text{cm}^3$, and $3.5 \times 10^{18}/\text{cm}^3$ for $x=0.15$, 0.2 , and 0.22 were obtained, respectively. That is, from our experimental results, we conclude that effective doping density is higher when indium content x is larger. When indium content x is increased, the conduction band discontinuity of GaAs and $\text{In}_x\text{Ga}_{1-x}\text{As}$ increases, which contributes to carrier confinement and thus linearity. However, since doping efficiency also increases with increasing x , Fermi level will increase as well, which means that carriers will be less confined if doping density is too high. Therefore, there exist an optimum doping (or threshold voltage) in these devices we considered. This explains why the linearity became better when x is increased from 0 to 0.15 and became to degrade from $x=0.2$ to 0.22 as we mentioned previously.

Although the calculated effective doping density of $x=0.22$ is larger than $x=0.2$ or $x=0.15$, the measured sheet charge density is lower than $x=0.2$. This can be explained by interface state charge density (Q_I) as follows. Under the first-order approximation, sheet charge density can be given by $Q_s = (\epsilon/d) \cdot (V_G - V_{\text{th}}) - Q_I$. If we assume Q_I is equal to $10^{12}/\text{cm}^2$ when $x=0.22$ and is equal to 0 when $x=0.15$ and $x=0.2$ for simplicity, and use the experimental V_{th} as listed in Table II, sheet charge densities of $2.30 \times 10^{12}/\text{cm}^2$, $3.82 \times 10^{12}/\text{cm}^2$, $5.24 \times 10^{12}/\text{cm}^2$, and $4.54 \times 10^{12}/\text{cm}^2$ can be obtained for devices with $x=0$, 0.15 , 0.2 , and 0.22 , respectively. The trend is consistent with the Hall measurement.

The room temperature dc characteristics for the $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) DCFETs with 1- μm -long gate were summarized in Table II. We observed an enhancement of $g_{m,\text{ext}}$ from 241 mS/mm for $x=0$ to 350 mS/mm for $x=0.15$ DCFETs. However, $g_{m,\text{ext}}$ values dropped to 306 mS/mm for $x=0.20$ and 275 mS/mm for $x=0.22$ DCFETs. The reason why $g_{m,\text{ext}}$ behaved differently from carrier density and mobility is still not very clear to us at this time but we propose the following explanation. By extending the above-mentioned theory of Delagebeaudeuf

and Linh, it can be easily derived that normalized transconductance g_m of a DCFET operated at its saturation electron velocity v_s is given by

$$g_m = \frac{\epsilon_2 v_s}{d}. \quad (2)$$

The saturation velocity of $\text{In}_x\text{Ga}_{1-x}\text{As}$ is larger than that of GaAs and hence therefore corresponding g_m 's are larger than that of GaAs. However, as we mentioned before, in the case of $x=0.2$, the channel thickness is a little over the critical thickness and in the case of $x=0.22$, the channel thickness is far beyond the critical thickness. Also from the published data of Anderson *et al.*,²⁶ we found that our devices with $x=0.22$ and $x=0.2$ are located at the regions where large and relatively small concentration of structure defects appear, respectively, while the device with $x=0.15$ (channel thickness less than the critical thickness of 212 Å) is located at the region of high quality. Structure defects degrade electron saturation velocity and therefore g_m begin to degrade when x is equal or greater than 0.2. We believe carrier density and mobility did not degrade as much as the saturation velocity did. Therefore, carrier density and mobility of $x=0.2$ sample is still larger than that of $x=0.15$ sample whereas the saturation velocity of $x=0.2$ is smaller than that of $x=0.15$ and thus g_m of $x=0.2$ is smaller than that of $x=0.15$. Sources resistance for devices with $x=0$, 0.15 , 0.2 , and 0.22 were 1.21, 0.75, 0.69, and 0.74 Ω mm, respectively. By taking these source resistances into account, we found that intrinsic transconductances show similar characteristics to the extrinsic transconductances we used in Fig. 3 for discussion here. Therefore general conclusions deduced from the discussions using extrinsic transconductances remain unchanged.

The maximum channel current ($I_{\text{ds,max}}$) increased from 360 mS/mm when $x=0$, to 575 mA/mm when $x=0.15$, and to 630 mA/mm when $x=0.20$. A slight drop for $x=0.22$ was also observed. The dc characteristics of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) DCFETs were consistent with previous Hall measurements, and we concluded the optimized dc performance of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) DCFETs is obtained with the x value ranging between $x=0.15$ and $x=0.20$ for a 150-Å-thick $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel.

IV. MICROWAVE CHARACTERISTICS

Microwave on-wafer S parameters for $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) DCFETs with 1.0- μm -long gate were measured in common-source configuration from 45 MHz to 40 GHz by an HP8510C network analyzer in conjunction with Cascade probes. As can be seen clearly in Fig. 4, f_{max} 's and f_t 's of strained devices were much higher than those of the lattice-matched one ($x=0$). The flat region of f_{max} 's and f_t 's of strained devices were also much wider than those of the lattice-matched one ($x=0$).

Table III is a summary of the results of maximum oscillation frequency (f_{max}) and current-gain cutoff frequency (f_t) for all devices ($x=0$, 0.15 , 0.20 , 0.22) biased at V_{ds}

FIG. 4. Maximum oscillation frequency ($f_{\max}$'s) and current gain cut-off frequency (f_T 's) as a function of I_{ds} of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) doped-channel FETs with $1.0\text{-}\mu\text{m}$ -long gate.

$=4\text{ V}$, with V_{gs} tuned for a maximum S_{21} . The average transit frequencies were $f_T = 21.6\text{ GHz}$ and $f_{\max} = 53.2\text{ GHz}$ for $x = 0.20$ DCFETs. These values were roughly 23% and 52% higher than those ($f_T = 17.6\text{ GHz}$ and $f_{\max} = 34.9\text{ GHz}$) of the lattice-matched DCFETs ($x = 0$). The microwave performance started to degrade by further increase of the indium content x in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel, i.e., $f_T = 18.6\text{ GHz}$ and $f_{\max} = 48.1\text{ GHz}$ for $x = 0.22$. Note that the trend of the f_T 's with respect to the x is similar to the dependence of g_m on x , since f_T is directly proportional to g_m . The microwave characteristics from these $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) DCFETs were consistent with the previous dc investigations; namely, the performance was enhanced by increasing the indium content. From these results, again, we concluded that the optimized microwave performance of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ DCFETs is obtained with the x value ranging between $x = 0.15$ and $x = 0.20$ for a $150\text{-}\text{\AA}$ -thick $\text{In}_x\text{Ga}_{1-x}\text{As}$ doped channel.

V. CONCLUSION

Lattice-matched and strained $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) DCFETs were investigated in terms of dc and microwave performance. Due to superior transport properties of $\text{In}_x\text{Ga}_{1-x}\text{As}$, high-quality undoped

high-band-gap $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ insulating layer, large Schottky barrier and $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}$ conduction band offset, high current drivability, high breakdown, high linearity, and high speed $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ pseudomorphic DCFETs were achieved. The experimental results suggest that the optimized indium content of an $150\text{-}\text{\AA}$ -thick $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel is around $x = 0.15$ to $x = 0.20$. Degradation of device performance was observed for larger indium content ($x = 0.22$), which was associated with strain relaxation in this highly strained channel. These results showed that the $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ DCFETs with indium content x between 0.15 and 0.20 were very suitable for microwave high power device applications.

ACKNOWLEDGMENT

Support from the National Science Council of R.O.C. under Contract No. NSC88-2219-E-002-009 is acknowledged.

- ¹L. D. Nguyen, P. J. Tasker, D. C. Radulescu, and L. F. Eastman, IEEE Trans. Electron Devices **36**, 2243 (1989).
- ²R. E. Lee, R. S. Beaubian, R. H. Noton, and J. W. Bacon, in IEEE MTT-S Technical Digest 1989, p. 975.
- ³K. L. Tan, R. M. Dia, D. C. Streit, A. C. Han, T. Q. Trinh, J. R. Velebir, P. H. Liu, T. Lin, H. C. Yen, M. Sholley, and L. Shaw, IEEE Electron Device Lett. **11**, 303 (1990).
- ⁴B. Kim, H. D. Shih, M. Wurtele, and H. Q. Tserng, IEEE Electron Device Lett. **9**, 203 (1988).
- ⁵P. M. Smith, in IEEE IEDM Technical Digest, 1987, p. 464.
- ⁶P. Saunier, R. J. Matyi, and Bradshaw, IEEE Electron Device Lett. **9**, 397 (1988).
- ⁷S. S. Lu, C. L. Huang, and T. P. Sun, Solid-State Electron. **38**, 25 (1995).
- ⁸S. S. Lu and Y. J. Wang, IEEE Electron Device Lett. **15**, 70 (1994).
- ⁹Y. Okamoto, M. K. Matsunaga, and M. Kuzuhara, Electron. Lett. **31**, 2216 (1995).
- ¹⁰Y. S. Lin, S. S. Lu, and T. P. Sun, IEEE Electron Device Lett. **18**, 150 (1997).
- ¹¹B. Pereiaslavets, K. H. Bachem, J. Braunstein, and L. F. Eastman, IEEE Trans. Electron Devices **42**, 1659 (1995).
- ¹²A. Ginoudi, E. Paloura, G. Costandinidis, J. C. Garcia, and P. Maurel, in IRPM Technical Digest, 1992, p. 389.
- ¹³T. Saito, N. Hidika, K. Ono, Y. Ohashi, and T. Shimura, in GaAs IC Technical Digest, 1995, p. 222.
- ¹⁴H. Suehiro, M. Shima, T. Shimura, and N. Hara, in GaAs IC Technical Digest, 1996, p. 77.
- ¹⁵M. Takikawa and K. Joshin, IEEE Electron Device Lett. **14**, 406 (1993).
- ¹⁶B. Pereiaslavets, G. H. Martin, L. F. Eastman, R. W. Yanka, J. M. Ballingall, J. Braunstein, K. H. Bachem, and B. K. Ridley, IEEE Trans. Electron Devices **44**, 1341 (1997).
- ¹⁷D. Geiger, E. Mittermeier, J. Dickmann, C. Geng, R. Winterhof, F. Scholz, and E. Kohn, IEEE Trans. Electron Devices **1**, 259 (1997).
- ¹⁸K. Yamaguchi, N. Iwata, M. Kuzuhara, Y. Takayama, IEEE Trans. Electron Devices **45**, 361 (1998).
- ¹⁹Y. J. Chan, D. Pavlidis, M. Razeghi, and F. Omnes, IEEE Trans. Electron Devices **37**, 2141 (1990).
- ²⁰Y. J. Chan and M. T. Yang, IEEE Electron Device Lett. **16**, 33 (1995).
- ²¹M. T. Yang and Y. J. Chan, IEEE Trans. Electron Devices **43**, 1174 (1996).
- ²²T. J. Miller, G. B. Backes, and M. I. Nathan, J. Appl. Phys. **76**, 7931 (1994).
- ²³J. W. Matthews and A. E. Blakeslee, J. Cryst. Growth **27**, 118 (1974).
- ²⁴D. Delagebeaudeuf and N. T. Linh, IEEE Trans. Electron Devices **24**, 955 (1982).
- ²⁵See, for example, S. M. Sze, *High Speed Semiconductor Devices* (Wiley, New York, 1990), p. 292.
- ²⁶T. G. Anderson, Z. G. Chen, V. D. Kulakovskii, A. Uddin, and J. T. Vallin, Appl. Phys. Lett. **51**, 752 (1987).

TABLE III. Summary of microwave characteristics of $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ ($0 \leq x \leq 0.22$) doped-channel FETs with $1.0\text{-}\mu\text{m}$ -long gate.

In content	$x = 0$	$x = 0.15$	$x = 0.20$	$x = 0.22$
f_T (GHz)	17.6 ± 0.3	23.1 ± 0.4	21.6 ± 0.3	18.6 ± 0.3
$f_{\max}$ (GHz)	34.9 ± 0.4	50.8 ± 0.5	53.2 ± 0.5	48.1 ± 0.4