that of a single-loop SF-CDR, with temperature ranging from 0 to 90°C. In addition, after the CDR IC is locked, it maintains the lock status even if V_{EE} changes from -2.9 to -3.7V. This clearly shows the efficiency of the duplicated PLL technique.

Fig. 3 Temperature dependence of lock status

—●— higher and lower limits at which novel CDR holds lock
--○-- higher and lower limits at which single SF-CDR holds lock

Fig. 4 Jitter transfer function and output waveforms

— ITU-T template
□ measured

Fig. 4 shows the output waveforms and jitter transfer function when the input data rate is 2.48832Gbit/s. The clock extraction was very precise (the jitter generation is 0.0095 UI (3.8ps)) and the eye opening of the output data was sufficiently wide. The RMS jitter generation, jitter tolerance, and jitter transfer function meet the jitter specifications in the ITU-T recommendation for STM-16 (RMS jitter generation: less than 0.01 UI; jitter-tolerance: 1.5 UI up to 0.1MHz and a 20dB/decade rolloff to 1MHz; jitter transfer: peaking less than 0.1dB within a 2MHz bandwidth [2]). The power consumption (including that of the I/O circuit) is 0.77W.

Conclusion: A novel CDR IC based on the duplicated PLL technique has been developed using 0.5μm Si bipolar technology. The CDR IC, which has a power consumption of only 0.77W, has a lock range that is twice as wide as that of a single-loop CDR and it achieves an RMS jitter of less than 0.01 UI, good jitter-tolerance, and low jitter-transfer cutoff frequency, all of which meet the jitter requirements stipulated in the ITU-T recommendations, with a power consumption of only 0.77W.

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Analogue BiCMOS squarer and its applications

Cheng-Chieh Chang, Shen-Iuan Liu and Jiin-Long Lee

A BiCMOS squarer using active attenuators which has been fabricated in a 10μm BiCMOS process is presented. Experimental results show that the nonlinearity of the squarer can be kept below 2% across the entire input voltage range of ±0.3V. Its -3dB bandwidth is measured to be ~1MHz. Moreover, based on the proposed squarer circuits, a four-quadrant multiplier and a vector summation circuit have also been realised. The proposed circuits are expected to be useful in analogue signal processing applications.

Introduction: Many CMOS analogue signal-processing building blocks which exploited the characteristics of MOS transistors have been developed, such as transconductance amplifiers and multipliers [1-6] etc. In this Letter, a new BiCMOS squarer and multiplier and vector summation circuits are presented. One of the advantages of the proposed circuit is that it is self-biased without requiring additional biasing circuits. Experimental results are given to verify the theoretical analysis.

Fig. 1 Active attenuator circuit and proposed BiCMOS squarer

a Active attenuator
b Proposed BiCMOS squarer

Circuit description: The so-called active attenuator [4] or nested circuit [5] is shown in Fig. 1a. Assume that both the nMOS devices are biased in strong inversion with individual wells to avoid the body effect. Let the transconductance parameters of M_1 and M_2 be K_1 and K_2 , respectively. I_B is the DC current. For normal operation, M_1 will be in the triode region of operation and M_2 will be in saturation. Thus, the following equations can be obtained:

$$I_B = K_1 \left[(V_X - V_T)V_1 - \frac{V_1^2}{2} \right] \quad (1)$$

and

$$I_B = \frac{K_2(V_X - V_1 - V_T)^2}{2} \quad (2)$$

From eqns. 1 and 2, eliminating I_B

$$V_1 = \sqrt{2I_B} \left(\sqrt{\frac{1}{K_1} + \frac{1}{K_2}} - \sqrt{\frac{1}{K_2}} \right) \quad (3)$$

The proposed analogue BiCMOS squarer is shown in Fig. 1b. Assume that the current mirrors and the bipolar transistors are in their active region and the base-to-emitter voltages of Q_1 and Q_2 are equal. The collector current of Q_1 will equal the drain current of M_2 . Neglecting the base current, it will force the current I_a to zero. According to eqn. 3, the following equation can be obtained:

$$V_1 - V_2 = \frac{\sqrt{I_1}}{G} \quad (4)$$

where I_1 is the drain current of M_1 and $G = (\sqrt{1/K_1 + 1/K_2} - \sqrt{1/K_2})^{-1}$. However, the above derivation is based on the constraint that $V_1 > V_2$. The actual squarer is shown in Fig. 1b. The output current I_o of the proposed squarer circuit can be expressed as

$$I_o = G^2 (V_1 - V_2)^2 \quad (5)$$

Based on the quarter-square principle [3], an analogue four-quadrant multiplier can also be developed using the proposed squarer circuits. Moreover, this squarer can be used to realise a vector summation circuit [7]. The proposed vector summation circuit is shown in Fig. 2. By adding all the output currents of the squarer circuits and using the attenuator circuit as the square-rooting circuit, the output voltage of the proposed vector summation circuit can be derived as

$$V_o = \frac{G}{G_o} \sqrt{(V_{1x} - V_{1y})^2 + (V_{2x} - V_{2y})^2 + \dots + (V_{nx} - V_{ny})^2} \quad (6)$$

where the conductance $G_o = \sqrt{1/2}(\sqrt{1/K_{o1} + 1/K_{o2}} - \sqrt{1/K_{o1}})^{-1}$ and K_{o1} and K_{o2} are the transconductance parameters of transistors M_{o1} and M_{o2} .

Fig. 2 Proposed vector summation circuit

Fig. 3 Output waveform of multiplier with triangular signal (1kHz) and sinusoidal signal (10kHz) of amplitude 0.2V

Upper trace (1V/div): triangular signal
Lower trace (1V/div): output
Horizontal scale 500µs/div

Experimental results: The proposed circuits have been fabricated in a 10µm BiCMOS process. The aspect ratios of all the devices in Fig. 1b are listed in Table 1. The circuit was evaluated under the following measurement conditions: $R = 51\text{ k}\Omega$ and supply voltages of $\pm 2.5\text{V}$. The input range of the squarer has a nonlinearity of less than 2% within $\pm 0.3\text{V}$. The measured -3dB bandwidth of the squarer is $\sim 1\text{ MHz}$.

Table 1: Aspect ratios of devices in Fig. 1b

Transistor	M_1-M_3, M_7-M_9	$M_4-M_6, M_{10}-M_{12}$	$M_{13}-M_{14}$	Q_1-Q_4
W/L [µm/µm]	5/25	5/5	25/5	$A_E = 4 \times 4.4 \mu\text{m}^2$

The measured input range of the proposed multiplier is within $\pm 0.2\text{V}$. A typical multiplier output waveform is shown in Fig. 3 where both a triangular signal (1kHz) and sinusoidal signal (10kHz) with amplitude 0.2V are applied.

Fig. 4 Output waveform of two-input vector summation circuit

Upper trace (200mV/div): input signal
Lower trace (20mV/div): output
Horizontal scale 500µs/div

The measurement of the vector summation circuit requires additional external $n\text{MOS}$ transistors (denoted by *) which are commercial components (CD4007). Two sinusoidal signals are applied to the two-input (i.e. $n = 2$ in Fig. 3) vector summation circuit. One of the two signals is a 1kHz sinusoidal signal with an amplitude of 0.3V and the other is a 3kHz sinusoidal signal with the same amplitude. Its output waveform is shown in the lower trace (20mV/div) of Fig. 4 and one of the input signals is shown in the upper trace (200mV/div).

Conclusions: In this Letter, a BiCMOS squarer, a four-quadrant multiplier and a vector summation circuit have been presented by using the characteristics of MOS transistors. Experimental results have demonstrated their performance. The proposed circuits are expected to be useful in analogue signal processing applications.

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Application of linearly independent arithmetic transform in testing of digital circuits

S. Rahardja and B.J. Falkowski

Recently introduced linearly independent arithmetic transforms and their corresponding spectral coefficients are used to detect faults in digital circuits. The results show that for many classes of logical functions, the LIA logic transformations are advantageous in terms of the number of their coefficients that have to be checked to identify the faults when compared to the case of the well-known arithmetic transform.

Introduction: With the introduction of Perkowski linearly independent (PLI) logic [4, 5], there has been a great interest in researching this and related areas. The existence of numerous PLI transformations will find applications in the design of exclusive-or based polynomial expansions which can be implemented in the form of readily available fine grain FPGAs and EPLDs. The algebra of PLI logic is strictly in $GF(2)$. A direct extension of PLI logic is a conversion of $GF(2)$ logic into an equivalent polynomial expansion where the arithmetic operations are addition, subtraction and multiplication. This leads to a derivation of a new logic family known as linearly independent arithmetic (LIA) logic [6]. The arithmetic transform [1, 2] is merely one of the many LIA transformations and has been extensively used in the testing and probabilistic analysis of logical circuits. In this Letter, comparisons of the application of various LIA transforms in the detection of stuck-at and bridging faults [1] are made.

Fault detection: A digital circuit realising a logical function $f(\vec{x}_n)$ is said to be faulty if permanent functional faults exist in the circuit that cause the output of the circuit to differ from the original $f(\vec{x}_n)$.

Definition 1: Let M_n be an LIA transformation matrix. If a digital circuit which is designed to realise $f(\vec{x}_n)$ has a permanent failure that produces a faulty function $f(\vec{x}'_n) \neq f(\vec{x}_n)$, then the LIA coefficient vectors are $\vec{A} = M_n^{-1} \vec{F} \neq M_n^{-1} \vec{F}' = \vec{A}'$, where $\vec{F}$ and $\vec{F}'$ are the truth vectors of the original and faulty functions, respectively. Hence, if a circuit is faulty, the unique spectral signature will deviate from the expected value. Thus, the detection of faults may be carried out by the simple verification of a spectral signature.

For every LIA transformation matrix, there exist different LIA spectral representations of a logical function. The logical function is uniquely expressed as the summation of the product of LIA coefficients and their PLI set of basis functions. If the function is faulty, again the detection of faults by verification of a signature will solely depend on the particular combination of the PLI set of basis functions of the transform.

Lemma 1: Let M_n be defined as in definition 1 and A_j represent all the LIA spectral coefficients necessary for the detection of all input stuck-at and bridging faults, where $j \in J$ is a set of all integers representing the subscripts of A_j . If

$$M'_n = [\vec{g}_{2^n-1}, \vec{g}_{2^n-2}, \dots, \vec{g}_0]$$

is another LIA transformation matrix the columns of which consist of the reverse arrangements of the set of PLI logical functions in M_n then A_{2^n-1-j} represents the LIA spectral coefficients necessary for the detection of all input stuck-at and bridging faults, and $j \in J$.

Class	LIA matrix	Bridging faults				Stuck-at faults			
		NPN ₂	NPN ₃	NPN ₄	all	NPN ₂	NPN ₃	NPN ₄	all
A	$[M_{n-1} O_{n-1}]$	<i>A₃</i>	<i>A₃</i>	<i>A₃</i>	<i>A₃</i>	<i>A₁A₂</i>	<i>A₃</i>	<i>A₃</i>	<i>A₁A₂A₃</i>
	$[M_{n-1} M_{n-1}]$	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₁A₂</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀A₁A₂</i>
B	$[O_{n-1} M_{n-1}]$	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀</i>	<i>A₀A₁</i>	<i>A₁A₂</i>	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀A₁A₂</i>
	$[O_{n-1} M_{n-1}]$	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀</i>	<i>A₀A₁</i>	<i>A₁A₂</i>	<i>A₀A₁</i>	<i>A₀</i>	<i>A₀A₁A₂</i>
	$[O_{n-1} J_{n-1}]$	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀A₁A₂</i>	<i>A₀A₁</i>	<i>A₀</i>	<i>A₀A₁A₂</i>
	$[M_{n-1} J_{n-1}]$	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₁A₂A₃</i>	<i>A₀</i>	<i>A₀</i>	<i>all</i>
	$[O_{n-1} I_{n-1}]$	<i>A₁</i>	<i>A₀A₁</i>	<i>A₀</i>	<i>A₀A₁</i>	<i>A₁</i>	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀A₁</i>
	$[M_{n-1} I_{n-1}]$	<i>A₁</i>	<i>A₀A₁</i>	<i>A₀</i>	<i>A₀A₁</i>	<i>A₁</i>	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀A₁</i>
	$[O_{n-1} M_{n-1}]$	<i>A₀A₂</i>	<i>A₀A₂</i>	<i>A₀</i>	<i>A₀A₁A₂</i>	<i>A₀A₂</i>	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀A₁A₂</i>
	$[O_{n-1} I_{n-1}]$	<i>A₀</i>	<i>A₀A₂</i>	<i>A₂</i>	<i>A₀A₂</i>	<i>A₁</i>	<i>A₀A₂</i>	<i>A₀A₁</i>	<i>A₀A₁</i>
C	$[O_{n-1} M_{n-1}]$	<i>A₁</i>	<i>A₀A₁</i>	<i>A₀</i>	<i>A₀A₁</i>	<i>A₁</i>	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀A₁</i>
	$[J_{n-1} J_{n-1}]$	<i>A₀</i>	<i>A₀A₂</i>	<i>A₂</i>	<i>A₀A₂</i>	<i>A₁</i>	<i>A₀A₁</i>	<i>A₁</i>	<i>A₀A₁</i>
	$[J_{n-1} M_{n-1}]$	<i>A₀A₂</i>	<i>A₀A₂</i>	<i>A₀</i>	<i>A₀A₂</i>	<i>A₀A₂</i>	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀A₁A₂</i>
	$[O_{n-1} J_{n-1}]$	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₁A₂A₃</i>	<i>A₀</i>	<i>A₀</i>	<i>all</i>
	$[M_{n-1} I_{n-1}]$	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₁A₂A₃</i>	<i>A₀</i>	<i>A₀</i>	<i>all</i>
	$[I_{n-1} M_{n-1}]$	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀</i>	<i>A₀A₁</i>	<i>A₀A₂</i>	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₀A₁A₂</i>
	$[I_{n-1} I_{n-1}]$	<i>A₀A₁</i>	<i>A₀A₁</i>	<i>A₁</i>	<i>A₀A₁</i>	<i>A₁A₂</i>	<i>A₀A₁</i>	<i>A₀</i>	<i>A₀A₁A₂</i>
	$[M_{n-1} M_{n-1}]$	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀A₁A₂</i>	<i>A₀</i>	<i>A₀</i>	<i>A₀A₁A₂</i>

Fig. 1 Detection of input stuck-at or bridging faults using different classes of LIA spectral coefficients under NPN classes of logical functions

Fig. 1 shows a summary of the methods for detecting input stuck-at or bridging faults using different classes of LIA transformation matrices which were introduced in [6]. In the Figure, O_{n-1} is a $2^{n-1} \times 2^{n-1}$ square matrix with all its elements 0, I_{n-1} is a $2^{n-1} \times 2^{n-1}$ identity matrix, and J_{n-1} is a $2^{n-1} \times 2^{n-1}$ reverse-identity matrix, i.e. elements in the reverse-diagonal positions with all others 0. The detection of faults is classified by two-variable NPN-equivalence classes [3]. For $n = 2$, there are altogether four NPN classes, denoted NPN₁, NPN₂, NPN₃ and NPN₄. The number of LIA spectral coefficients required to detect input stuck-at or bridging faults for a specific NPN class is shown in bold letters in Fig. 1. The required spectral coefficients are shown in italics.

From Fig. 1 it can be seen that for the arithmetic transformation matrices (class A), only one spectral coefficient is necessary to detect bridging faults for all two-variable logical functions. Comparing with other transformation matrices, the arithmetic transform is optimal, while some other transformation matrices also require only one spectral coefficient to detect the fault. For the linear functions [3], only one spectral coefficient is required for the detection of bridging faults regardless of the chosen transformation matrix. In the detection of stuck-at faults, the matrices in class A require two spectral coefficients for the NPN₂ and NPN₃ classes, and one spectral coefficient for the NPN₄ class. Generally, for any two-variable logical function, a total of three spectral coefficients are needed. Forming a comparison with other LIA transformation matrices, the minimal number of spectral coefficients required for the detection of input stuck-at faults of all two-variable logical functions is 2.